Class-AB Large-Swing CMOS Buffer Amplifier with Controlled Bias Current

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***Abstract*—A class-AB large swing CMOS buffer amplifier with new error amplifier circuits is presented. The error amplifier accurately controls the quiescent current through the output transistors, thereby reducing the variation of the quiescent power dissipation due to process and temperature variations. The buffer amplifier fabricated using 1.2-μm CMOS technology occupies an area of 103 mil^2 and dissipates an average of 4.7 mW under the quiescent condition with the standard deviation of only 3.2% of the average value. It has −63.6 dB THD with 3.5 V_{pp} output swing into a 300 Ω/150 pF load at 5 kHz.**

I. Introduction

ALTHOUGH a class-AB configuration employing a complementary source follower is well suited for minimizing the quiescent power dissipation of the CMOS output buffer amplifier, it has limited applications because of the reduced output swing. Thus an output buffer employing a pseudo-source follower shown in Fig. 1 has been widely used for a large swing output [1]–[5]. It is composed of a pair of common source MOS transistors and a pair of complementary error amplifiers. However, the quiescent current of the output buffer shown in Fig. 1 may have a large variation from the design target value due to the random offset voltage of the error amplifier. To reduce such variation an additional block may be inserted, which senses the current flow through the output transistors and controls the current to the target value [2]; or a source follower may be added to the circuit [3]–[5]. Although these approaches could alleviate such problems, the circuit area of the buffer is increased and the additional part of the circuit draws more current. In this paper a large-swing CMOS buffer amplifier using a low-gain, bias-controlled amplifier as the error amplifier is presented. Minimizing the variation of the quiescent current is our primary design goal as well as achieving high performance. This amplifier is designed to drive public telephone lines at voice band frequencies for telecommunication and audio applications.

II. Circuit Description

The proposed buffer amplifier consists of a high-gain input stage and a unity gain class-AB output stage. The input stage is a conventional two-stage amplifier which is comprised of a differential amplifier and a common source amplifier. The output stage includes two complementary error amplifiers and two output transistors as shown in Fig. 1.

Fig. 2 shows the circuit schematic of the error amplifier for driving the n-channel output transistor M32. To enable this error amplifier to be operated with input voltages near the

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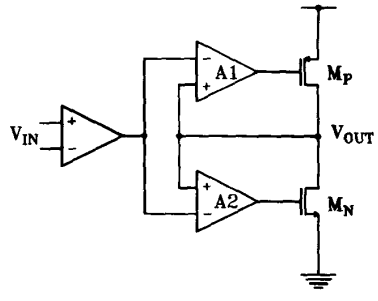


Fig. 1. Complementary class-AB output buffer amplifier.

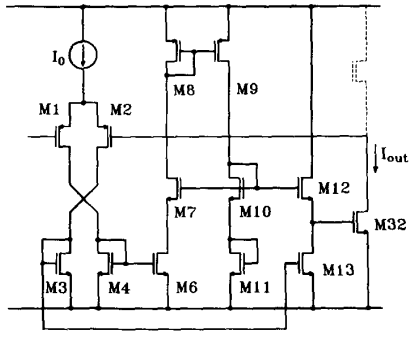


Fig. 2. Circuit schematic of the error amplifier.

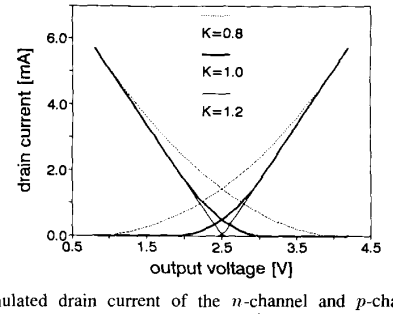


Fig. 3. Simulated drain current of the n-channel and p-channel output transistors with different K values.

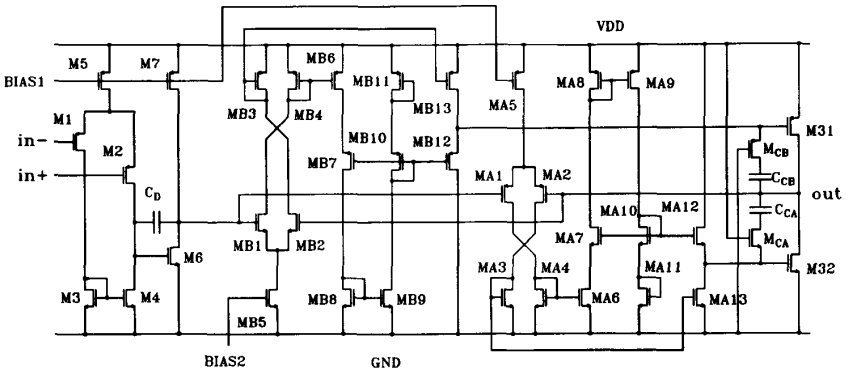


Fig. 4. Complete circuit schematic of the CMOS buffer amplifier.

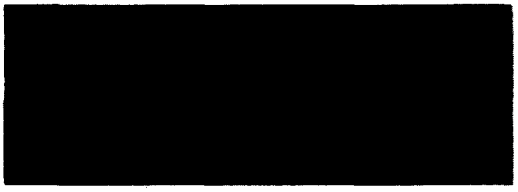


Fig. 5. Photomicrograph of the buffer amplifier.

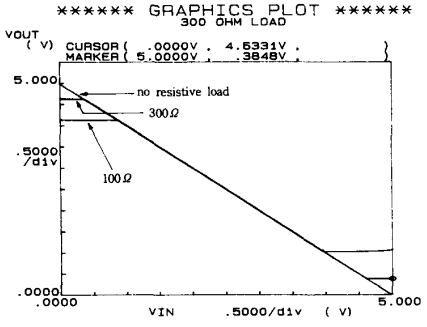


Fig. 6. DC transfer characteristics of the amplifier connected in an inverting unity-gain configuration with 100 Ω, 300 Ω, and no resistive load.

negative supply, a source-coupled pair of pMOS transistors are employed. Due to the back-bias effect this pair provides a common-mode input range exceeding the negative supply. The dual of this circuit is used to drive the p-channel output transistor.

To reduce the variation of the quiescent current due to random offset voltage, the open loop gain of the error amplifier must have a relatively small value of an order of 10 [1]. Such low voltage gain can be achieved using a low resistance load like the diode-connected transistor M10. With this configuration we obtained an open loop voltage gain of about 11, so that 2 mV of input offset voltage of the error amplifier results in 22 mV of output offset voltage. At $I_{D32} = 500\,\mu$A, this amount of output voltage change in the error amplifier causes the output quiescent current to change by about 16%, which is acceptable.

One requirement of the error amplifier is that it has to provide a large voltage swing on the gate of the output transistor to drive the resistive load with a moderately sized output transistor. The maximum voltage swing of a standard differential stage with a current mirror load is only approximately 1.5 V [5]. The proposed error amplifier shown in Fig. 2 can drive the gate of the output transistor M32 up to $V_{DD} - V_{T,M12}$. The SPICE simulation shows that the maximum gate voltage swing is 3.2 V, which is about twice the value achieved with the standard configuration.

Another requirement in designing the error amplifier is that it must provide the correct quiescent dc output voltage to yield the desired quiescent current of the output transistor. In the balanced quiescent condition, the drain currents of transistor M1 and M2 are equal to half the bias current I_0. Because the sizes of transistor M10 and M11 are the same as those of transistor M12 and M13, respectively and the drain currents of these four transistors are the same, the drain voltage of transistor M13 is same as the gate voltage. Thus the drain current of the output transistor M32, the quiescent current, is given by

$$I_{\mathrm{OUT}} = I_{\mathrm{D13}} \cdot \frac{(W/L)_{32}}{(W/L)_{13}}. \tag{1}$$

The drain current I_{D13} of M13 is

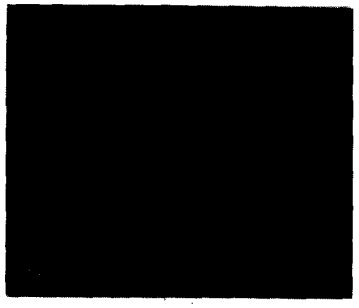
$$I_{\mathrm{D13}} = I_{\mathrm{D3}} \cdot \frac{(W/L)_{13}}{(W/L)_{3}}. \tag{2}$$

Since the drain current of M3 is equal to half of the bias current I_0, we can derive the output current by combining (1) and (2), which is given by

$$I_{\mathrm{OUT}} = \frac{1}{2} \cdot \frac{(W/L)_{32}}{(W/L)_{3}} \cdot I_0. \tag{3}$$

(3) shows that the quiescent current of this output buffer is linearly related to the bias current I_0 and the W/L ratio of the two transistors M3 and M32.

If we want to decrease the quiescent current without sacrificing the current drive capability, we can make the size of M13 larger. If we increase the size of M13 by a factor of K,



(a)

(b)

Fig. 7. Transient responses of the amplifier connected in a noninverting unity-gain configuration with 5-V single supply and 300 Ω/150 pF load; (a) a 3.5 V_{pp} step, (b) a 20 mV_{pp} step.

the gate over-drive of M32, $V_{GS,M32} - V_{T,M32}$, is given by

$$\begin{aligned} & V_{GS,M32} - V_{T,M32} \\ & = V_{GS,M10} + V_{GS,M11} - V_{GS,M12} - V_{T,M32} \\ & = \sqrt{\frac{2\left(\frac{W_{11}}{W_3}\right)\cdot\left(\frac{I_0}{2}\right)}{\mu C_{ox}\left(\frac{W_{10}}{L_{10}}\right)}}(1-\sqrt{K}) + \sqrt{\frac{2\left(\frac{W_{11}}{W_3}\right)\cdot\left(\frac{I_0}{2}\right)}{\mu C_{ox}\left(\frac{W_{11}}{L_{11}}\right)}} \\ & \quad + (V_{T,M10} - V_{T,M12}) \end{aligned} \tag{4}$$

assuming $W_{12} = W_{10}$, $W_4 = W_3$, $W_6 = W_{11}$, and $L_{12} = L_{10}$.

(3) can be derived from (4) as a special case of $K = 1$. Since the back-bias effects are almost compensated by taking the difference of the threshold voltages of the transistors M10 and M12 as shown in the last part of (4), the output is a primary function of only $(W/L)_{32}$, $(W/L)_{13}$, and I_0. Fig. 3 shows the simulated drain current of the n-channel and p-channel output transistors at three different K values, 0.8, 1.0, and 1.2. We can see that the quiescent current, the current at 2.5 V, is decreased as K is increased. Because the W/L ratios of the transistor M10 and M12 are small and that of the output transistor M32 is large, a small change of the current of the transistor M10 and M12 causes large change of the output current as shown in Fig. 3.

Fig. 4 shows the complete circuit diagram of the output buffer amplifier. The W/L values of the transistors used in this circuit are summarized in Table I.

TABLE I
DEVICE SIZES

M1	50/5	MA1	100/4	MB1	60/6
M2	50/5	MA2	100/4	MB2	60/6
M3	4/6	MA3	30/6	MB3	50/4
M4	4/6	MA4	30/6	MB4	50/4
M5	12.5/5	MA5	50/5	MB5	50/5
M6	16/6	MA6	120/6	MB6	200/4
M7	25/5	MA7	6/15	MB7	5/5
M31	750/2	MA8	50/5	MB8	50/6
M32	500/2.5	MA9	50/5	MB9	50/6
C_D	15 pF	MA10	6/15	MB10	5/5
C_{CA}	6 pF	MA11	120/6	MB11	200/4
C_{CB}	6 pF	MA12	6/15	MB12	5/5
		MA13	120/6	MB13	200/4
		M_{CA}	6.8/3	M_{CB}	10/2

TABLE II
OUTPUT BUFFER AMPLIFIER PERFORMANCE SUMMARY
(V_{DD} = 5 V, R_L = 300 Ω, C_L = 150 pF)

Parameters	Measured Results
Die area	103 mil^2
A_{vol}	85 dB
F_u	397 kHz
Phase margin	55°
PSRR + (dc)	101 dB
(1 kHz)	96 dB
PSRR - (dc)	106 dB
(1 kHz)	79 dB
CMRR (dc)	111 dB
(1 kHz)	75 dB
Harmonic distortion	
(freq. = 5 kHz)	
$V_{out,pp}$ = 3.5 V	
R_L = 300 Ω HD2	-71.7 dB
HD3	-68.5 dB
R_L = 3kΩ HD2	-66.7 dB
HD3	-81.5 dB
$V_{out,pp}$ = 4.0 V	
R_L = 300 Ω HD2	-68.5 dB
HD3	-66.2 dB
R_L = 3 kΩ HD2	-66.0 dB
HD3	-82.6 dB
$S/(THD + N)$	
($V_{out,pp}$ = 3.5 V, freq. = 5 kHz)	
R_L = 300 Ω	63.6 dB
R_L = 3 kΩ	66.4 dB
Slew rate	0.65 V/μs
V_{offset}	
avg	-1.3 mV
std	1.5 mV
Power dissipation	
avg	4.7 mW
std	0.15 mW
Output swing	4.25 V

AC stability of the complete amplifier is guaranteed when we provide a wide-band output stage and compensate the input stage to produce a dominant pole. The dominant pole in the input stage is formed by the Miller capacitor, C_D. The compensation of each error amplifier in the output stage is done with a Miller capacitor, C_C and a zero nulling resistor, M_C.

III. Experimental Results

The output buffer amplifier presented was fabricated using 1.2-μm, n-well, double-polysilicon, double-metal CMOS technology. A photomicrograph of the output buffer is shown in Fig. 5. The total die area of the amplifier is only 103 mil^2. The curves in Fig. 6 show the dc transfer characteristics in an inverting unity-gain configuration with different resistive loads under a single 5-V supply. The output voltage swing of the buffer amplifier is 4.25 V and within 0.38 V from each power rail in case of 300 Ω load. Fig. 7 shows the step response of the buffer amplifier connected in a non-inverting unity-gain configuration. Fig. 7(a) and (b) show the large signal response with a 3.5 V_{pp} output and the small signal response with a 20 mV_{pp} output, respectively. The average value of the measured offset voltage of the amplifier is 1.3 mV and the standard deviation is 1.5 mV. The average power dissipation measured from samples in two different lots is 4.7 mW and the standard deviation is 0.15 mW, which is only 3.2% of the average value. The total harmonic distortion of the amplifier is -63.6 dB with a 3.5 V_{pp} output swing into a 300 Ω/150 pF load at 5 kHz. All the measured results are summarized in the Table II.

IV. Summary

A full CMOS class-AB buffer amplifier has been presented which has a large output voltage swing on a low impedance load. The amplifier dissipates 4.7 mW of quiescent power to a 300-Ω load under a 5.0-V single supply and the standard deviation of the quiescent power dissipation is only 3.2% of the average value.

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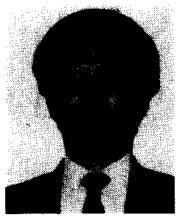

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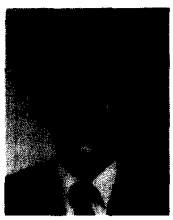

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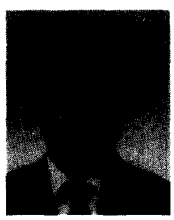

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