High-Speed Low-Power Darlington ECL Circuit

C. T. Chuang, K. Chin, P. F. Lu, and H. J. Shin

Abstract— **This paper presents an ECL circuit with a Darlington configured dynamic current source and active-pull-down emitter-follower stage for low-power high-speed gate array application. The dynamic current source provides a large dynamic current during the switching transient to improve the power delay of the logic stage (current switch). A novel self-biasing scheme for the dynamic current source and the active-pull-down transistor with no additional devices and power in the biasing circuit is described. Based on a 0.8-μm double-poly self-aligned bipolar technology at a power consumption of 1 mW/gate, the circuit offers 28% improvement in the loaded ($FI/FO = 3, C_L = 0.3$ pF) delay and 42% improvement in the load driving capability compared with the conventional ECL circuit. The design and scaling considerations of the circuit are discussed.**

I. Introduction

THE power dissipation of high-speed bipolar ECL circuits [Fig. 1(a)] has long been known to limit their VLSI applications. Recently, various active-pull-down schemes [1]–[4] have been actively pursued to reduce the power consumption and enhance the speed of ECL circuit. While these schemes reduce the dc power consumption in the emitter-follower stage and improve the pull-down delay, there are still some constraints limiting the use of these circuits for low-power high-speed gate array applications. For example, 1) a special element, such as a capacitor [1]–[3] or charge storage diode [4] is used to couple the signal from the logic stage to the base of the pull-down n–p–n transistor, 2) substantial power consumption is still needed in the current switch to achieve fast switching, 3) additional devices are needed to implement the biasing circuit for the active-pull-down transistor, 4) the power consumption for the biasing circuit is wasted, and 5) large resistor values (typically several tens of kΩ) are needed for the biasing circuit to minimize the biasing power (the biasing current is typically kept at several tens of μA). The large resistor values not only have direct impact on the cell size but also imply a dual sheet-resistance process and added process complexity (especially if polysilicon resistors are used) since the collector load resistors are typically in the range of about 0.5–2.0 kΩ.

II. Circuit Configuration and Operation

In the present scheme [Fig. 1(b)], resistors R_{S1} and R_{S2} form the current source as in a regular ECL circuit. An additional transistor Q_S is added, which, together with the input transistor Q_1, forms a Darlington configured dynamic current source to provide a large current only during the switching transient. Resistors R_{S1} and R_{S2} not only act as the steady-state current source but also form the biasing circuit for Q_S. Transistor Q_S is biased at near cut-in condition with essentially no dc current when the input is "Low." (The V_{BE} of Q_S is set by the voltage drop of the steady state switching current across the resistor R_{S1}.) When the input rises to "High," the voltage at node A follows immediately once the input crosses the reference voltage, resulting in transient overdrive at the base of Q_S and hence large dynamic current for fast pull-down of the collector node C. Notice that while the loading at node C is increased due to the capacitances associated with the collector of Q_S, the large dynamic current provided by Q_S overwhelms this additional loading (especially for the loaded case with multiple fan-in) and improves the switching speed of the logic stage with no (or very little) additional power consumption.

This Darlington-like scheme can be extended to the active-pull-down driving stage as shown in Fig. 1(b), where the active-pull-down transistor Q_D forms a Darlington-like configuration with the input transistor Q_1. The biasing current of Q_D is established by R_D. Capacitor C_D is the speed-up capacitor for Q_D if desired. Notice that the whole biasing circuit for the active-pull-down transistor is established without extra devices and power consumption. Also, the power supply and I/O for the present circuit are compatible wih the conventional ECL

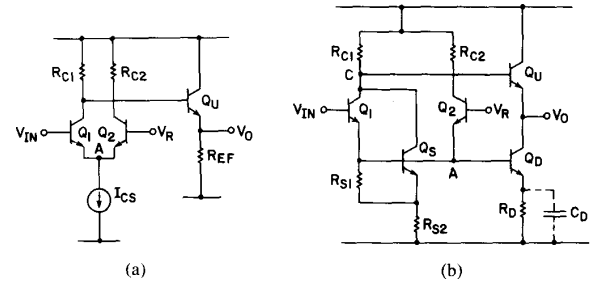


Fig. 1. Schematics of (a) conventional ECL circuit (the current source I_{CS} can be implemented either by a resistor or by a transistor current source), and (b) Darlington ECL circuit.

TABLE I
Typical Transistor Parameters

Design Rule	0.8 μm	0.5 μm
A_E (Wafer)	0.4 × 4 μm^2	0.25 × 2 μm^2
H_{FE}	100	120
Base Transit Time	6 ps	3 ps
C_{EB}	7.54 fF	5.96 fF
C_{CB}	3.8 fF	2.37 fF
C_{CS}	6.52 fF	4.82 fF
R_E	17.5 Ω	56 Ω
R_{BX}	164 Ω	200 Ω

Manuscript received October 15, 1992; revised June 25, 1993.

The authors are with IBM Research Division, T. J. Watson Research Center, Yorktown Heights, NY 10598.

IEEE Log Number 9211907.

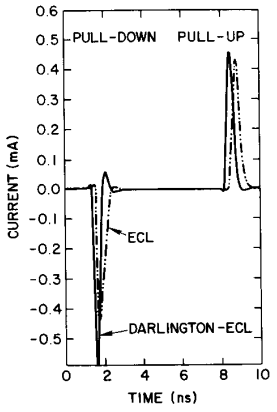


Fig. 2. Net pull-up and pull-down currents during the switching transient for the conventional ECL circuit and the Darlington ECL circuit (0.8-μm design rule, $FI/FO = 3, C_L = 0.3$ pF, 1 mW/gate).

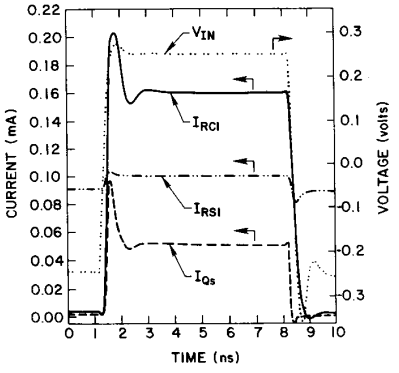


Fig. 3. Pertinent waveforms during the switching transient for the Darlington ECL circuit. V_{IN} is the voltage at the input, I_{RS1} is the current flowing through the (current source) resistor R_{S1}, I_{Qs} is the current flowing through the dynamic current source transistor Q_S, and I_{RC1} is the current flowing through the load resistor R_{C1} (0.8-μm design rule, $FI/FO = 3, C_L = 0.3$ pF, 1 mW/gate).

circuit, and the two circuits can be readily mixed to offer additional degree of freedom in design optimization.

Fig. 2 compares the net pull-up and pull-down currents of the present circuit with those for the conventional ECL circuit during the switching transient at a power consumption of 1 mW/gate with $FI/FO = 3$ and $C_L = 0.3$ pF. These waveforms are based on a 0.8-μm double-poly self-aligned bipolar technology [5], [6] with pertinent measured device parameters listed in Table I. The device parameters and models have been calibrated against the ECL circuit as well as static frequency divider performance. Clearly, the present circuit not only offers a larger, sharper pull-down current but also improves the pull-up current by shutting off Q_S and Q_D quickly and momentarily during the switching transient. (The speed in this case is 208 ps for the conventional ECL circuit and 150 ps for the present circuit.) The pertinent waveforms during the switching transient are shown in Fig. 3. The dynamic current through the dynamic current source I_{Qs} can be seen to add to the steady state switching current I_{RS1}, thus improving the switching speed of the logic stage.

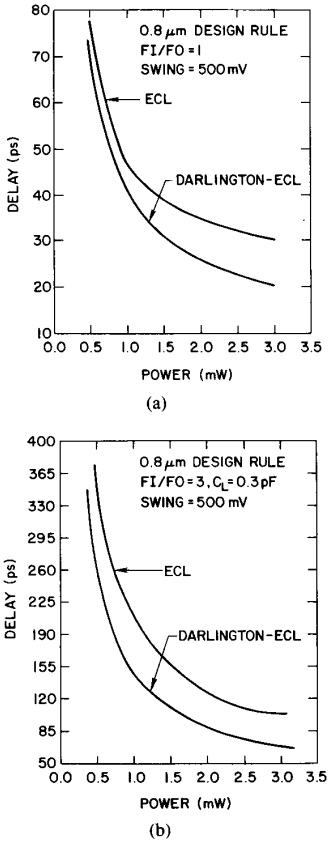
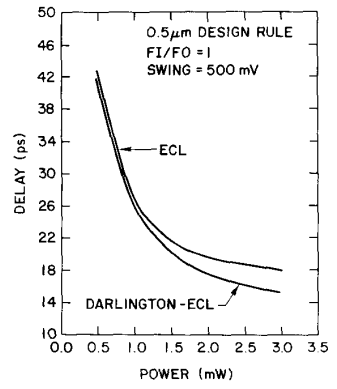


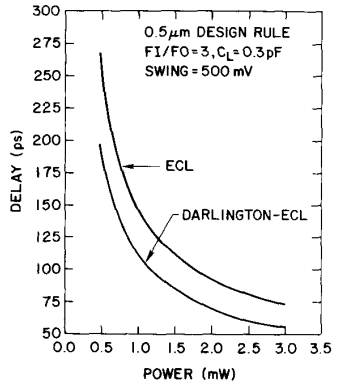
Fig. 4. (a) Unloaded ($FI/FO = 1$) power-delay characteristics, and (b) loaded ($FI/FO = 3, C_L = 0.3$ pF) power-delay characteristics for the conventional ECL circuit and the Darlington ECL circuit at 0.8-μm design rule.

III. Circuit Performance

The power-delay characteristics for the conventional ECL circuit and the present Darlington ECL circuit at 0.8-μm design rule (see Table I) are shown in Fig. 4. For the unloaded case [$FI/FO = 1$, see Fig. 4(a)] the speed improvement is about 11.5% (41.5 ps versus 46.9 ps) at 1 mW/gate and 32.5% (20.4 ps versus 30.2 ps) at 3 mW/gate with respect to the conventional ECL circuit. The smaller improvement at low power regime is expected due to the extra loading of the capacitances associated with the collector of the dynamic current source transistor Q_S on the collector node C, as discussed previously. For the loaded case [$FI/FO = 3, C_L = 0.3$ pF, see Fig. 4(b)], speed improvements of 28% (150 ps versus 208 ps) at 1 mW/gate and 34.6% (104 ps versus 68 ps) at 3 mW/gate are obtained compared with the conventional ECL circuit. Scaled performance of the conventional ECL circuit and the present circuit at 0.5- μm design rules are shown in Fig. 5. For the unloaded case [$FI/FO = 1$, see Fig. 5(a)], the present circuit achieves delays of 15.5 ps at 3.0 mW/gate and 26 ps at 1.0 mW/gate, respectively. For the loaded case [$FI/FO = 3, C_L = 0.3$ pF, see Fig. 5(b)], the delays are 56.8 ps at 3.0 mW/gate and 112 ps at 1.0 mW/gate.



(a)



(b)

Fig. 5. (a) Unloaded ($FI/FO = 1$) power-delay characteristics, and (b) loaded ($FI/FO = 3, C_L = 0.3$ pF) power-delay characteristics for the conventional ECL circuit and the Darlington ECL circuit at 0.5-μm design rule.

The superior load driving capability of the circuit is illustrated in Fig. 6. At 0.8-μm design rule with $FI/FO = 3$ and 1 mW/gate, the circuit achieves a driving capability of 203 ps/pF, a 42% improvement over the 352 ps/pF of the conventional ECL circuit.

IV. Discussion

The ac-noise sensitivity of the circuit is worth discussing. Notice that in the Darlington-like dynamic current source [Fig. 1(b)], the current flowing through R_{S2} is the sum of the current through R_{S1} and that through the dynamic current source Q_S. Suppose for any reason (due to either noise or disturbance), the voltage at node A rises. The current through R_{S1} and Q_S will increase. Hence the current through R_{S2} will increase, causing the voltage at the emitter of Q_S to rise, thus decreasing (or stabilizing) the current through R_{S1} and Q_S. So this feedback, basically a single-stage emitter degeneration feedback, helps terminate any transient disturbance.

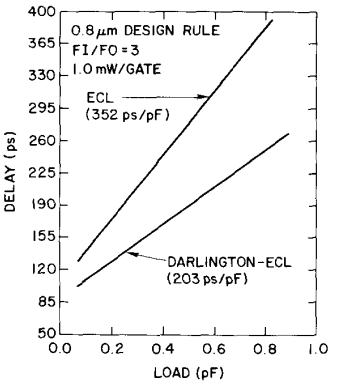


Fig. 6. Delays versus capacitive loading for the conventional ECL and the Darlington ECL circuit (0.8-μm design rule, $FI/FO = 3$, 1 mW/gate).

For the loop through the collector of Q_S, consider the case when the input rises for any reason. The voltage at node A follows. The current in Q_S will increase and the voltage at node C will decrease. However, this decrease in node C voltage is essentially isolated from node A (except for coupling through some second-order effect such as parasitic diffusion capacitance) and has only minor effect on the voltage/current at node A.

V. Conclusion

In summary, we have described a new high-speed low-power ECL circuit with Darlington configured dynamic current source and active-pull-down emitter-follower stage. The dynamic current source improves the power-delay of the logic state (current switch). A novel self-biasing scheme for the dynamic current source and the active-pull-down transistor with no additional devices/power in the biasing circuit was described. The superior power-delay performance, load driving capability, and improved scalability of the circuit were illustrated, and key aspects of the circuit were discussed.

References

[1] K. Y. Toh *et al.*, "A 23 ps/2.1 mW ECL gate," in *Dig. Tech. Papers, 1989 ISSCC*, pp. 224–225.

[2] K. Y. Toh, C. T. Chuang, T. C. Chen, and J. D. Warnock, "A 23-ps/2.1 mW ECL gate with an ac-coupled active-pull-down emitter-follower stage," *IEEE J. Solid-State Circuits*, vol. 24, no. 5, pp. 1301–1306, Oct. 1989.

[3] M. Usami and N. Shiozawa, "SPL (super push-pull logic): A bipolar novel low-power high-speed logic circuit," in *Dig. Tech. Papers, Symp. VLSI Circuits*, 1989, pp. 11–12.

[4] C. T. Chuang and K. Chin, "A high-speed low-power charge-buffered active-pull-down ECL circuit," in *Proc. 1990 IEEE Bipolar Circuits and Technology Meeting*, pp. 132–135.

[5] T. C. Chen *et al.*, "A submicron high performance bipolar technology," in *Dig. Tech. Papers, Symp. VLSI Technology*, 1989, pp. 87–88.

[6] T. C. Chen *et al.*, "A submicrometer high-performance bipolar technology," *IEEE Electron Device Lett.*, vol. 10, pp. 364–366, Aug. 1989.