Application Specific CMOS Output Driver Circuit Design Techniques to Reduce Simultaneous Switching Noise

R. Senthinathan and J. L. Prince

Abstract—**Application specific CMOS circuit design techniques to reduce simultaneous switching noise (SSN—also known as Delta-I noise or ground bounce) were analyzed. Detailed investigation on the CMOS output driver switching current components was performed. The limitations in using current controlled (CC) CMOS output drivers in high-speed (> 30 MHz) design applications are explained. Application specific, high-speed, controlled slew rate (CSR) CMOS output drivers were studied and designed. For a given device channel length, once the predriver and driver device sizes are fixed, the performance (speed, switching noise, sink/source capabilities) is determined. With controlled slew rate output drivers, more than 50% improvement was found in the input receiver noise immunity (measure of maximum tolerable SSN) compared to conventional drivers, while the speed and sink/source capabilities are preserved. This effective SSN reduction improvement is achieved with only a small increase in output driver silicon area. The CSR output driver uses distributed and weighted switching driver segments to control the output driver's slew rate for a given load capacitance. These CSR CMOS output drivers were compared with standard CMOS output drivers, showing significant reduction in effective switching noise pulse width.**

I. Introduction

As we scale down CMOS devices into the submicron region, the operating frequency of an output driver increases (frequencies over 60 MHz), which translates to reduction in rise/fall times and pulse width. For a 5-V supply, this corresponds to an output transient time less than 0.4 V/ns for a given load capacitance (i.e. $\tau_r = \tau_f < 2$ ns for $C_{\text{Load}} = 25\,pF$). Increase in output switching speed increases the rate of change of switching current (di/dt). Owing to the chip–package interface power (V_{DD}/V_{SS}) distribution parasitics, simultaneous switching noise (SSN) is created when output drivers switch simultaneously. It is essential that at any given arbitrary time T_0, SSN must be limited within the maximum allowable noise level. Unless power and ground noise are controlled, reliable operation of logic devices that are connected to the same V_{DD}/V_{SS} busses is not guaranteed. Some of the encountered problems with false operations due to simultaneous switching noise are 1) false triggering, 2) double clocking, and/or 3) missing clocked pulses [1], [2].

A typical chip–package interface is shown in Fig. 1 [2]. An output driver final stage circuit with lumped package parasitics is shown in Fig. 2 [2]. As we switch more and more high-current-drive outputs, not only is a low effective inductance L_{VSS} essential, but also clever circuit designs to control the di/dt through device-package V_{DD}/V_{SS}, in order to reduce SSN. Two different custom output driver design methodologies are often practiced in application specific integrated circuits (ASIC) [1]: 1) current controlled (CC) output driver [3], and 2) controlled slew rate (CSR) output driver [4]. In this work both the CC and the CSR output driver design methodologies are investigated in detail. In addition to reducing SSN, circuit design techniques have been used to control the reflection noise by controlling the output rise/fall times of the output drivers [5], [6]. SSN can be reduced by skewing and/or damping output driver switching noise waveform. The effects of skewing and/or damping switching waveform on the SSN, and the trade-offs in using these techniques, are explained in [7]. Application specific, tri-statable CSR CMOS output drivers were designed, and their performance and SSN are analyzed in detail. Performance and SSN of CSR output drivers were compared with conventional (current unregulated) output drivers. Advantages in using these CSR output drivers to switch a large number of outputs (> 32) are explained.

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R. Senthinathan is with APDC/Sector Technology, Motorola, Inc., Austin, TX 78762.

J. L. Prince is with the Center for Electronic Packaging Research, Department of Electrical and Computer Engineering, University of Arizona, Tucson, AZ 85721.

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II. CMOS Output Driver Switching Current Components

In order to design application specific CC or CSR output drivers, it is essential to understand the output driver switching current components. The di/dt is proportional to the ground noise for a given package design (L_{VSS} fixed). Notice that both the through current (also known as the overlap current) I_T and the charging/discharging current I_D contribute to the total switching current through the V_{DD}/V_{SS} device–package interface. The through current is the component of the output driver current flowing directly from the V_{DD} to V_{SS}. To demonstrate the impact of these current components on the total switching current, a standard CMOS output driver (for 1-μm L_{eff}: $W_P = 250, W_N = 160$) with 1 ns input risetime was used [1]. In this work, a typical lumped 168-pins pin grid array (PGA) package parasitics ($L_{VSS} = 5$ nH, $C_{VSS} = 1$ pF, and $R_{VSS} = 1\,\text{m}\Omega$) were selected for the SPICE simulations. The simple final stage of a CMOS output driver circuit is shown in Fig. 3(a). Three different capacitive loadings were selected for this study. Output voltage switching characteristics are shown in Fig. 3(b) for $C_{\text{Load}} = 0$, 25, 100 pF and curves A, B, and C, respectively. Switching current through the V_{SS} device–package interface path (source end of the N-channel transistor) is plotted in Fig. 3(c). Notice that since both the final stage P-channel and N-channel transistor inputs are connected to the same node (gates are tied together), through current is

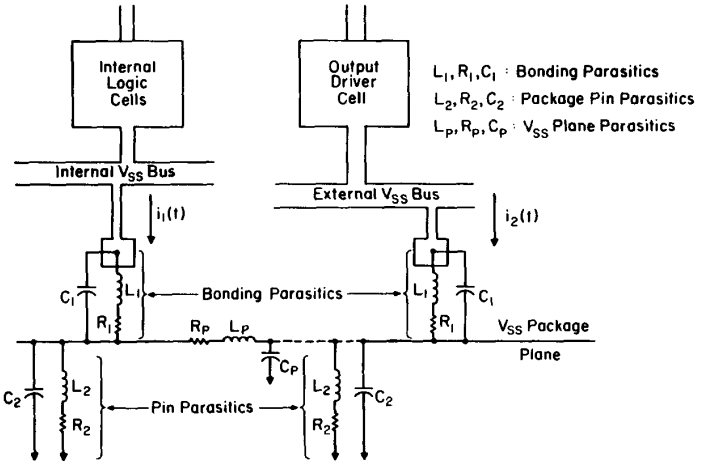

Fig. 1. A typical chip-package interface [2].

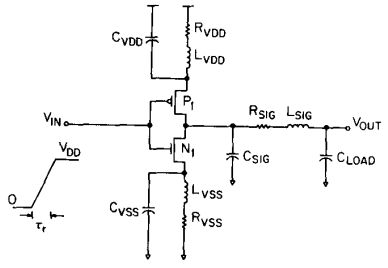

Fig. 2. Output driver final stage equivalent circuit [2].

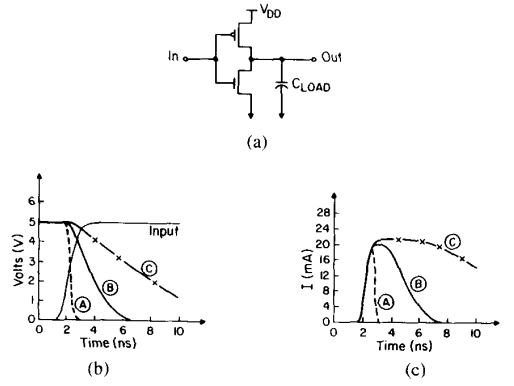

Fig. 3. (a) CMOS output driver switching characteristics. (b) Voltage switching characteristics. (c) Current switching characteristics. Here C_{Load} for case A = 0 pF, B = 26 pF, and C = 100 pF.

not minimized. This effect is illustrated in Fig. 3(c) where the rising edge of the total switching current is controlled by the through current for all three capacitive loadings. Because of this, the maximum di/dt is almost same for $C_{\text{Load}} = 0$, 25, and 100 pF. However, when the through current is turned off, total switching current is controlled by the discharging current, and this effect is evident from the falling edge of the total switching current shown in Fig. 3(c).

Note that the through current I_T does not contribute to charging or discharging the load capacitance, but contributes to the switching noise. This through current is present when both the P-channel and the N-channel transistors are in saturation region and momentarily ON. With clean (not noisy) V_{DD}/V_{SS} on-chip buses, the final output driver N-channel saturation current is [8]

$$I_N = \frac{K_N}{2}(V_g - V_{tn})^2 \tag{1}$$

where $K_N = \mu_n C_{ox}(W/L)$, V_g is the gate voltage, and V_{tn} is the N-channel transistor threshold voltage. Similarly, the P-channel saturation current is [8]

$$I_P = \frac{K_P}{2}(V_{DD} - V_g - V_{tp})^2 \tag{2}$$

where $K_P = \mu_p C_{ox}(W/L)$ and V_{tp} is the P-channel transistor threshold voltage. It has been shown that by requiring that $I_P = I_N$, the switching voltage V_{GT} is [9]

$$V_{GT} = \frac{\sqrt{K_P}V_{DD} + \sqrt{K_N}V_{tn} - \sqrt{K_P}V_{tp}}{\sqrt{K_P} + \sqrt{K_N}}. \tag{3}$$

The maximum through current $I_T(\max)$ is given by [9]

$$I_T(\max) = \frac{K_N K_P}{2(\sqrt{K_N} + \sqrt{K_P})}(V_{DD} - V_{tp} - V_{tn})^2. \tag{4}$$

The discharging current (I_D) when the output switches from V_{DD} to 0 V is

$$I_D = C_{\text{LOAD}}\frac{dV}{dt} \tag{5}$$

or, approximately,

$$I_D \approx C_{\text{Load}}\frac{V_{DD}}{\tau_f} \tag{6}$$

where τ_f is the output fall time. Notice that τ_f is a function of C_{Load}.

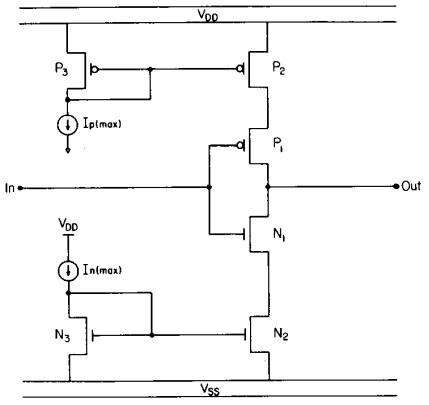

Fig. 4. Current controlled CMOS output driver.

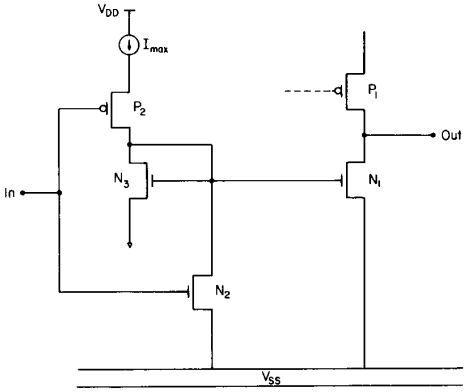

Fig. 5. Switching current controlled/unregulated CMOS output driver.

III. Current Controlled Output Drivers

The objective of a current controlled output driver is to control the maximum switching current $I_{\max}$ of the switching output. Here

$$I_{\max} = \max[I_T, I_D]. \tag{7}$$

It must be noted that controlling the switching current also limits the switching speed of the output driver. For example, if the maximum switching current is limited to $I_{\max}$, then for a given load capacitance C_{Load} the output switching transient is limited by

$$\tau = \frac{C_{\text{Load}} V_{DD}}{I_{\max}}. \tag{8}$$

For the current controlled output driver circuit shown in Fig. 4, the charging and discharging currents are limited by $I_P(\max)$ and $I_N(\max)$. Here $I_P(\max)$ and $I_N(\max)$ are realized using simple current mirrors [10]. From (8), the output driver rise/fall times are limited to,

$$\tau_r = \frac{C_{\text{Load}} V_{DD}}{I_P(\max)} \tag{9a}$$

and

$$\tau_f = \frac{C_{\text{Load}} V_{DD}}{I_N(\max)}. \tag{9b}$$

The increase in output transient time and the realization of a low V_{ol} (output low voltage) for a given I_{ol} (output sink current when $V_{\text{out}} = V_{ol}$) are major limitations in using current controlled output drivers. In addition, the switching speed of a fully current controlled output driver is always less than or equal to the switching speed of an equivalent current unregulated output driver. Simulations have demonstrated that the use of a current controlled output driver degrades the switching speed for clock frequencies of 30 MHz or greater [1].

To have both the current unregulated output driver (when switching current is lower than $I_{\max}$) for the slower switching conditions and the current controlled output driver (switching current is equal or greater than $I_{\max}$) for the faster switching conditions, a complimentary switch is designed. In Fig. 5, due to symmetry, only the sink portion of the current controlled output driver circuit with a complimentary switch is shown. The input signal to the output driver controls the switch to turn ON and OFF the unregulated ($P2, N3$, and $N1$ OFF) and the controlled ($P2, N3$, and $N1$ ON) switching current.

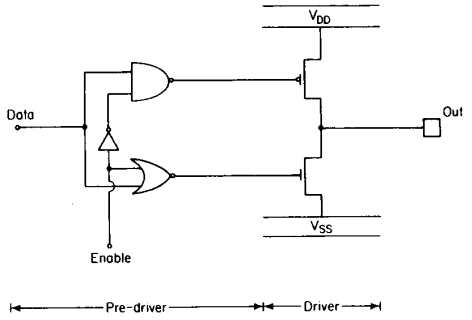

Fig. 6. A typical tri-statable (enable high) CMOS output driver.

IV. Controlled Slew Rate Output Drivers

The objective of a controlled slew rate output driver is to control the output driver's switching rise and fall times. To control the di/dt by controlled slew rate, the designer has to make sure the output driver design is not limited by the through current. This can be achieved by not connecting the gate terminals of the output stage P-channel and the N-channel transistors, and by making sure that there is a skew between the P-channel and the N-channel turning OFF/ON and ON/OFF times. In Fig. 6, a commonly used tri-statable (with enable high) CMOS output driver circuit is shown. In practice, the pre-driver V_{DD}/V_{SS} are connected to the internal (also called clean) V_{DD}/V_{SS} buses, and final stage output driver V_{DD}/V_{SS} buses are connected to external (also called noisy) V_{DD}/V_{SS} buses. This is because final stage driver device sizes (channel width) are very large compared to the internal, or even to the predriver, device sizes. Note that the increase in channel width increases the drive strength and also increases the switching noise.

However, increase in final stage output driver device sizes also increases the input capacitance of these devices. The

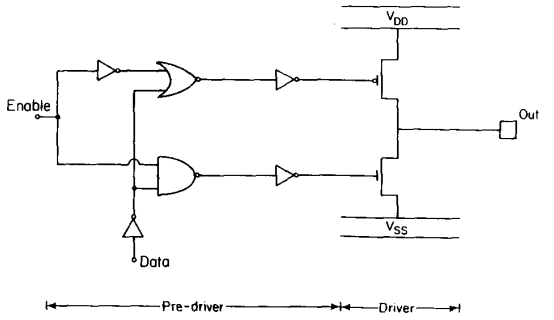

Fig. 7. High-speed, tri-statable (enable low) CMOS output driver.

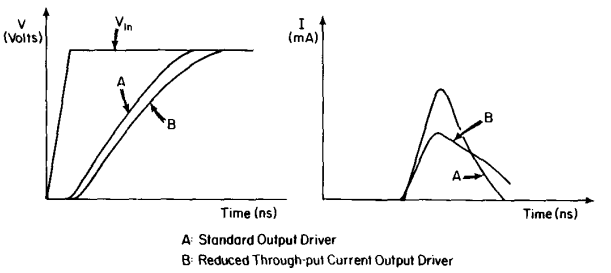

Fig. 8. Tri-State output driver switching characteristics.

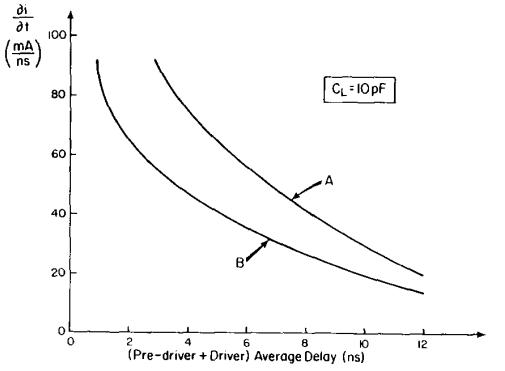

Fig. 9. Driver delay-switching noise limitations.

increase in input capacitance of the final stage may demand a larger drive strength predrivers compared to the internal gates drive strength to minimize the delay of the overall output driver [1]. Note that NAND, NOR, and other logic gates (except inverters and pass transistors) require larger silicon area with high input capacitance compared to a simple inverter to achieve a certain current drive. A high-speed, tri-statable (with enable low) CMOS output driver circuit utilizing the inverters for predrivers is shown in Fig. 7. The functionality of these tri-statable drivers shown in Figs. 6 and 7 are given in Tables I and II, respectively.

It is important to skew the arrival times of the input signals of the final stage to minimize the I_T of the output driver. This can be realized by selecting appropriate predriver device sizes. Skewing the switching time at the final P-channel and N-channel transistors gives rise to the overall delay. However, for high current drive output drivers, with a little trade-off in delay significant reduction in switching noise can be realized. In Fig. 9, a typical tri-statable output driver voltage and current switching characteristics are shown for a standard and reduced through current output drivers. Even with reduced through current output drivers, there is a delay-di/dt limitation. This is because increasing the final output driver device channel widths to reduce the overall delay increases the switching noise. In Fig. 8, the delay-di/dt curve for a 8-mA (D.C. sink for $V_{ol} = 0.4$ V) tri-statable output driver is shown. For a single driver, knowing the effective inductive L_{VSS} as seen by the output driver on its ground path, the delay-di/dt curve can be mapped to the delay-SSN limitation curve. Here the maximum SSN amplitude $V_1 = L_{VSS}\, di/dt$. Note that there is a switching noise pulse width associated with the maximum switching noise amplitude. Both the maximum switching noise amplitude and its associated pulse width have an impact on the dynamic noise immunity of input receivers, as well as in other internal circuits that are susceptible to false switching due to SSN feed through [7]. In practice, the delay-di/dt limitation can be a major limiting factor in a system design, especially when a large number of high current drive outputs switch simultaneously. It is important to control the maximum switching current $I_{\max}$, and also the time it takes for this current spike to reach its maximum value (T), to reduce the effective simultaneous switching noise.

In Fig. 10, a CSR tri-statable CMOS output driver circuit is shown. Functionality of this driver is given in Table I. These CSR output drivers were designed for the following drive strengths 1) PLIO (3.2 mA D.C. sink for $V_{ol} = 0.4$ V), 2) PLIO3 (8 mA D.C. sink for $V_{ol} = 0.4$ V), and 3) PLIO5 (12 mA D.C. sink for $V_{ol} = 0.4$ V). As shown in Fig. 11, in these CSR output driver designs, the final output stage of these drivers is split into several driver segments. It was found that when the current drive of the drivers increase, the number of optimal segments required to control effective di/dt also increases. Simulations have demonstrated that having more than three driver segments in the final stage is useful only when the output current drive is greater than 32 mA (D.C. sink for $V_{ol} = 0.4$ V) and driving a load capacitance of 25 pF or greater.

A final output driver using three driver segments (as shown in Fig. 10) was implemented in PLIO, PLIO3, and PLIO5 CSR output driver designs. The weighted ratio of 1:2:3 was selected for driver segment (1, 2, and 3) device sizes, respectively. For example, for a conventional PLIO5 driver, $W_P = 624\,\mu$m and $W_N = 414\,\mu$m, the following device sizes were selected for the CSR PLIO5 driver stages 1) $W_{P1} = 104\,\mu$m, $W_{N1} = 69\,\mu$m, 2) $W_{P2} = 208\,\mu$m, $W_{N2} = 138\,\mu$m, and 3) $W_{P3} = 312\,\mu$m, $W_{N3} = 207\,\mu$m. A similar weighting scheme (1:2:3) was used to calculate the device sizes of final stage output driver segments of the PLIO3 and the PLIO output drivers. Notice that the increase in driver device sizes increases the input capacitance, and this increases the delay time between each driver segment's switching time ΔT. For example, if an N- or P-channel transistor in driver stage number one switches at T_o (arbitrary time) time, then the second driver switches at $T_o + \Delta T_1$ time, and the final (or third) driver

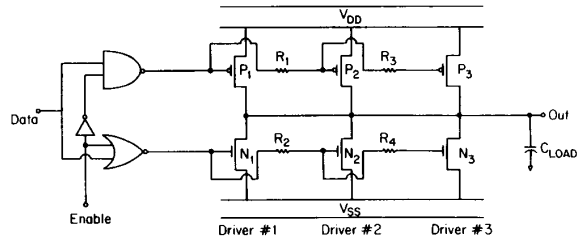

Fig. 10. Tri-statable, Controlled Slew Rate (CSR) output driver.

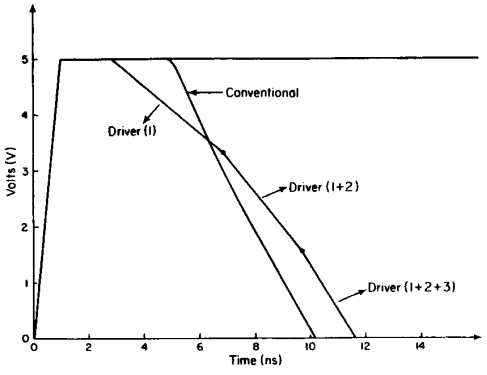

Fig. 11. CSR output driver voltage switching characteristics.

switches at $T_o + \Delta T_2$ time. In this design, all the P-channel and N-channel transistors in each driver segment are designed to minimize the through current on all driver segments. The input capacitance (C_I) of each stage is proportional to

$$C_I = kW_{\text{total}}C_{\text{unit}} \tag{10}$$

where W_{total} = total channel width, k = fringing factor, and C_{unit} = per-unit-length capacitance for a given CMOS technology (L_{eff} fixed). With the switching point centered around $V_{DD}/2$ and using delay estimations in RC tree networks, delays between output driver segments can be calculated [11].

$$\Delta T_1^N = \frac{1}{2}R_2(C_I^{N2} + C_I^{N3}) + \frac{1}{2}R_4C_I^{N3} \tag{11}$$

$$\Delta T_2^N = \frac{1}{2}R_4C_I^{N3} \tag{12}$$

$$\Delta T_1^P = \frac{1}{2}R_1(C_I^{P2} + C_I^{P3}) + \frac{1}{2}R_3C_I^{P3} \text{ and} \tag{13}$$

$$\Delta T_2^P = \frac{1}{2}R_3C_I^{P3} \tag{14}$$

where the superscripts on ΔT and C_I denote the P- or N-channel transistor.

The appropriate ΔT value can be realized by adjusting the driver segments device sizes (vary C_I) and/or changing the resistor (R_I) values. The selection criteria depend on the trade-offs between the driver delay and the simultaneous switching noise for a specific application. In this work, a

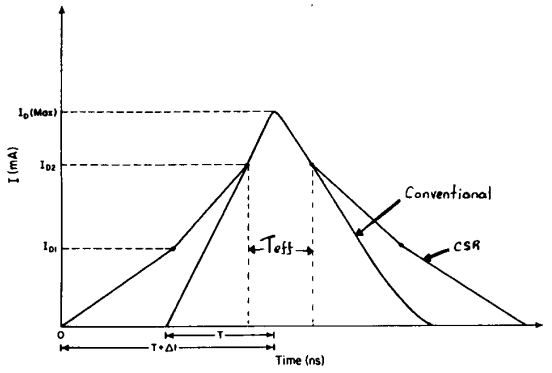

Fig. 12. CSR output driver current switching characteristics.

TABLE I
TRI- STATABLE (ENABLE HIGH) CMOS OUTPUT DRIVER (SEE FIG. 6)

Enable	Data	Out
1	x	Z
0	0	0
0	1	1

standard 1-kΩ resistance was used for all four resistors. Even though poly resistors (sheet) have little variation with process and temperature ($\approx 60 \pm 20\,\Omega$), diffusion resistors (sheet) ($\approx 130 \pm 35\,\Omega$) were used to save the silicon area. To control the slew rate by adjusting the ΔT, the ratio between resistors is important, and not the absolute value. These output driver (PLIO, PLIO3, and PLIO5) designs were implemented using standard cells (i.e., all the output drivers had some silicon area). The design of our biggest conventional PLIO5 output driver occupied $200\,\mu\text{m} \times 305\,\mu\text{m}$ silicon area (excluding bond-pad area). Within this output driver cell area, $200\,\mu\text{m} \times 120\,\mu\text{m}$ and $200\,\mu\text{m} \times 60\,\mu\text{m}$ were occupied by P- and N-channel transistors, respectively. Design of CSR output driver required an additional 40-μm silicon area for resistors (R_1, R_2, R_3, and R_4) realization. Implementation of a CSR PLIO5 output driver increased the output driver standard cell area to $200\,\mu\text{m} \times 330\,\mu\text{m}$. Notice that CSR output driver realization on silicon has increased the standard cell length by only $25\,\mu\text{m}$.

In Figs. 11 and 12 a typical CSR output driver voltage and current switching characteristics are compared with the conventional output drivers. As expected, including the additional resistors (R_1, R_2, R_3, and R_4) in the output driver design increases the driver delay for a given load capacitance. However, these delays are very small compared to the effective switching noise pulse width reduction. These CSR output drivers' performance-noise values are compared with the conventional output drivers, and the results are given in Table III. Note that even though there is not much reduction in the maximum peak switching noise amplitude, more than 50% reduction in the noise pulse width was realized using CSR output drivers. This is because the dynamic noise immunity study on the TTL-level compatible CMOS input receivers (the receivers used in conjunction with the output drivers) showed

TABLE II
HIGH DRIVE, TRI-STATABLE (ENABLE LOW) CMOS OUTPUT DRIVER (FIG. 7) x = DON 'T C ARE; Z = HIGH-IMPEDANCE OR HIGH-Z STATE

Enable	Data	Out
0	x	Z
1	0	0
1	1	1

that for a 2-ns noise pulse width the maximum tolerable switching noise amplitude is 1.2 V, whereas for a 0.8-ns noise pulse width the maximum tolerable switching noise amplitude is 2.6 V. From Table III it is clear that the use of CSR over conventional output drivers reduces the effective switching noise pulse width by 46%, 43%, and 60% for PLIO, PLIO3, and PLIO5 output drivers, respectively. This reduction in pulse width increases the maximum tolerable switching noise amplitude by more than two times (more than 50% improvement). The impact of having increased maximum allowable SSN has a two-fold advantage in a system design: 1) Designers can switch more CSR output drivers simultaneously compared to the conventional output drivers for a noise-limited system design, or 2) for a given number of bits switching simultaneously in a not-noise-limited system design, the use of CSR over conventional output drivers will permit designers to reduce the number of V_{DD}/V_{SS} bond-pad/package-pin connections required for the output drivers. These connections are also known as external, or dirty, V_{DD}/V_{SS} connections. The reduction in number of bond-pads/package-pins for output driver V_{DD}/V_{SS} connections may permit the system designer to place the die in a smaller package (reduce I/O count). Placing a die in a smaller package often reduces the cost of the product in a single-chip packaged product.

V. SUMMARY

Detailed investigations on the CMOS output switching current components and their impact on the simultaneous switching noise were performed. Current controlled output driver circuit design technique and its capabilities and limitations are explained. Controlled slew rate output driver design technique and methods of realizing skewing times between driver segments are given. The advantage in using controlled slew rate output drivers over the conventional output drivers to minimize the effective simultaneous switching noise was demonstrated.

TABLE III
PERFORMANCE-SSN COMPARISON OF CONVENTIONAL AND CSR OUTPUT DRIVERS

Driver Type	Performance-Noise	Conventional Driver	CSR Driver
PLIO	Delay [1h + h1]/2 (ns)	9.6	10.3
"	Sink/Source (mA)	3.5	3.4
"	Noise Pulse Amp. (mV)	430	424
"	Noise Pulse Width (ns)	1.3	0.7
PLIO3	Delay [1h + h1]/2 (ns)	7.5	7.8
"	Sink/Source (mA)	9.2	8.3
"	Noise Pulse Amp. (mV)	655	637
"	Noise Pulse Width (ns)	1.6	0.9
PLIO5	Delay [1h + h1]/2 (ns)	4.9	5.1
"	Sink/Source (mA)	12.5	12.1
"	Noise Pulse Amp. (mV)	800	741
"	Noise Pulse Width (ns)	2.0	0.8

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