A Bipolar Four-Quadrant Analog Quarter-Square Multiplier Consisting of Unbalanced Emitter-Coupled Pairs and Expansions of Its Input Ranges

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***Abstract*—A bipolar four-quadrant analog multiplier based on the quarter-square technique, which is constituted from unbalanced emitter-coupled pairs, and some methods for extending the input voltage range, are described. The building blocks for the circuit consist of an unbalanced emitter-coupled pair with different emitter areas, an emitter-coupled pair with an input bias offset, and an unbalanced emitter-coupled pair with unbalanced emitter degeneration. A basic squaring circuit is realized from two identical unbalanced emitter-coupled pairs with emitter area ratio *K* and cross-coupled inputs and parallel-connected outputs. The quarter-square multipliers proposed in this paper can operate under low supply voltage (typically <3 V, and a minimum of 1 V). Therefore, the Gilbert multiplier, which has been the most popular analog multiplier in bipolar technology over the past few decades, can be replaced.**

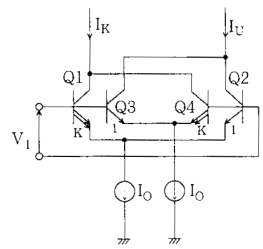

Fig. 1. A basic squaring circuit consisted of two identical unbalanced emitter-coupled pairs with emitter area ratio K.

I. Introduction

In this decade, portable equipment, such as mobile telephones, hand held movie cameras, cassette players, radio receivers, have become widely available and increasingly smaller and lighter. These equipment typically operate on low supply voltage achieved though the usage of LSI/VLSI chips. Nowadays, supply voltages for equipments like mobile telephones, hand held movie cameras, and cordless telephones are in the 2–3 volt range. Although the Gilbert multiplier [1], [2] has been the most popular bipolar multiplier used in multiplication circuitries, it requires a supply voltage of more than 3 V. Therefore, a new bipolar four-quadrant analog multiplier which can operate at less than 3 V is highly desirable.

In 1993, the author proposed the unified circuit theory on low voltage four-quadrant analog multipliers [3]. In this paper, the author demonstrates multiplication characteristics for a bipolar quarter-square multiplier based on the emitter area ratio unbalance technique [3] and discusses some methods of extending the linear input range for the quarter-square multiplier.

II. Squaring Circuit Consisted of Two Identical Unbalanced Emitter-Coupled Pairs

Fig. 1 shows a basic squaring circuit consisted of two identical unbalanced emitter-coupled pairs with emitter area ratio K and cross-coupled inputs and parallel-connected outputs. Assuming matched devices and ignoring basewidth modulation, the differential output current, ΔI_{C1}, for the first unbalanced emitter-coupled pair with emitter area ratio K is [4].

$$\Delta I_{C1} = I_{C1} - I_{C2} = \alpha_F I_0 \tanh\left(\frac{V_1 + V_K}{2V_T}\right) \tag{1}$$

where $V_T = kT/q$ is the thermal voltage, k is Boltzmann's constant, T is absolute temperature in degrees Kelvin, q is magnitude of the electron charge, parameter α_F is the dc common-base current gain, I_0 is a current sink, V_1 is the input voltage, and V_K is the offset voltage defined as $V_K = V_T \ln K$.

The differential output current ΔI_1 for a basic squaring circuit is [4]

$$\begin{aligned}\Delta I_1 &= I_K - I_U = (I_{C1} + I_{C4}) - (I_{C2} + I_{C3})\\ &= (I_{C1} - I_{C2}) + (I_{C4} - I_{C3})\\ &= \Delta I_{C1} + \Delta I_{C2}\\ &= \alpha_F I_0 \left\{\tanh\left(\frac{V_1 + V_K}{2V_T}\right) - \tanh\left(\frac{V_1 - V_K}{2V_T}\right)\right\}.\end{aligned} \tag{2}$$

Collector currents, I_K and I_U, versus input voltage are shown in Fig. 2 for various values of K.

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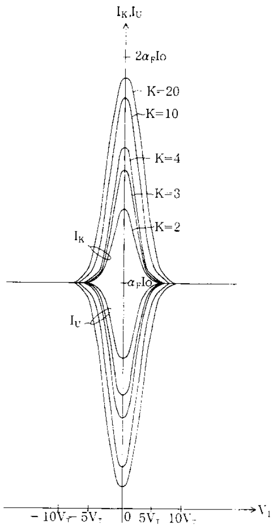


Fig. 2. DC transfer curves of a basic squaring circuit consisted of two identical unbalanced emitter-coupled pairs with emitter area ratio K.

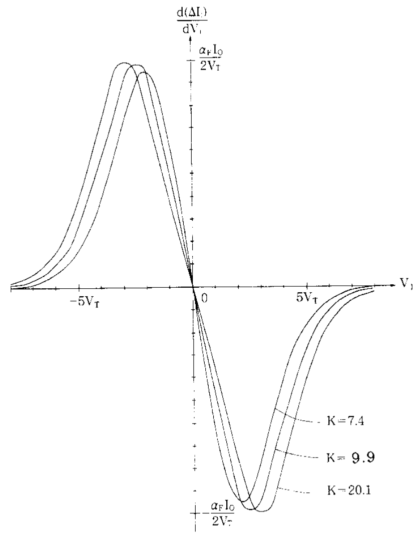


Fig. 3. Transconductance of a basic squaring circuit consisted of two identical unbalanced emitter-coupled pairs with emitter area ratio K.

For $|x| \ll 1$, $\tanh x = x - x^3/3$, then (2) becomes

$$\begin{aligned}\Delta I_1 &= \alpha_F I_0 \left\{ \frac{V_K}{V_T} - \frac{V_K}{4V_T^3} V_1^2 - \frac{2}{3}\left(\frac{V_K}{2V_T}\right)^3 \cdots \right\} \\ &= \alpha_F I_0 \ln K \left\{ 1 - \frac{1}{4V_T^2} V_1^2 - \frac{1}{12}(\ln K)^2 \right\} \cdots . \end{aligned} \tag{3}$$

The differential output current, ΔI_1, includes a component that is proportional to the square of the differential input voltage, V_1. Therefore, two identical unbalanced emitter-coupled pairs with cross-coupled inputs and parallel-connected outputs, as shown in Fig. 1, can be used as a squaring circuit for quarter-square multiplier.

Taking the derivatives of (2), the transconductance for the basic squaring circuit consisted of two identical unbalanced emitter-coupled pairs with emitter area ratio K is expressed as

$$\frac{d(\Delta I_1)}{dV_1} = \frac{\alpha_F I_0}{2V_T} \left\{ \operatorname{sech}^2\left(\frac{V_1 + V_K}{2V_T}\right) - \operatorname{sech}^2\left(\frac{V_1 - V_K}{2V_T}\right) \right\}. \tag{4}$$

Fig. 3 shows the transconductance characteristics for the basic squaring circuit with parameter K. An ideal squaring circuit should yield a linear derivative.

The optimum value of V_K which will yield a linear derivative over the widest input voltage range is about 2.29 V_T (i.e., the optimum K value is about 9.9). If K is less than 9.9, the input voltage range for the basic squaring circuit with a linear transconductance becomes narrower. If K is greater than 9.9, a cross-over distortion from transconductances of the two unbalanced emitter-coupled pairs appears. An input voltage range with almost linear transconductance for the basic squaring circuit is obtained for $-2V_T < V_K < 2V_T$.

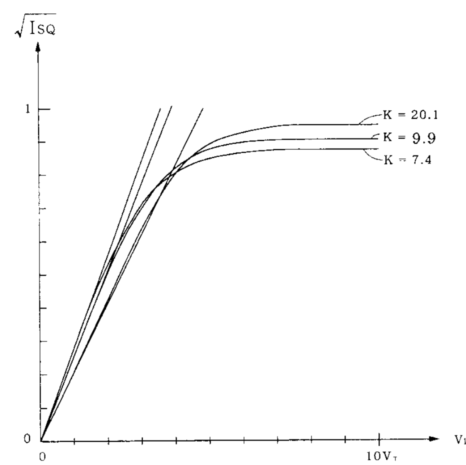


Fig. 4. Relationship between the square-root of the differential output current of a basic squaring circuit consisted of two identical unbalanced emitter-coupled pairs with emitter area ratio K and the differential input voltage V_1.

The square-law relationship between the drain current and the gate-to-source voltage for an MOS field-effect transistor (MOSFET) is usually evaluated by plotting as the square-root of the drain current versus the gate-to-source voltage.

Here

$$I_{SQ} = \frac{\Delta I_1|_{V1=0} - \Delta I_1}{2\alpha_F I_0}. \tag{5}$$

Fig. 4 shows the square-root of the differential output current for the basic squaring circuit versus the differential input voltage calculated using (5). An ideal squaring circuit should yield a linear line.

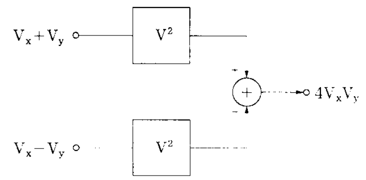


Fig. 5. A quarter-square multiplier block diagram showing cross-coupled outputs of two identical squaring circuits.

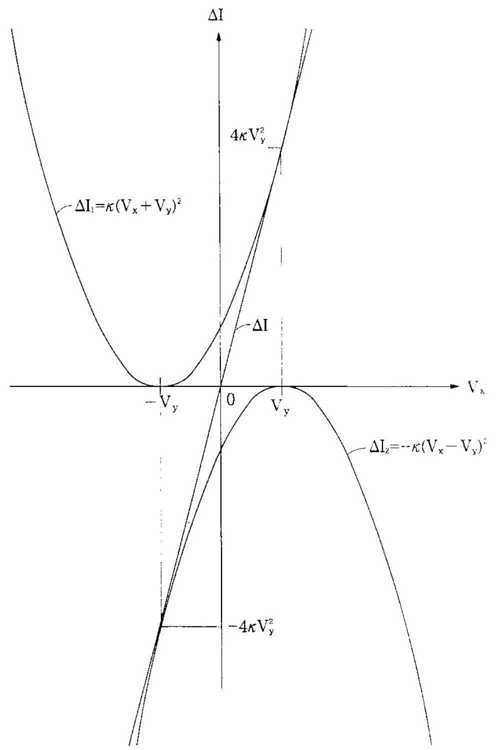


Fig. 6. A graphical illustration of linear behavior for a four-quadrant analog multiplier based on the quarter-square technique.

III. Composition of Quarter-Square Multiplier

A quarter-square multiplier can be constructed from two squaring circuits, as shown in Fig. 5, by cross-coupling their output terminals. Fig. 6 illustrates the linear behavior of the quarter-square multiplier. The multiplication method is based on the identity

$$\begin{aligned} \Delta I &= I_P - I_q = \kappa(V_x + V_y)^2 - \kappa(V_x - V_y)^2 \\ &= 4\kappa V_x V_y \end{aligned} \tag{6}$$

where κ is a transconductance constant. Multiplication error arises only from the difference between the transfer curves of the two squaring circuits and the parabolic function.

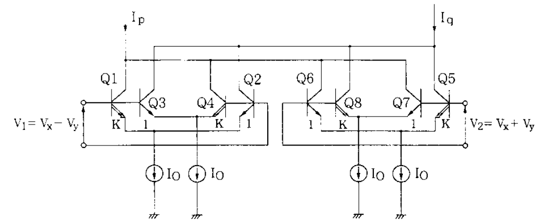


Fig. 7. A basic quarter-square multiplier consisted of four identical unbalanced emitter-coupled pairs with emitter area ratio K.

The differential output current, ΔI, for the basic quarter-square multiplier shown in Fig. 7, is

$$\begin{aligned} \Delta I &= I_p - I_q = \Delta I_1 - \Delta I_2 \\ &= \alpha_F I_0 \left[\left\{ \tanh\left(\frac{V_1 + V_K}{2V_T}\right) - \tanh\left(\frac{V_1 - V_K}{2V_T}\right) \right\} \right. \\ &\quad \left. - \left\{ \tanh\left(\frac{V_2 + V_K}{2V_T}\right) - \tanh\left(\frac{V_2 - V_K}{2V_T}\right) \right\} \right] \end{aligned} \tag{7}$$

and the second-order approximation of (7) is

$$\Delta I \fallingdotseq -\frac{\alpha_F I_0 \ln K}{4V_T^2}(V_1^2 - V_2^2) \tag{8}$$

where

$$V_1 = V_x - V_y \tag{9a}$$

$$V_2 = V_x + V_y. \tag{9b}$$

Substituting (9) into (7),

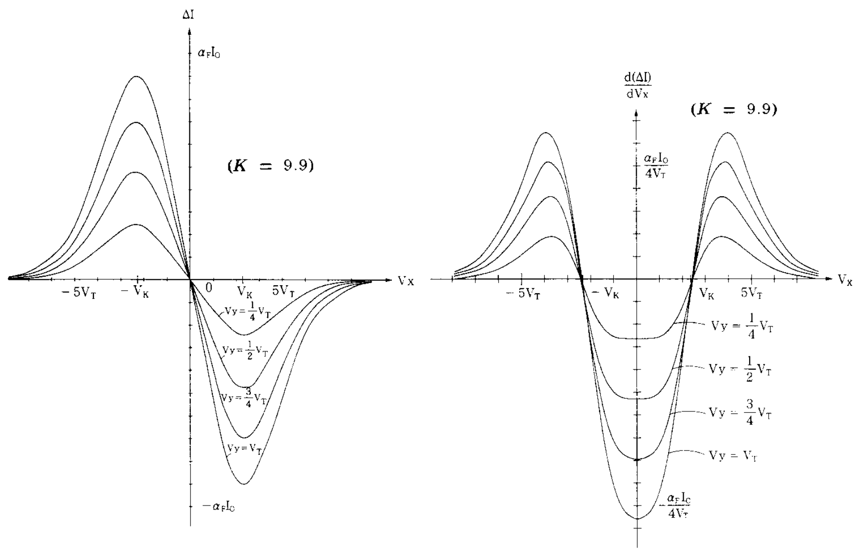
$$\begin{aligned} \Delta I &= \alpha_F I_0 \left[\tanh\left\{\frac{V_x - (V_y - V_K)}{2V_T}\right\} \right. \\ &\quad + \tanh\left\{\frac{V_x + (V_y - V_K)}{2V_T}\right\} \\ &\quad - \tanh\left\{\frac{V_x - (V_y + V_K)}{2V_T}\right\} \\ &\quad \left. - \tanh\left\{\frac{V_x + (V_y + V_K)}{2V_T}\right\} \right] \end{aligned} \tag{10}$$

and substituting (9) into (8), the second-order approximation is

$$\Delta I \fallingdotseq \alpha_F I_0 \frac{\ln K}{V_T^2} V_x V_y. \tag{11}$$

The result is a differential output current expressed in terms of the first input voltage V_x and the second input voltage V_y. Equation (11) represents the approximated differential output current of a quarter-square multiplier described in this paper.

The approximated differential output current for a Gilbert multiplier is given by $\Delta I \fallingdotseq \{\alpha_F^2 I_0/(4V_T^2)\}V_x V_y$. Since the fractional temperature coefficient is 3,333 ppm/°C for V_T and is less than 100 ppm/°C for α_F, α_F is usually neglected in approximation analysis. Thus, differential current is approximated by $\Delta I \fallingdotseq \{I_0/(4V_T^2)\}V_x V_y$ for the Gilbert multiplier and by $\Delta I \fallingdotseq \{(\ln K)I_0/(V_T^2)\}V_x V_y$ for the basic quarter-square multiplier based on the emitter area ratio unbalance technique [3].



(a) (b)

Fig. 8. DC characteristics of a basic quarter-square multiplier. (a) Transfer curves for four values of V_y. (b) Transconductance characteristics for four values of V_y.

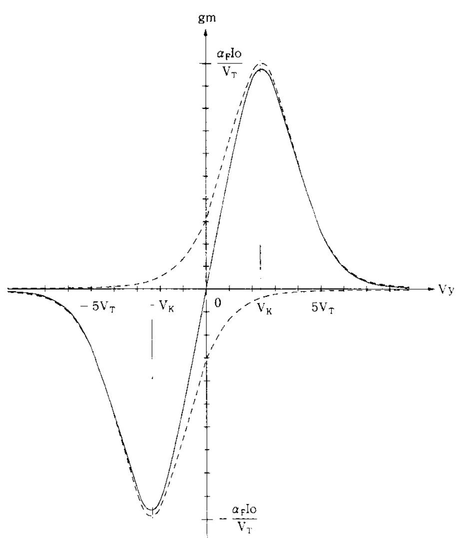
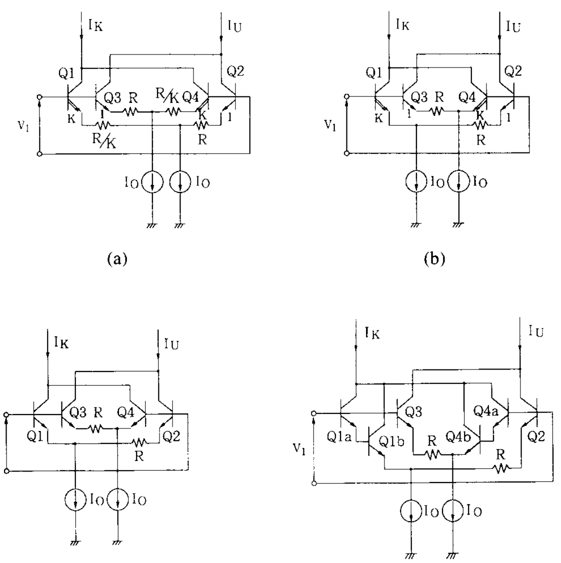


Fig. 9. Short-circuit transconductance of a basic quarter-square multiplier.



(c) (d)

Fig. 10. Squaring circuits consisting of unbalanced emitter-coupled pairs with unbalanced emitter degeneration. (a) Transistor-pair with emitter area ratio K and degeneration resistor ratio $1/K$. (b) Transistor-pair with emitter area ratio K and an emitter resistor. (c) Transistor-pair with one side emitter resistor. (d) Transistor-pair of a Darlington-pair and a transistor with an emitter resistor.

Taking the derivatives of (10), the transconductance for the basic quarter-square multiplier is

$$\frac{d(\Delta I)}{dV_x} = \frac{\alpha_F I_0}{2V_T}\left[\operatorname{sech}^2\left\{\frac{V_x-(V_y-V_K)}{2V_T}\right\} + \operatorname{sech}^2\left\{\frac{V_x+(V_y-V_K)}{2V_T}\right\} - \operatorname{sech}^2\left\{\frac{V_x-(V_y+V_K)}{2V_T}\right\} - \operatorname{sech}^2\left\{\frac{V_x+(V_y+V_K)}{2V_T}\right\}\right]. \quad (12)$$

Fig. 8(a) shows the dc transfer characteristics of a basic quarter-square multiplier, calculated using (10) with second input voltage V_y as a parameter. Workable input voltage range for a bipolar multiplier is about $\pm 2V_T$, as shown in Fig. 8(a).

Fig. 8(b) shows the transconductance characteristics of a basic quarter-square multiplier calculated using (12) with parameter V_y. Linear input voltage range is very narrow, as shown in Fig. 8(b).

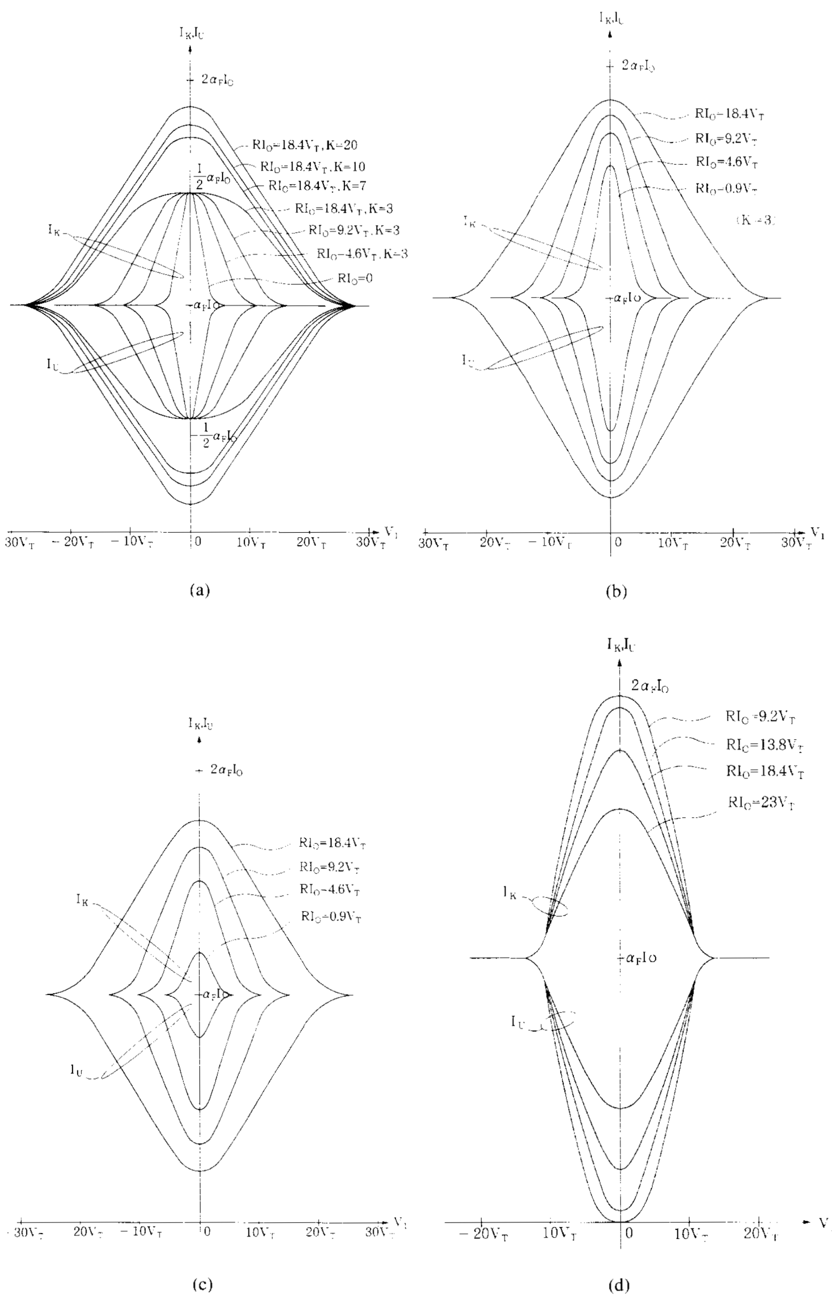


Fig. 11. SPICE simulations of the squaring circuits consisted of unbalanced emitter-coupled pairs for various values of RI_0. (a) Transistor-pair with emitter area ratio $K = 3$ and the degeneration resistor ratio $1/K = 1/3$. (b) Transistor-pair with emitter area ratio $K = 3$ and an emitter resistor. (c) Transistor-pair with one side emitter resistor. (d) Transistor-pair of a Darlington-pair and a transistor with an emitter resistor.

The short-circuit transconductance of a basic quarter-square multiplier is

$$gm(V_y) = \left.\frac{d(\Delta I)}{dV_x}\right|_{V_x=0} = \frac{\alpha_F I_0}{V_T}\left\{\operatorname{sech}^2\left(\frac{V_y - V_K}{2V_T}\right) - \operatorname{sech}^2\left(\frac{V_y + V_K}{2V_T}\right)\right\}. \quad (13)$$

Fig. 9 shows the short-circuit transconductance of a basic quarter-square multiplier as a monotonically increasing function over the second input voltage range as large as $\pm V_K$. The optimum value of V_K is also determined from Fig. 9 to be about 2.29 V_T (i.e., the optimum value of K is about 9.9). The peak value of the transconductance is $0.960\{\alpha_F I_0/V_T\}$ when K is 9.9.

Taking notice of each differential pair in this circuitry, the input terminals are connected to the base of a unit transistor

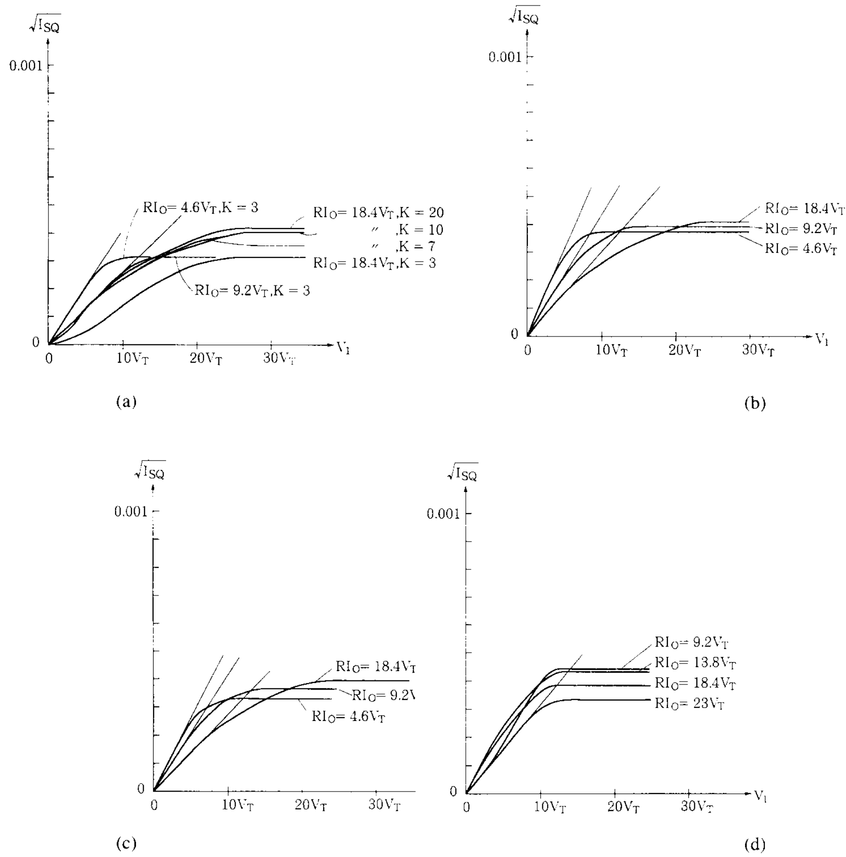


Fig. 12. Relationship between the square root of the differential output current of the squaring circuit consisted of two identical unbalanced emitter-coupled pairs with unbalanced emitter degeneration and the differential input voltage V_1. (a) Transistor-pair with emitter area ratio K and the degeneration resistor ratio $1/K$. (b) Transistor-pair with emitter area ratio $K = 3$ and an emitter resistor. (c) Transistor-pair with one side emitter resistor. (d) Transistor-pair of a Darlington-pair and a transistor with an emitter resistor.

with unit emitter area and to the base of a K-ratioed transistor with K times emitter area and the output terminals are also connected to collectors of two unit transistors and collectors of two K-ratioed transistors. Therefore, each pair of differential input terminals and differential output terminals is balanced in itself. It is similar to a "multi-tanh" doublet consisting of two identical unbalanced emitter-coupled pairs with emitter area ratio $K = 2 + \sqrt{3}$ and cross-coupled input and output stages.

Based on existing research [5], this basic quarter-square multiplier shown in Fig. 7 should be operational at 1 V power supply.

IV. Squaring Circuit Consisted of Two Identical Unbalanced Emitter-Coupled Pairs with Unbalanced Emitter Degeneration

Squaring circuits can also be built from unbalanced emitter-coupled pairs with unbalanced emitter degeneration and are similar to the circuit using unbalanced emitter-coupled pair with emitter area ratio K, as shown in Fig. 1. Unlike the unbalanced emitter-coupled pair with emitter area ratio K, however, the unbalanced emitter-coupled pairs with unbalanced emitter degeneration is not analytical and is therefore difficult to analyze with hand calculations.

Fig. 10 shows four squaring circuits consisting of two unbalanced transistor-pairs with unbalanced emitter degeneration. A squaring circuit consisted of two unbalanced emitter-coupled pairs with emitter area ratio K and emitter degeneration resistor ratio $1/K$ is shown in Fig. 10(a). This circuit has been introduced as a full-wave rectifier [4] by the author. A squaring circuit consisted of two unbalanced emitter-coupled pairs with emitter area ratio K and an emitter resistor is shown in Fig. 10(b). A squaring circuit consisted of two unbalanced emitter-coupled pairs with one side emitter resistor is shown in Fig. 10(c). A squaring circuit consisted of two unbalanced emitter-coupled pairs of a Darlington-pair and a transistor with an emitter resistor is shown in Fig. 10(d).

Unbalanced transistor-pairs have input offset voltages resulted from the unbalance in emitter area and emitter degeneration. Input dynamic ranges of squaring circuits from such unbalanced transistor-pairs are limited within these input offset voltages. Although squaring circuits shown in Figs. 10(a) and 10(b) have two parameters, emitter area ratio (K) and emitter degeneration (RI_0), squaring circuits shown in Figs. 10(c) and

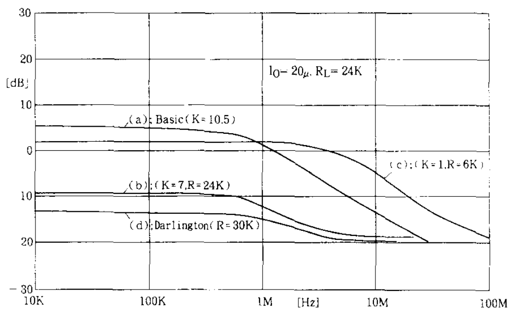


Fig. 13. Frequency characteristics of the quarter-square multipliers simulated with SPICE.

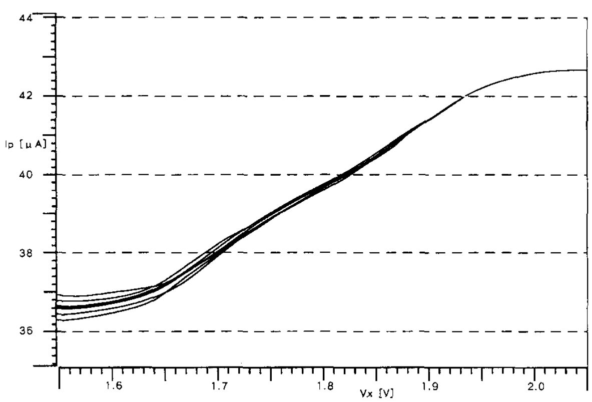


Fig. 14. Device mismatch effects on the quarter-square multiplier simulated with SPICE.

(d) have only one parameter, emitter degeneration (RI_0). A squaring characteristic can be estimated by differentiation as above mentioned. Another method of estimating the characteristics of a squaring circuit is to plot the relationship between square-root of the output current and the input voltage. Plot of square-root of current with an ideal square-law characteristic will appear linear.

V. Computer Simulation

A. Squaring Circuits

Circuit performances for emitter-coupled pairs with emitter degeneration are simulated using SPICE.

Fig. 11 shows the SPICE simulations for the four squaring circuits shown in Fig. 10 and for different values of RI_0 (product of an emitter-degeneration resistance R and a current source I_0) or K, where I_0 is taken to be $20\,\mu$A and α_F is taken to be 0.99 [6]. DC transfer characteristics for each of the two identical unbalanced emitter-coupled pairs with unbalanced emitter degeneration and cross-coupled inputs and parallel-connected outputs, as shown in Fig. 10, can approximate the square characteristic, similar to the unbalanced emitter-coupled pairs with emitter area ratio K, as shown in Fig. 1.

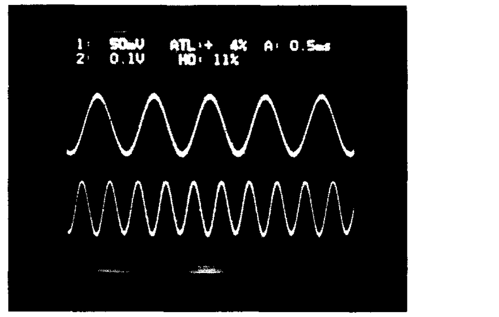


Fig. 15. Input and output waveforms of the basic squaring circuit. (Upper: input waveform, Lower: output waveform).

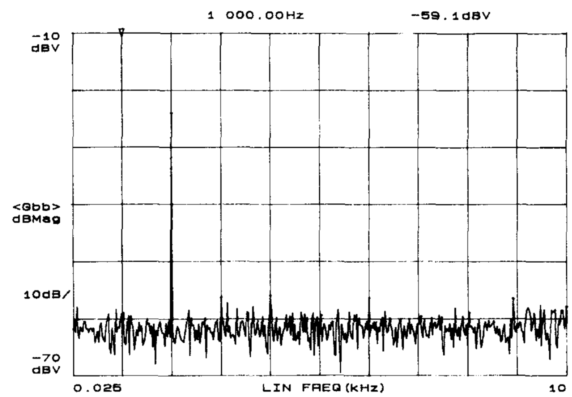


Fig. 16. Output spectrum of the basic squaring circuit.

Fig. 12 shows the square-root characteristics of differential output current for the squaring circuits in Fig. 10. The input range for the squaring circuit shown in Fig. 10(c) can be extended to about $\pm 5V_T$ when RI_0 is $4.6V_T$, to about $\pm 5.4V_T$ when RI_0 is $9.2V_T$, and allowing for a little ripple to about $\pm 8.5V_T$ when RI_0 is $18.4V_T$. Therefore, the optimal emitter degeneration for this circuit [Fig. 10(c)] is about $4.6V_T$. The same analysis can be applied to the squaring circuit shown in Fig. 10(b). Since the offset voltage component from unbalanced emitter area is much smaller than the offset voltage component from unbalanced emitter degeneration, the optimal emitter degeneration for the circuit shown in Fig. 10(b) is about $4V_T$. An input voltage which cuts off a transistor without an emitter resistor in an unbalanced emitter-coupled pair with one side emitter degeneration is ($V_T \ln K - 2V_T - v$) where v is about $3V_T$. Therefore, the input range for a squaring circuit consisted of two identical unbalanced emitter-coupled pairs with one side emitter degeneration can be extended to about $(5 - \ln K)V_T$. This squaring circuit has very limited linear input range compared with others because an unbalanced emitter area ratio of K reduces the linear input range by a factor $\ln K$.

Finally, input range for the circuit shown in Fig. 10(d) can be successfully extended to $\pm 9.6V_T$ if emitter degeneration is adequately set at $23V_T$. Input dynamic range for this circuit is $(VBE_{(\text{sat})} + 2V_T)$ for $(VBE_{(\text{sat})} + 2V_T) > RI_0$.

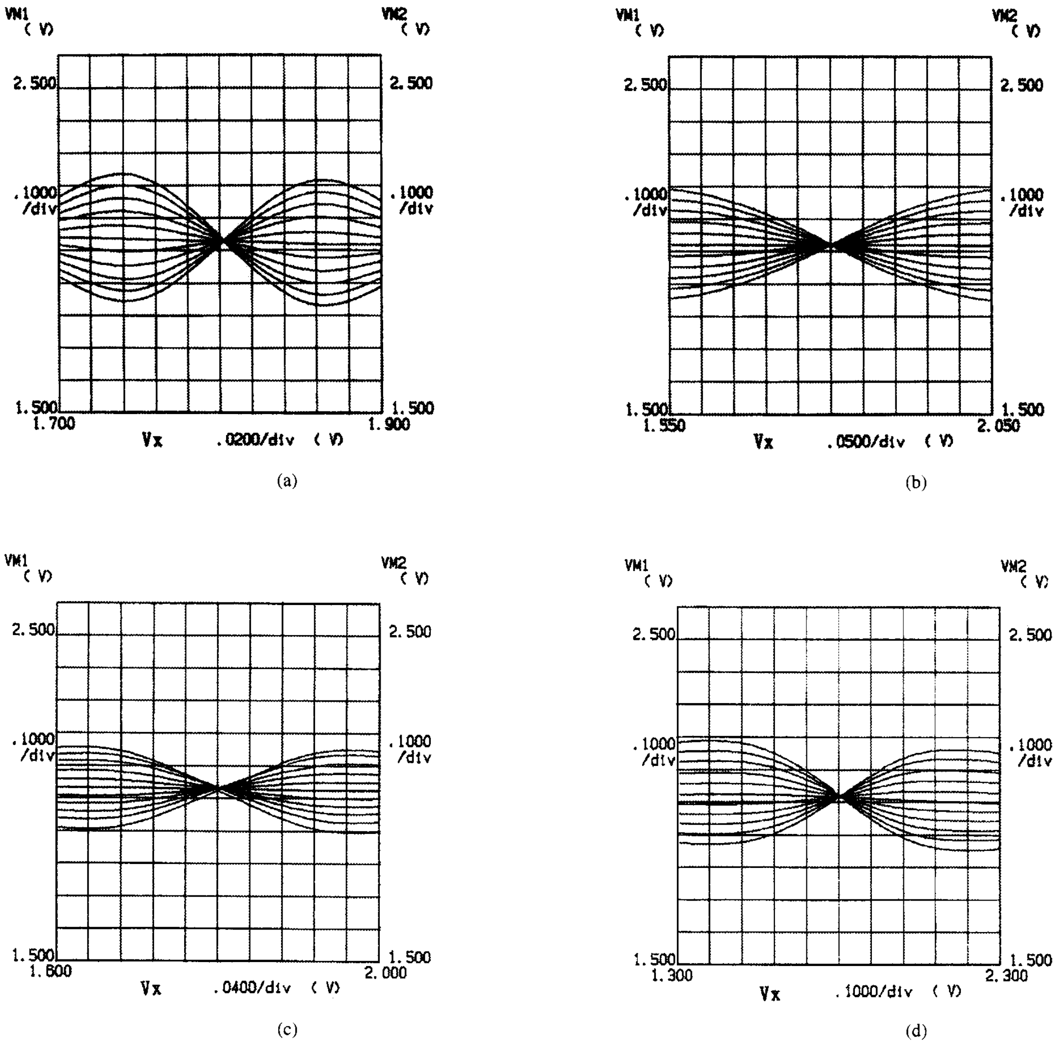


Fig. 17. Measured dc transfer characteristics of the quarter-square multipliers consisted of two identical squaring circuits (a) Shown in Fig. 1, with parameter V_y; 0 mV, ±10 mV, ±20 mV, ±30 mV, ±40 mV, ±50 mV, when K is 10. (b) Shown in Fig. 10(a), with parameter V_y; 0 mV, ±50 mV, ±100 mV, ±150 mV, ±200 mV, ±250 mV, when K is 7 and RI_0 is about $18.4V_T$. (c) Shown in Fig. 10(c), with parameter V_y; 0 mV, ±20 mV, ±40 mV, ±60 mV, ±80 mV, ±100 mV, when RI_0 is about $4.6V_T$. (d) Shown in Fig. 10(d), with parameter V_y; 0 mV, ±50 mV, ±100 mV, ±150 mV, ±200 mV, ±250 mV, when RI_0 is about $23V_T$.

The input range for the circuit shown in Fig. 12(a) can be extended by applying adequate unbalanced emitter degeneration according to K value. For example, the input range is extended to $\pm 6V_T$ when $RI_0 = 4.6V_T$ and $K = 3$, or $\pm 9V_T$ when $RI_0 = 18.4V_T$ and $K = 7$.

B. Quarter-Square Multipliers

Frequency characteristics for the quarter-square multipliers are simulated using SPICE since hardware simulations using breadboards are imprecise at high frequency due to wire stray capacitances. Fig. 13 shows the frequency characteristics of quarter-square multiplier circuits shown in Figs. 1, 10(a), 10(c), and 10(d), with parameter $V_y = 20$ mV, $V_y = 100$ mV, $V_y = 60$ mV, and $V_y = 100$ mV.

These quarter-square multipliers can be used in low frequency (<1 MHz) application at a 0.24 mW low power consumption and can be used in high frequency (>1 MHz) and low supply voltage (<3 V) applications by increasing power consumption.

The effects of device mismatch were evaluated by SPICE simulation. Fig. 14 shows the SPICE simulations for the quarter-square multiplier consisted of two identical squaring circuits shown in Fig. 10(a) and based on the assumption that the mismatch between the two pairs do not exceed ±5% of each other. In a quarter-square multiplier, device mismatch effects the input or output offset voltage, asymmetry and linearity of the transfer curve.

VI. Experimental Results

A basic squaring circuit consisted of two identical unbalanced emitter-coupled pairs with emitter area ratio $K = 10$, as shown in Fig. 1, is demonstrated by using transister-

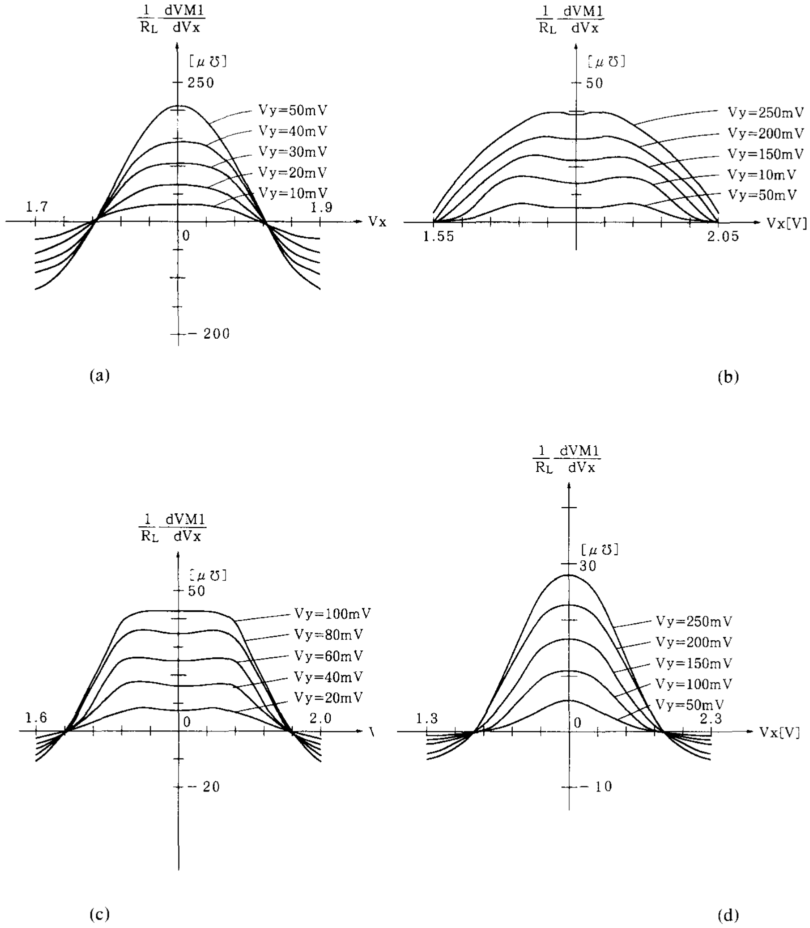


Fig. 18. Transconductance characteristic calculations for the quarter-square multipliers consisted of two identical squaring circuits using measured values shown in Fig. 17. (a) Shown in Fig. 1, with parameter V_y; 10 mV, 20 mV, 30 mV, 40 mV, 50 mV. (b) Shown in Fig. 10(a), with parameter V_y; 50 mV, 100 mV, 150 mV, 200 mV, 250 mV. (c) Shown in Fig. 10(c), with parameter V_y; 20 mV, 40 mV, 60 mV, 80 mV, 100 mV. (d) Shown in Fig. 10(d), with parameter V_y; 50 mV, 100 mV, 150 mV, 200 mV, 250 mV.

arrays [6]. Fig. 15 shows the input and output waveforms for the basic squaring circuit. The input is a 100 mV_{PP}, 1 kHz signal. The resulting output frequency spectrum is shown in Fig. 16. The fundamental frequency (1 kHz) is -59.1 dB_v, second harmonic frequency (2 kHz) is -23.9 dB_v, third harmonic frequency (3 kHz) is -56.2 dB_v, and fourth harmonic frequency (4 kHz) is -55.9 dB_v, etc. The fundamental and other harmonic frequency is suppressed to more than 32.0 dB, compared with second harmonic frequency (2 kHz).

Fundamental dc operations of the quarter-square multipliers are demonstrated with unbalanced emitter-coupled pairs by using transister-arrays [6] and resistors. Fig. 17 shows dc transfer characteristics for the quarter-square multipliers where $VM1 = R_L I_P, VM2 = R_L I_q$ and $R_L = 24K\Omega$. Fig. 17(a) shows dc transfer characteristics for the basic quarter-square multiplier shown in Fig. 7, with V_y of 0 mV, ±10 mV, ±20 mV, ±30 mV, ±40 mV, ±50 mV and K of 10. Fig. 17(b) shows dc transfer characteristics for the quarter-square multiplier consisted of two identical squaring circuits shown in Fig. 10(a), with V_y of 0 mV, ±50 mV, ±100 mV, ±150 mV, ±200 mV, ±250 mV, K of 7 and RI_0 of about $18.4V_T$. Fig. 17(c) shows dc transfer characteristics for the quarter-square multiplier consisted of two identical squaring circuits shown in Fig. 10(c), with V_y of 0 mV, ±20 mV, ±40 mV, ±60 mV, ±80 mV ±100 mV and RI_0 of about $4.6V_T$. Fig. 17(c) shows dc transfer characteristics for the quarter-square multiplier consisted of two identical squaring circuits shown in Fig. 10(d), with V_y of 0 mV, ±50 mV, ±100 mV, ±150 mV, ±200 mV, ±250 mV and RI_0 of about $23V_T$. Linear input ranges were successfully extended to as large as 200 mV.

Fig. 18 shows transconductance characteristic calculations for these quarter-square multipliers using measured values shown in Fig. 17. Fig. 18(a) shows transconductance characteristic calculations for the basic quarter-square multiplier with V_y of 10 mV, 20 mV, 30 mV, 40 mV, 50 mV. Fig. 18(b) shows transconductance characteristic calculations for the quarter-square multiplier consisted of two identical squaring circuits shown in Fig. 10(a) with V_y of 50 mV, 100 mV, 150 mV, 200 mV, 250 mV. Fig. 18(c) shows transconductance characteristic calculations for the quarter-square multiplier consisted of two identical squaring circuits shown in Fig. 10(c) with V_y of 20 mV, 40 mV, 60 mV, 80 mV, 100 mV. Fig. 18(c) shows transconductance characteristic calculations for the quarter-square multiplier consisted of two identical squaring circuits shown in Fig. 10(d) with V_y of 50 mV, 100 mV, 150 mV, 200 mV, 250 mV.

VII. Conclusion

A bipolar four-quadrant analog quarter-square multiplier which can be operated at low supply voltage was realized. Fundamental multiplication characteristics, such as linearity, are evaluated by test circuits and frequency characteristics and device mismatch effects are simulated with SPICE.

The input range for a squaring circuit can be extended by applying unbalanced emitter degeneration to the emitter-coupled pair. Therefore, the linear input ranges for the quarter-square multiplier can be successfully extended by using transistor-pairs consisted of a unit transistor with an emitter resistor and a K-ratioed transistor with a $1/K$-valued emitter resistor, or a Darlington–pair and a transistor with a series connected emitter resistor.

In this paper, the unbalanced emitter degeneration technique for a squaring circuit is proposed and demonstrated using breadboards.

Because matching devices are critical to the realization of superior multiplication characteristics, the multipliers discussed in this paper are implemented in bipolar IC technology.

Although a multiplier consisted of a Darlington–pair and a transistor with a series connected emitter resistor requires a higher V_{supply} (one V_{BE}, or about 0.6 V) than the supply voltage for a basic multiplier, it is particularly well suited for low-voltage applications, such as AGC amplifiers, frequency mixers, modulators, and demodulators.

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