Brief Papers

Digital-Compatible High-Performance Operational Amplifier with Rail-to-Rail Input and Output Ranges

Wen-Chung S. Wu, Ward J. Helms, Jay A. Kuhn, and Bruce E. Byrkett

Abstract— **Decreasing integrated-circuit feature sizes and increased packing densities are opening new applications for single chip systems. The technology choices for these systems are dominated by digital performance issues, however, analog functions must also be performed. This paper presents a CMOS buffer amplifier which operates on a single 5-V power supply. Because of the uniquely symmetrical design, which compared to past work [2]–[6], adds the following advantages:**
1) Rail-to-rail linear, symmetrical operation at both the input and output.
2) Unique output stage allows the use of gate channel capacitors of standard MOSFET's as the compensation capacitor saving die area from 80% ~ 93% in a standard single polysilicon digital processes.
3) Large gain-bandwidth product.
4) High power supply rejection ratio.
5) Good common-mode rejection ratio.
6) Easy compact layout suitable for design automation (layout as a parametric cell, allows easy adaption to changing processes). The buffer is capable of driving 300 Ω || 100 pF with a loaded gain-bandwidth product of more than 4 MHz and a fully loaded slew rate of greater than 4 V/μs.

I. Circuit Description

THE cascode input stage has been redesigned to attain a more symmetrical topology, improved, better balanced circuit performance. This improves the CMRR and PSRR performance of the circuit. The new input stage is shown in Fig. 1. This is an improvement over the input stage of Fisher and Koch [5] as the common mode voltage moves from the positive to the negative rail, the stage goes through three modes. First the PMOS devices are cutoff, then both device pairs operate, and finally the NMOS devices cutoff, during this time the input stage transconductance changes by a factor of 2. This requires excessive frequency compensation to ensure stability at all input levels. Also, transient distortion may occur as rapid changes in common-mode voltage modulate the transconductance value.

The input stage shown in Fig. 1, based on a bipolar counterpart [7], was devised to overcome the aforementioned problem. The n-channel MOS pair MI1, MI2, is biased by a current source MP1 via MN3 and the current mirror MN1, MN2, when the p-channel MOS pair is nonconducting. When the common-mode input voltage is at least equal the reference voltage V_r = 1 V above AVss (assuming equal transistor threshold voltages). When the input CM voltage decreases through the reference voltage V_r, the source current is gradually steered from the source of MN3 to the p-channel pair, removing current from the n-channel pair. Since the transconductance of MOSFET's are proportional to the square root of drain current, unlike the direct proportion of bipolar devices, keeping the sum of the drain currents constant, the combined transconductance variation of PMOS and NMOS pairs will be improved from a factor of 2 to a factor of $\sqrt{2}$ compared to the original circuit of Fisher and Koch [5].

To make the top PMOS cascode stage work symetrically with the bottom NMOS stage we have employed a "floating current source." Current mirrors are formed by MB6, M10, and MB5, M9. Transistors MB7 and MB4 act as resistors. The bias currents for the upper and lower cascode stages M11, M13 and M7, M5 are thus set equal. With proper selection of the ratio between MB5, M9 and MB6, M10, we may set the reference current while maintaining node A and node B at the same potential. This has been confirmed by simulation when even considering temperature and processes variations, the voltage difference between node A and node B is maintained to be less than 5%.

A. Output Stage

Fig. 2, shows an output stage model which has been modified from a circuit previously reported [4], [8]. When limited to a five volt or less power supply, the choice of output stage configuration is severely limited by the voltage overhead of the transistor gate-to-source voltage. For near-the-rail swing application, it is inevitable to use common-source output transistors. Therefore, one must solve the classical class B level shifting problem. Complementary output devices MA1 and MA2 are driven by complementary common-gate level shifters MA3 and MA4. These common-gate devices are driven from the folded cascode input stage previously discussed with currents $I + gm_n/2$ and $I + gm_p/2$ as shown in the figure.

During quiescent operation, both MA3 and MA4 are biased into a conducting state. The gate-to-source V_{GS} bias voltages of the output transistors are kept low to minimize quiescent power consumption. The exact bias levels are controlled by the reference voltages V_{B1} and V_{B2}.

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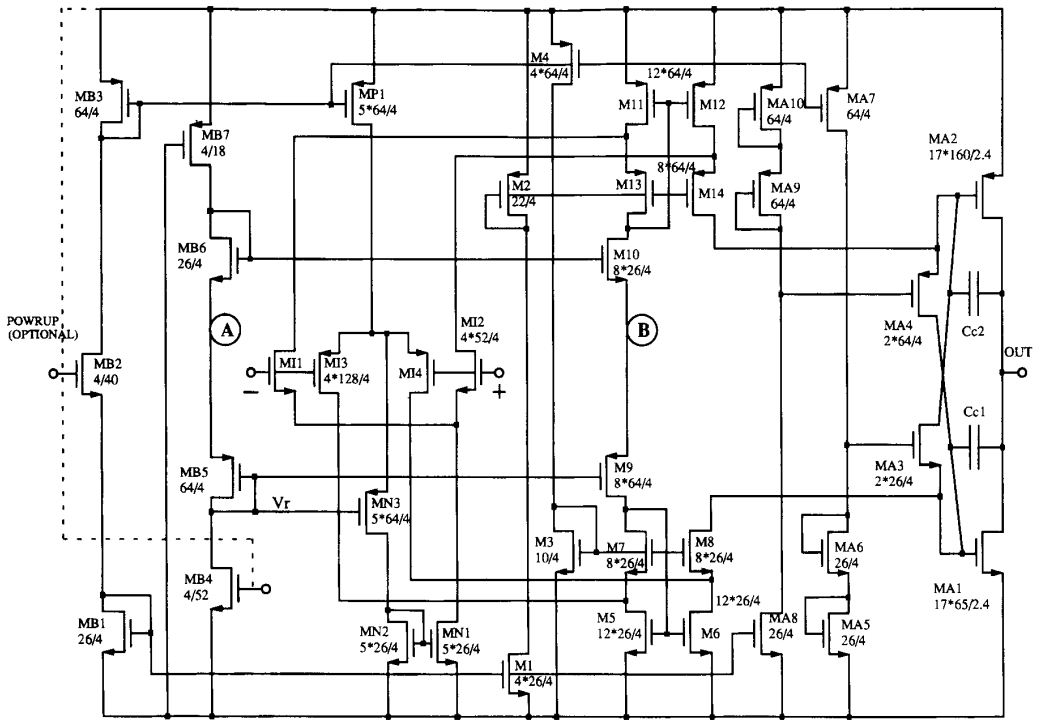

Fig. 1. Rail to rail operational amplifier schematic.

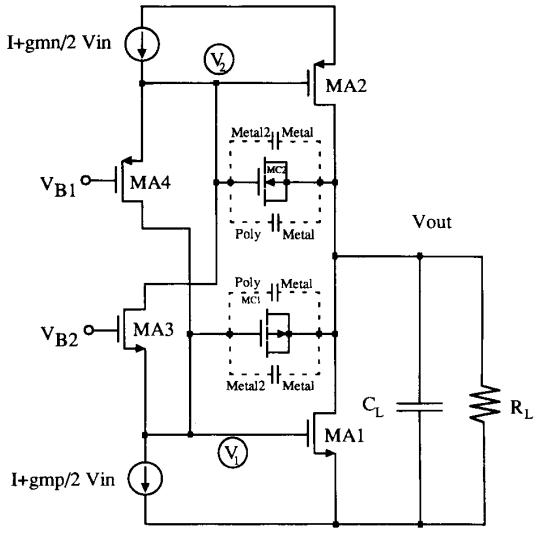

Fig. 2. Miller compensation by using MOSFET C_{GS}. C_{GD}, and C_{GB}.

During a negative slewing period, the gate voltage of MA1 will be pulled high. Fixed gate potential V_{B2} will cause MA3 to cutoff. MA4 will carry the full bias current, driving its source and the gate of MA2 high, turning off MA2. Under the condition of strong sourcing, MA2 will be turned on, symetrically repeating the above operation on the other side of the circuit. Ultimately the swing on the gate of MA1 (MA2) will reach a limit at $2V_{DS(\text{sat})}$ from the positive (negative) rail. This large drive swing to both output devices allows driving heavy loads close to the rails. After the slewing period, as the input signal returns toward zero, both MA3 and MA4 will turn on again and the circuit quickly settles to a quiescent state. The entire amplifier schematic is shown in Fig. 1.

B. Frequency Compensation

Similar to conventional two-stage operational amplifiers, Miller compensation capacitors are used to stabilize the operation of the op amp in closed loop operation. The compensation capacitor is placed across the complementary output gain stage, and the dominant pole frequency of the overall amplifier will then be $g_{mi}/[(g_{mo}R_L)C_C]$, where g_{mi} is the input device transconductance, MA3 or MA4, and g_{mo} is the output device transconductance MA1 or MA2.

In a double metal single polysilicon digital process, the compensation capacitor can normally be built with the form of a poly-metal-metal2 sandwich that is about one-tenth as area efficient as a similar double polysilicon capacitor. A double polysilicon process will typically cost 10–20% more than a standard digital process due to extra mask and processing steps. The unit capacitance between poly-poly2 is about 7 to 15 times larger than that between polysilicon and metal or between metal and metal2.

The MOS transistor itself can be used as a capacitor when biased in the triode region, the gate forming one plate and the source, drain, and channel forming another. Unfortunately, the lightly doped underlying substrate causes a very high voltage

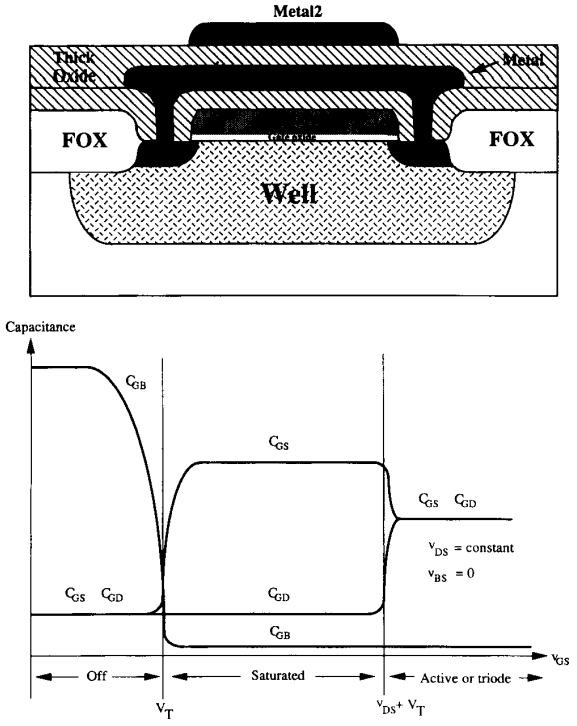

Fig. 3. Voltage dependence of C_{GS}, C_{GD}, and C_{GB} as a function of v_{GS} with v_{DS} = constant and v_{BS} = 0.

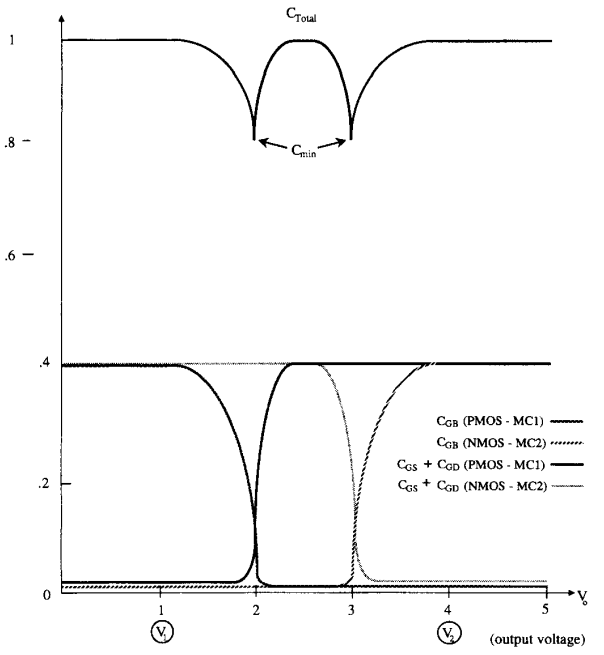

Fig. 4. Capacitance versus output voltage (V_o).

coefficient. The symetrical design of this output stage allows us to use the gate channel capacitances from standard MOSFET's as the compensation capacitor because circuit symetry cancels much of the capacitance nonlinearity as shown in Fig. 4. This achieves similar area efficiency to double-poly capacitors. The nonlinearity of the gate channel capacitance versus terminal voltages, are shown in Fig. 3. The gate channel capacitance is large when the transistor is operating within the saturation region. If we use an NMOS and PMOS in parallel as the compensation capacitor the op amp will be stable at any output voltage as long as the gate channel capacitance provided by either MOSFET's is larger than or equal to the total required compensation capacitance.

Additional die area is saved by using the gate channel capacitors above with the gate-to-bulk diffusion capacitance from the same MOSFET. The circuit diagram of the output stage is shown in Fig. 2. Since the gate potentials of MA1 (V_1) and MA2 (V_2) are biased near 1 V and 4 V, respectively, we can then draw a capacitance versus V_o plot based on Fig. 2, in Fig. 4. As long as $C_{\min}$ is larger than the total required compensation capacitance, the op amp will be fully compensated. We now may add sandwitch capacitances $C_{\text{metal}-\text{metal2}}$ and $C_{\text{metal}-\text{poly}}$ to further increase the capacitance per unit die area.

II. Performance

We have implemented three op amps which utilize the folded cascode input stage introduced in Fig. 1 and three types of compensation capacitor. These op amps were fabricated through the MOSIS service in a 2 μm p-well double metal single polysilicon CMOS process.

One uses parallel PMOS and NMOS compensation capacitors, op_npc, another, op_cgb, uses gate channel capacitances together with the gate-bulk capacitance of MOSFET's and the final one, op_c, uses a sandwich-like capacitor. Special layout considerations were taken to avoid large parasitic source and drain capacitances and resistances. For maximum compactness and symmetry, all transistors were pitch matched and placed with all the PMOS on one side and all the NMOS on the other. This allows minimum guard ring area, but still avoids possible latchup between PMOS and NMOS. Most importantly, these op amps are programmable, i.e., they have user-configurable bias current (by varying the size of MB1), compensation, and output impedance. This allows easy modification across processes with minimal change in layout (this is an important issue in designing modules for a silicon compiler using parametric layout techniques).

Dc transfer characteristic measurements for gains of $+1$ and -1 under light and heavy loading conditions show that with light loading the output will swing to within 100 mv of the rails and with heavy loading, 300 ohms, to within 400 mv. The frequency response for all three op-amps were measured with load a light load 1 MΩ $\|$ 11 pF and with a heavy load, 300 Ω $\|$ 100 pF. The results are summarized in Table I and the frequency response plot of the efficient compensation scheme described above, op_cgb, is shown in Fig. 5. Frequency response measurements of these op amps with heavy 300 Ω $\|$ 300 pF loads clearly show that the fabricated op amp is suitable to drive a 300 Ω $\|$ 300 pF load with a small deterioration in the phase margins ($\sim 15°$). Our fabricated compensation capacitor values were nonideal and

TABLE I
PERFORMANCE PARAMETERS OF FABRICATED OP AMPS

Parameter	Measured Data		
	op_c	op_cgb	op_npc
Die Area	690 sq mil	566 sq mil	641 sq mil
Load	1MegΩ || 11pf 300Ω ||100pf	1MegΩ ||11pf 300Ω ||100pf	1MegΩ ||11pf 300Ω ||00pf
Avol	95 dB 68 dB	95 dB 68 dB	95 dB 68 dB
Phase Margin	81 deg 76 deg	90 deg 83 deg	46 deg 65 deg
Gain Margin	12 dB 10 dB	18 dB 15 dB	9 dB 9 dB
Bandwidth	6.5 MHz 4.1 MHz	5.4 MHz 3.4 MHz	14.2 MHz 5.6 MHz
Slew Rate	5 V/μs 4 V/μs	5 V/μs 4 V/μs	5 V/μs 4 V/μs
Vos	10 mV	10 mV	10 mV
PSRR	100 dB	100 dB	100 dB
CMRR dc	88 dB	88 dB	88 dB
CMRR 1 MHz	65 dB	65 dB	65 dB
Noise @ 100 Hz	455 nV/$\sqrt{}$Hz	455 nV/$\sqrt{}$Hz	455 nV/$\sqrt{}$Hz
Noise @ 100 kHz	36 nV/$\sqrt{}$Hz	36 nV/$\sqrt{}$Hz	36 nV/$\sqrt{}$Hz
Input CMR	0 −5 V	0 −5 V	0 −5 V
Power Dissapation	2 mW	2 mW	2 mW

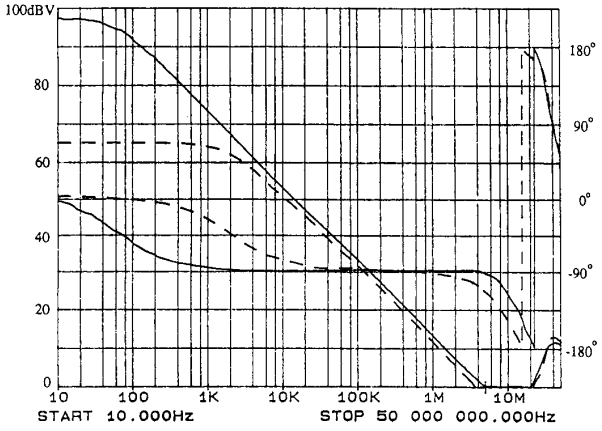

Fig. 5. Open loop transfer characteristics versus frequency for op_cgb. ——: $R_L \parallel C_L = 1\,\mathrm{M}\Omega \parallel 11$ pF, — —: $R_L \parallel \mathrm{L} = 300\,\Omega \parallel 100$ pF.

are responsible for some deviation in the measured unity-gain bandwidths and phase margins. For the measured frequency response plots we can readily infer that these op amps may be compensated for an unloaded gain-bandwidth of around 8–10 MHz and a loaded (300 Ω || 100 pF) one of around 4–5 MHz, with a phase margin of 60 degrees.

The total harmonic distortion when driving 4.5 V_{p-p} into 1 kΩ load, 4 V_{p-p} into 300 Ω load and 3 V_{p-p} into 100 Ω load, at 10 kHz was −65 dB, −55 dB and −55 dB, respectively. At one kilohertz, the normal distortion reporting frequency, we could not observe the distortion with our HP35660 Dynamic Signal Analyzer, therefore our distortion figures are given at the more difficult frequency of 10 kHz. The $1/f$ noise corner is at around 100 kHz with an observed noise of ~ 16 nV/sqr. Hz. Taking into account the frequency response of the circuit this corresponds to a noise floor of 36 nV/sqr. Hz.

To prove the op amps rail-to-rail common-mode performance, the small-signal frequency response was repeated using different input common-mode voltages. The variation in gain is observed to be only a few decibels across the input CMR. The phase margin remains almost the same across the input CMR for op_c, changes less than 10 degrees for op_cgb, and increases to about 30 degrees when compared to the zero CM voltage for op_npc. The change in the phase margin can be explained by gate channel capacitance variation with terminal voltage.

III. SUMMARY

Digital compatible CMOS buffer amplifiers have been presented which achieve a high degree of linearity along with heavy load (300 Ω || 100 pf) driving capability from a single 5-V supply. It has been shown that with a novel design of the class AB output stage, we are able to use the gate channel capacitance from standard MOSFET's as the compensation capacitors for the op amp achieving similar area efficiency as double poly-silicon capacitors. These op amps have good performance characteristic in terms of CMRR, PSRR, and noise level which makes them attractive in many high-performance circuit applications. The variation of small-signal voltage gain versus input CMR are similar with a recently reported result [12]. Circuit details and measured results have been given which clearly show improvement over the previously reported results [2]–[6], [12].

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