Eliminating Inductive Noise of External Chip Interconnections

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Abstract— **On-chip balanced drivers can essentially eliminate inductive noise, without any power dissipation penalty, and independently of the number of chip drivers switching simultaneously or the switching speed. In addition, balanced interconnections on PWB's and MCM's substantially reduce crosstalk, increase noise immunity, and eliminate ground noise.**

I. Introduction

A major performance limit of electrical interconnections is encountered when one attempts to interconnect a high-speed, high pin-out integrated circuit chip having many drivers that switch simultaneously. For example, when 32 b switch simultaneously in the same direction at 1 ns or so, the inductive noise (i.e., ΔI noise, or ground bounce) developed between the ground in the printed wiring board (PWB) and the ground in the chip is excessive [1]–[5] and can cause system errors.

The purpose of this paper is to describe how on-chip balanced drivers together with associated balanced chip receivers can essentially eliminate this source of noise without a power dissipation penality. On-chip balanced drivers are needed to drive balanced interconnections on PWB's and multichip modules (MCM's) in order to realize the substantial benefits of reduced crosstalk, increased noise immunity, and elimination of ground noise [6].

II. Unbalanced On-Chip Drivers

Fig. 1(a) shows the conventional method used to drive unbalanced transmission lines on a PWB. For our purposes, only the AC circuit needs to be considered. That is, power supply voltages, bias resistors, voltage planes, and by-pass capacitors are omitted. The rate of change of ground return current, $\dot{I}_g$, flows from the terminations located at the chip receivers, through the ground vias, ground plane, ground via at the chip, wire bond of the chip, ground via on the chip, and finally to the chip ground plane. The magnitude of the inductive noise developed between the two ground planes in Fig. 1(a) is indicated as v_n. Neglecting mutual inductances, it is given, approximatedly, by [1]

$$v_n = \frac{L_s(n\dot{I})}{N_g} \tag{1}$$

where

L_s = self inductance of the ground return path (nH)
n = number of chip drivers switching simultaneously in the same direction
$\dot{I}$ = rate of change of the signal current (ma/ns)
N_g = number of ground leads on the chip.

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For example, for $n = 8$, $N_g = 3$, $\dot{I} = 20$ ma/ns, and $L_s = 2.62$ nH (e.g., a 100 mil wire bond), (1) yields $v_n = 140$ mv. This value of v_n is already significant relative to the AC noise immunity of ECL of about 215 mv, especially since crosstalk can contribute an equal amount of noise. As the rise time is reduced to 0.1 ns, v_n increases by an order of magnitude, and inductive noise becomes overwhelming. Thus, L_s must be reduced, since increasing N_g is not efficient because ground leads carry no information and replace potential signal leads.

To help reduce L_s, solder bumps and TAB for chip attachment may be effective. This has the potential of significantly reducing the inductive noise, v_n. Another method which can complement these technologies involves using balanced on-chip drivers and balanced interconnections.

III. Balanced On-Chip Drivers

For balanced on-chip drivers, Fig. 1(a) is transformed into Fig. 1(b) by replacing each on-chip unbalanced driver with a balanced driver, and replacing each unbalanced signal lead with a balanced pair of leads. In this case, there is no net rate of change of current flow, $\dot{I}_g = 0$, in the ground return path and the inductive noise across the common ground is eliminated, or $v_n = 0$. In addition, we shall see that the balanced interconnections can easily be impedance matched at both ends which significantly reduces signal reflections. Some other benefits of balanced interconnections are discussed in [6], namely a significant reduction in crosstalk, and a substantial increase in noise immunity along with the elimination of ground noise. In this manner, it becomes practical to retain wire bond chip attachment for high-speed chips (rise time ~0.1 ns). This can complement the development of the high technology chip attachments mentioned earlier.

Some of the additional signal leads needed can be obtained from the reduction in the number of ground leads required when using balanced interconnections relative to unbalanced interconnections. Recall, only those drivers which switch simultaneously (i.e., to within a duration equal to a signal rise time) in the same direction need to be balanced.

One usually expects a factor of two power dissipation penalty when using balanced drivers. In the next section, we shall present a particular balanced driver circuit that can avoid this significant power dissipation penalty.

IV. Power Dissipation

Fig. 2(a) shows the output portion of a conventional unbalanced driver circuit which is impedance matched at the receiver end only. $-V_1$ and $-V_2$ denote the two logic levels, and $-V_T$, R_T, denote the power supply voltage and termination resistor, respectively. For convenience, we shall let

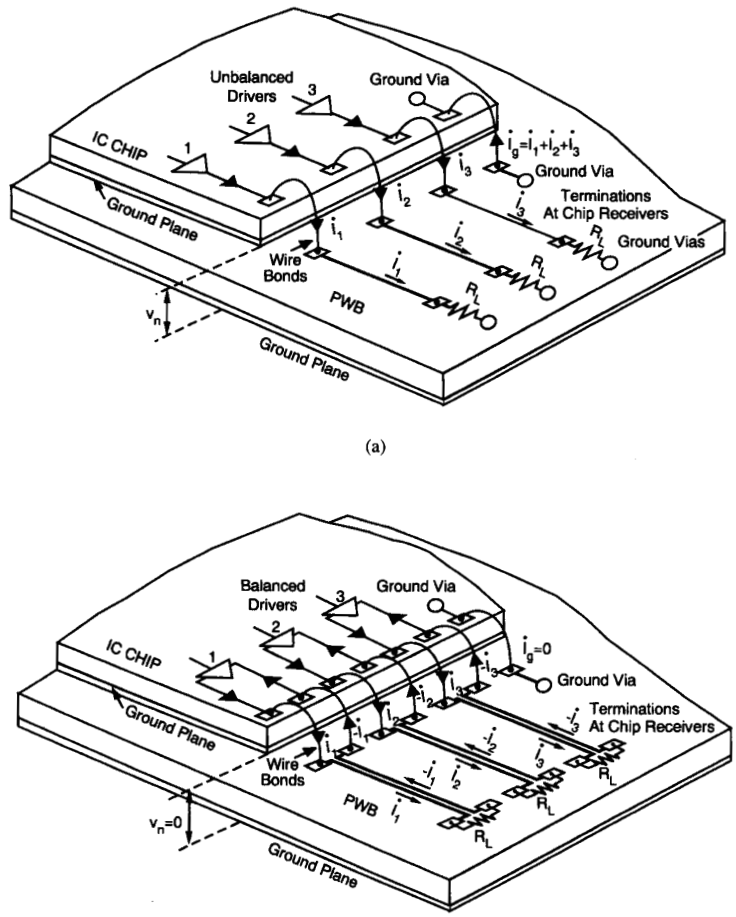


Fig. 1. AC circuits for unbalanced and balanced drivers. (a) AC circuit for unbalanced drivers. (b) AC circuit for balanced drivers.

$V_T > V_2 > V_1 > 0$. Z_0 and R_0 denote the characteristic impedance of the unbalanced transmission line and output impedance of the ECL emitter follower, respectively.

The time average power dissipated by the output portion of the unbalanced circuit is given by

$$\bar{P}_U = \left[\frac{1}{2}\right]\left[\frac{V_T(V_T - V_1)}{R_T} + \frac{V_T(V_T - V_2)}{R_T}\right], \quad (2)$$

or

$$\bar{P}_U = V_T[2V_T - V_2 - V_1]/(2R_T). \quad (3)$$

Let

$$\bar{P}_U = \bar{P}_{Ui} + \bar{P}_{Ue} \quad (4)$$

where

$\bar{P}_{Ui}$ = average unbalanced power dissipated internal to the chip (i.e., the emitter follower) and

$\bar{P}_{Ue}$ = average unbalanced power dissipated external to the chip (i.e., the termination resistor).

$\bar{P}_{Ui}$ and $\bar{P}_{Ue}$ are given by

$$\bar{P}_{Ui} = [V_2(V_T - V_2) + V_1(V_T - V_1)]/(2R_T), \quad (5)$$

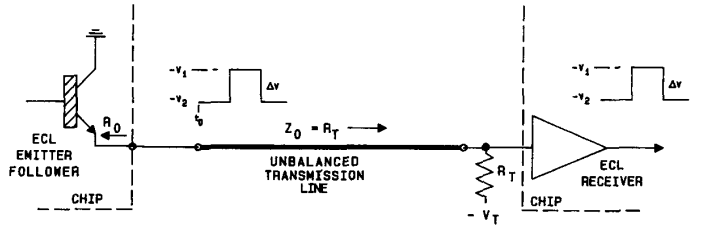
and

$$\bar{P}_{Ue} = \left[(V_T - V_2)^2 + (V_T - V_1)^2\right]/(2R_T). \quad (6)$$

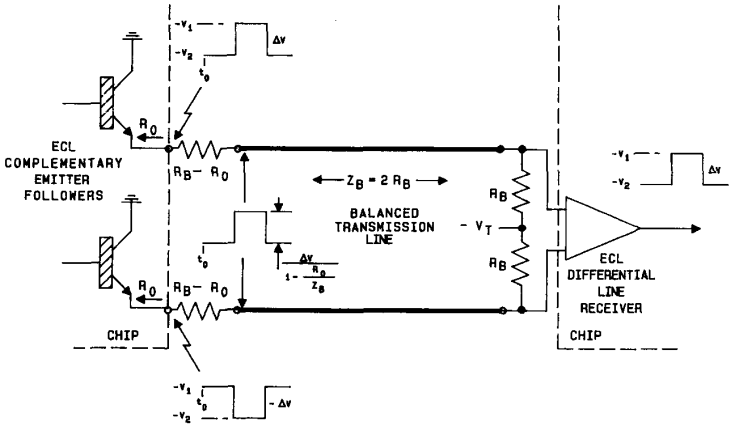
The one-half factors appearing in (2), (5), and (6) result from the uniform averaging of the power dissipations during the two states V_2, V_1. For example, during state V_2 the first term in (5) indicates that the power dissipation between collector and emitter is $V_2(V_T - V_2)/R_T \equiv V_2 I_2$ where I_2 represents the collector-emitter current flow.

Fig. 2(b) shows the output portion of a particular balanced driver circuit that is impedance matched at both the driver and receiver ends. Z_B and R_B denote the characteristic impedance of the balanced transmission line and termination resistors, respectively. The remaining portions of the unbalanced and balanced on-chip drivers (not shown in Fig. 2) are identical and dissipate equal power.

The power dissipated by the output portion of the balanced circuit can be considered as twice the unbalanced portion but with $R_T = 2R_B - R_0$. This relation results from comparing one branch of the balanced driver in Fig. 2(b) with the



(a)



(b)

Fig. 2. The unbalanced and balanced ECL driver circuits dissipate equal average power when $R_B = R_T + R_0/2$. (a) Unbalanced driver circuit, impedance matched at one end. (b) Balanced driver circuit, impedance matched at both ends.

unbalanced driver circuit in Fig. 2(a). Accordingly, we have that

$$\bar{P}_B = 2\bar{P}_U|_{R_T=2R_B-R_0}, \tag{7}$$

and

$$\frac{\bar{P}_B}{\bar{P}_U} = \frac{2R_T}{2R_B - R_0}. \tag{8}$$

In analogy with (4), let

$$\bar{P}_B = \bar{P}_{Bi} + \bar{P}_{Be} \tag{9}$$

where $\bar{P}_{Bi}$ = average balanced power dissipated internal to the chip (i.e., the two emitter followers) and
$\bar{P}_{Be}$ = average balanced power dissipated external to the chip (i.e., the four resistors).

$\bar{P}_{Bi}$ and $\bar{P}_{Be}$ are given by

$$\bar{P}_{Bi} = 2\bar{P}_{Ui}|_{R_T=2R_B-R_o}, \tag{10}$$

and

$$\bar{P}_{Be} = 2\bar{P}_{Ue}|_{R_T=2R_B-R_0}. \tag{11}$$

If we impose the constraint that the power dissipated by the output portions of the balanced and unbalanced driver circuits be equal, we have from (8) that

$$\frac{\bar{P}_B}{\bar{P}_U} = 1, \tag{12}$$

TABLE I
AVERAGE POWER DISSIPATION OF ECL DRIVER CIRCUITS HAVING $R_0 = 6\Omega$

Unbalanced Driver	Balanced Driver
$(R_T = 50\Omega, Z_0 = 50\Omega)$	$(R_B = 53\Omega, Z_B = 106\Omega)$
$\bar{P}_U$ = 26.80 mW	$\bar{P}_B$ = 26.80 mW
$\bar{P}_{Ui}$ = 15.01	$\bar{P}_{Bi}$ = 15.01
$\bar{P}_{Ue}$ = 11.79	$\bar{P}_{Be}$ = 11.79

or

$$R_B = R_T + R_0/2, \tag{13}$$

and

$$Z_B \equiv 2R_B = 2R_T + R_0. \tag{14}$$

As an example, let V_T = 2 V, V_2 = 1.705 V, V_1 = 0.955 V, $R_T = 50\Omega$, and $R_0 = 6\Omega$. These are typical values for present day National Semiconductor ECL drivers and yield the results presented in Table I.

As mentioned earlier, the values of $\bar{P}_{Ui}$ and $\bar{P}_{Bi}$ only account for the average power dissipated by the output emitter followers of the on-chip ECL drivers. To account for the power dissipated in the remaining portion of the on-chip ECL driver circuitry, a common power dissipation of about 25 mW must be added to both $\bar{P}_{Ui}$ and $\bar{P}_{Bi}$. The total power dissipated becomes 26.8 + 25 = 51.8 mW and the on-chip power dissipation is 15 + 25 = 40 mW. Accordingly, about

77% of the total power dissipated by the ECL driver circuits is dissipated on-chip.

Interestingly, (8) is a general result that holds for general IC drivers independent of the operating voltages V_T, V_2, and V_1. For example, Fig. 2 and the equations above apply when the ECL technology is replaced with comparable GaAs technology. For unbalanced and balanced GaAs drivers we have that $V_T = 2$ V, $V_2 = 1.9$ V, $V_1 = 0.4$ V, $R_T = 50\ \Omega$, $R_0 = 8\Omega$, and $R_B = 54\Omega$. The above equations yield $\bar{P}_U = \bar{P}_B = 34$ mW, $\bar{P}_{Ui} = \bar{P}_{Bi} = 8.3$ mW, and $\bar{P}_{Ue} = \bar{P}_{Be} = 25.7$ mW. Also, for GaAs, the on-chip driver power dissipation not included in $\bar{P}_{Ui}$ or $\bar{P}_{Bi}$ is about 225 mW rather than 25 mW for ECL technology, and the GaAs drivers operate 3–5 times faster than ECL drivers. The total power dissipated becomes $34 + 225 = 259$ mW and the on-chip power dissipation is $8.3 + 225 = 233.3$ mW. Accordingly, about 90% of the total power dissipated by the GaAs driver circuits is dissipated on-chip.

Finally, a conventional balanced driver circuit results when the two resistors labeled $R_B - R_0$ in Fig. 2(b) are shorted out. For this case with $R_B = R_T$, we have that $\bar{P}_B = 2\bar{P}_U$ or the conventional balanced driver circuit dissipates twice the average power dissipated by the unbalanced driver and is impedance matched at only one end. Also the signal swing on the conventional balanced transmission line is $2\ \Delta V$ or about twice the signal swing when the two resistors are not shorted. This results in twice the crosstalk on any nearby unbalanced transmission lines.

V. Conclusion

The use of on-chip balanced drivers in place of conventional unbalanced drivers can essentially eliminate inductive noise of external chip interconnections in high-speed (rise time ~0.1 ns) electronic systems, without any power dissipation penalty. The chief penalty is the use of two conductors per signal for the balanced drivers. However, some of the required balanced leads can replace many of the ground leads which are no longer needed since ground noise is substantially reduced with the use of balanced interconnections. By eliminating inductive noise, it becomes possible to retain wire bonds for chip attachment of high-speed chips. Also, with the elimination of inductive noise, it becomes practical to introduce digital architectures having many high-speed drivers per chip to serve a large number of bits per word. In addition, on-chip balanced drivers and balanced interconnections on PWB's and MCM's substantially reduce crosstalk, and increase noise immunity.

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