Simple Precision Bias Circuit for Medium-Power Amplifiers

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Abstract— **We describe a new bias current regulation circuit for single-stage bipolar and FET amplifiers which achieves high precision and simplicity through a combination of feedback error amplifier with bandgap reference. The internally generated reference voltage can be preset between 100–200 mV. Our approach is ideal for applications where the overhead voltage must be minimized to reduce power dissipation, and typically offers $<$ 0.5% regulation and $\leq$ 40 ppm/°C temperature coefficient. We present three common applications which demonstrate the unique advantages of the new topology.**

I. Introduction

THE output level from a driver circuit is generally set by regulating the current through the active devices. Three typical applications are illustrated in Fig. 1. Fig. 1(a) depicts the bias circuit for a single stage limiting or linear amplifier [1], [2]. Q_0 could also be an FET, instead of the BJT shown [3]. The boxes denote isolation circuits that decouple the DC bias paths from the high frequency signal paths, which are omitted for brevity. In a limiting amplifier, Q_0 acts like a switch and thus the output signal level (current or voltage) is proportional to the bias current I_o; consequently, stabilization of I_o is a primary concern. The gain of a linear amplifier depends on the current I_o through Q_0: regulation of $< 3\%$ is often desirable in applications requiring very precise gain, even when feedback is employed [1]. Even in less demanding applications, knowledge that accurately preset bias levels should exist can greatly simplify circuit diagnosis and maintainance. Fig. 1(b) depicts a line driver for an electrical or optical interconnection which uses a differential amplifier as a current switch. Q_0 should maintain the driver output level within a 1–10% tolerance [4], [5]. By controlling the quiescent base or gate bias of Q_0, the error amplifier in these examples sets $I_o \approx V_{\text{ref}}/R_s$, where V_{ref} is a compensated reference voltage. V_{ref} is typically ≥ 1 V. In the third example, Fig. 1(c), a switch mode converter is controlled by feedback from R_s to maintain a preset current through an LED or high power laser, for which the load voltage $V_L = 0.5$–1.5 V [6].

Although precise regulation improves performance and maintainability, several practical drawbacks are encountered. First, power consumption is generally a major concern in low voltage circuits. The power efficiency of the circuit in Fig. 1(c) is reduced by a factor of $1 + V_{\text{ref}}/V_L$ due to the voltage drop across R_s. The voltage drop V_{ref} also raises the minimum supply voltage needed for circuits 1(a) and 1(b). In each case, it is very desirable to set $V_{\text{ref}} \ll 1$ V. The author is not aware of any regulator which produces a compensated voltage

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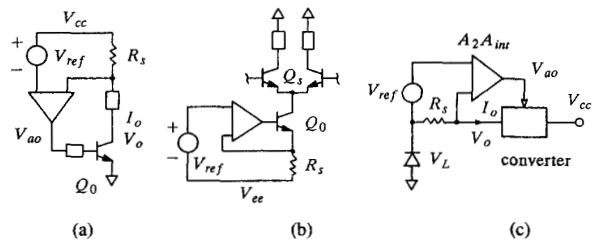


Fig. 1. Three common circuits where the operating point is established by current regulation: (a) linear or limiting amplifier, (b) laser or line driver, (c) LED or high power laser bias circuit.

$<$ 1 V referenced to V_{cc}. Additionally, the error amplifier must have a low input offset voltage and good common mode rejection, even though the amplifier input operates at [1]–[5] or beyond [6] the supply rail. Discrete circuits have traditionally been chosen for the feedback amplifier for simplicity [1]–[4], whereas IC operational amplifiers are not generally available with common-mode input voltages V_{icr} close to V_{cc}. Finally, increased circuit complexity may reduce the overall reliability and is undesirable. We describe a novel feedback circuit which incorporates a low voltage bandgap reference within the error amplifier to achieve high performance simply.

Two conventional current sensing feedback topologies used to implement the circuits in Fig. 1 are illustrated in Figs. 2(a) and (c) [1]–[3], [7], along with our corresponding proposed improved topologies in 2(b) and (d), respectively. The circuits in Figs. 1(b)–(c) are consistent with Fig. 2, while Fig. 1(a) would use complementary devices since its feedback loop is referenced to the positive rail. Q_1 and Q_2 compare the voltage drop I_oR_s with the reference source V_{ref}. Q_1 provides an offset voltage which compensates for the temperature and bias dependent V_{BE} of Q_2. The common base input stage in Fig. 2(a) provides a large voltage gain and an extended common mode range. The amplified error signal appears at the collector of Q_2 and adjusts the current through Q_0 by way of the intermediate amplifier. The intermediate amplifier may provide current gain, voltage gain, signal inversion, or level shifting, as required to control Q_0. In Fig. 2(c), the voltage followers provide level shifting and current gain for isolation. The intermediate differential amplifier must provide both voltage and current gain in this case. Although Fig. 2(b) is a much simpler circuit to build, the common collector topology in Fig. 2(d) is ideally suited for use with parasitic lateral bipolar transistors in CMOS applications.

II. New Approach

We shall first discuss the circuits in Figs. 2(a) and (b). A departure from conventional practice in circuit 2(a) must

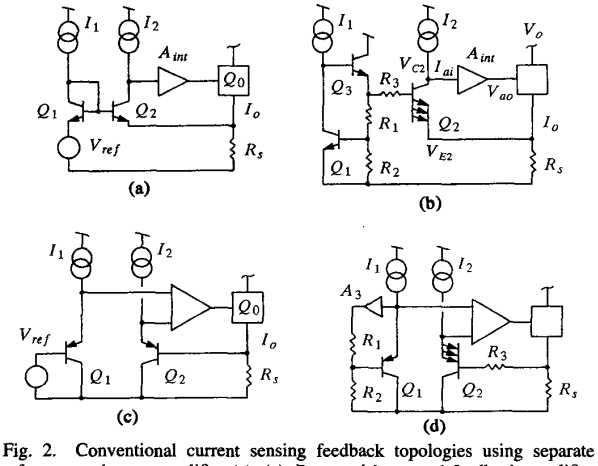


Fig. 2. Conventional current sensing feedback topologies using separate reference and error amplifier (a), (c). Proposed improved feedback amplifier topologies incorporating an internal low voltage bandgap reference (b), (d). A_{int} denotes the intermediate amplifier.

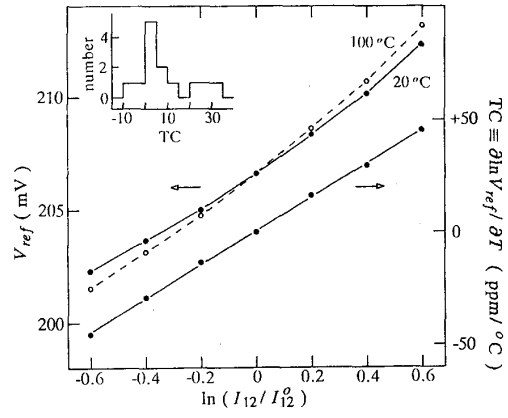


Fig. 3. Temperature and bias dependence of new feedback circuit prototype using CA3046 transistor array. Component values were $R_1 = 383\ \Omega$, $R_2 = 2.37\ \text{k}\Omega$, $R_3 = 3.83\ \text{k}\Omega$, $K = 27$. Zero TC point occurs at $I_{12}^{o} = 1$ mA.

be made when $V_{\text{ref}} \ll 1$ V, in which case ΔV_{BE} variations are controlled by carefully regulating the ratio of collector currents I_1 and I_2. This is a relatively simple task, and once steps to govern the current ratio are taken, the addition of $R_1 - R_3$ converts the amplifier $Q_1 - Q_2$ into a bandgap derived reference as shown in Fig. 2(b). This topology is much simpler than previously reported approaches using separate bandgap circuits [8]–[10]. Because essentially only one V_{BE} drop is used, the circuit can operate at supply voltages near 1 V. The divider $R_1 - R_2$ scales V_{BE1} with feedback from Q_3, whereas R_3 provides base current compensation [8], [11]. Voltage follower Q_3 isolates I_1 from the divider and is useful when β is low, but often can be omitted in favor of simplicity. Assuming that the closed-loop gain is large, nodal analysis of this circuit gives:

$$V_{\text{ref}} = \frac{R_1}{R_2} V_{\text{BE1}}(I_1, T) + \eta V_T \ln K + \frac{R_1 I_1}{\beta_1} - \frac{R_3 I_2}{\beta_2}, \quad (1)$$

where $K \equiv mI_1/I_2$ is the ratio of Q_1 to Q_2 emitter current densities and m is the usual ratio of transistor emitter areas. $V_T = k_B T/q$ is the thermal voltage and η is the forward ideality factor. The last two base current error terms in (1) cancel to first order when $R_3 = R_1(I_1\beta_2/I_2\beta_1)$. The first two terms in (1) have opposite temperature dependences and first-order temperature compensation is achieved by setting $(R_2/R_1)(\eta k_B/q) \ln K = -dV_{\text{BE1}}/dT$, in which case $V_{\text{ref}} \approx (R_1/R_2)(1250)$ mV [12]. V_{ref} can be set between 100–200 mV with the appropriate choice of K. The measured variation of both V_{ref} and the temperature coefficient $\text{TC} \equiv (\partial V_{\text{ref}}/\partial T)/V_{\text{ref}}$ with the net bias current $I_{12} \equiv I_1 + I_2$ are shown in Fig. 3 for an implementation of 2(b) built using a CA3046 npn transistor array and an op-amp. The nominal transimpedance $\partial V_{\text{ref}}/\partial I_{12}$ varies with temperature between 5.8 Ω to 7.3 Ω. The temperature coefficient for a given I_{12} was nearly constant over the entire temperature range of 20°–120°C. Note that although curvature compensation was not needed in our prototypes, it can be easily incorporated by shunting R_2 with a simple resistor-diode network [13]. The predominant logarithmic dependence is $\Delta V_{\text{ref}} \approx (R_1/R_2)\eta V_T \ln(I_{12}/I_{12}^{o})$, where I_{12}^{o} denotes the zero TC bias current. The inset shows the distribution of TC for a sample of 13 circuits with $I_{12} = 1.0$ mA, the intended nominal value for I_{12}^{o}. As shown by Fig. 3, adequate performance is obtained in most applications if I_{12} is within 20% of I_{12}^{o}. Although V_{ref} is sensitive to the ratio I_1/I_2, the advantage of this approach is that the value of I_{12} is not critical. I_1 and I_2 may be obtained from a simple current source (e.g., [14]), but often can be derived from voltages already available in the system. I_{12}^{o} could be temperature dependent in other implementations. Temperature compensation can be improved in these cases by additionally tailoring the temperature dependence of I_1 and I_2 [13]. The output current with circuits 2(a)–2(b) is slightly less than V_{ref}/R_s due to the emitter current from Q_2; $I_o = V_{\text{ref}}/R_s - I_2$. This error is $< 0.1\%$ when $I_o > 10$ mA and $I_2 = 10\ \mu$A. Circuits 2(c) and 2(d) will be discussed later, for which this small error is reduced by $1/\beta$.

The overall complexity and performance of the circuits in Fig. 1 achieved using the circuit in Fig. 2(b) also depends on the intermediate amplifier. Q_2 in Fig. 2(b) offers appreciable gain so the requirements on this intermediate amplifier are greatly simplified. The following discussion examines the regulation of circuit 2(b), with particular attention to the complexity of the intermediate amplifier in the applications shown in Fig. 1. Besides the regulation of I_1 and I_2, the stability of I_o is determined by the voltage gain A_{int} and the intrinsic supply rejection $\partial V_{\text{ao}}/\partial V_{\text{cc}}$ (feedback loop open) of the intermediate amplifier, as well as the common base voltage gain A_2 provided by Q_2. V_{ao} denotes the output of the intermediate amplifier. The overall current regulation for circuits 1(a) and 1(b) can be described by

$$R_s \Delta I_o = \Delta V_{\text{ref}} + \frac{1}{(A_2 A_{\text{int}})_{\text{ul}}} \frac{\partial V_{\text{ao}}}{\partial V_{\text{cc}}} \Delta V_{\text{cc}} + \frac{1}{A_2 A_{\text{int}}} \frac{g_{o0}}{g_{m0}} \Delta V_o, \quad (2)$$

where $A_2 A_{\text{int}}$ and $(A_2 A_{\text{int}})_{\text{ul}}$ are the overall amplifier gain with and without loading by Q_0, respectively, and g_{o0} is the output conductance of Q_0. An expression analogous to

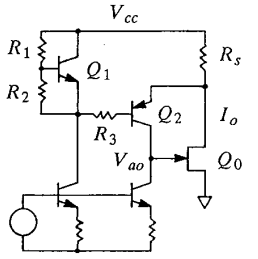
(2) holds for circuit 1(c) with the transistor gain g_{m0}/g_{o0} replaced by the control gain $\partial V_o/\partial V_{ao}$ of the converter. In deriving (2), base current errors are neglected and it is assumed that $|\Delta I_{E2}| \ll |\Delta I_O|$. Because of current gain limitations, we observe that $A_2 A_{int}$ in the third term of (2) is generally bounded above by $(I_2/(I_{ai})_{min})(1 + R_e I_o/V_T)$, where I_{ai} is the intermediate amplifier's input bias current and R_e is the resistance in series with Q_0's emitter. I_{ai} primarily depends on the number of transistors in the signal path, (n), excluding common base stages and current mirrors, and is bounded below by $(I_{ai})_{min} = I_o/\beta_0\beta^n$. β_0 denotes the current gain of Q_0, etc. The last term in (2) is usually negligible at low frequencies. It often simplifies analysis to note that the loading by Q_0 does not affect the second term in (2) since it attenuates both the feedback error signal and V_{cc} induced variations equally. However, this second term is implementation dependent and has no simple informative bound. The input bias current I_{ai} also contributes to the uncertainty in V_{ref} by altering I_2. It is desirable to keep $I_{ai}/I_2 < 1\%$, for which $n = 2$ is generally sufficient up to $I_o = 100$ mA with transistor current gains of 100.

The collector voltage V_{C2} will change as the feedback loop compensates for supply and temperature variations, etc. The corresponding deviation in Q_2's emitter voltage V_{E2} from the value of V_{ref} specified in (1) produces an apparent variation in V_{ref} given by $\partial V_{ref}/\partial V_{C2} = 1/A_2$. One can show that with ideal current sources supplying I_1 and I_2,

$$\frac{1}{A_2} \equiv \frac{\partial V_{E2}}{\partial V_{C2}} = \left(\frac{\eta V_T}{V_{AF2}} + \frac{1}{g_{m2}R_{ai}}\right)\left(1 + \frac{I_2}{\beta_2 I_1} + \frac{g_{m2}R_3}{\beta_2}\right), \tag{3}$$

where V_{AF} is the early voltage, $g_{m2} = I_2/\eta V_T$ is the transconductance of Q_2, and R_{ai} is the dynamic input resistance appearing at the intermediate stage. The first term in (3) contributes $1/4000$ for $V_{AF2} = 100$ V, which would be adequate for $< 1\%$ regulation. The second term exerts a dominant effect on A_2 for $I_2 = 100$ μA when R_{ai} is less than 1 MΩ. The last factor in (3) results from the compensatory voltage drop across R_3 and can be significant if Q_3 is omitted. The term in I_1 due to the impedance presented to Q_2's base by Q_1 is negligible. These results will next be applied to the three examples.

Circuit 1(a) represents the simplest application of circuit 2(b). Q_0 provides the necessary signal inversion so the intermediate amplifier need only provide current gain and level shifting. When this is obtained using voltage followers, R_{ai} reflects the input impedance of Q_0, so R_{ai} is ignored when (3) is substituted into $(A_2 A_{int})_{ul}$ and does not affect supply regulation. The intermediate stage can even be eliminated if Q_0 is an FET, as our example in Fig. 4 shows, since the DC gate current is negligible. Note again that the error amplifier input operates at V_{cc}, a task beyond the reach of conventional op-amps. The performance of this circuit, built using a CA3096CE npn/pnp transistor array, is reported in the accompanying table. In spite of the simplicity, the circuit has outstanding performance. The TC was -35 ppm/°C over the temperature range of 20°C–80°C, while the supply rejection was 0.28%/V at 20°C. Reliable operation is achieved with a



I_o	100 mA
V_{cc}	1.5 – 6.5V
max $\Delta I_o \mid_{20°}^{120°}$	0.3% ($V_{cc} = 2$V)
	0.4% ($V_{cc} = 5$V)
$d\ln I_o / dV_{cc}$	0.3%/V ($T = 20°$C)
	0.02%/V improved
	0.45%/V ($T = 100°$C)
	0.06%/V improved

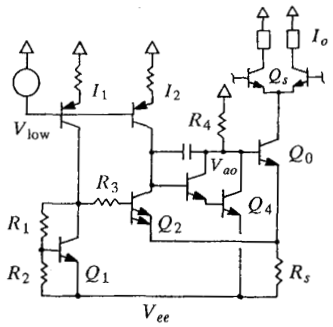
Fig. 4. MESFET amplifier bias circuit using CA3096CE transistor array. $m \approx 10$ is achieved using just two transistors in the array by substituting an npn in place of a pnp device for Q_1.

supply voltage down to 1.5 V. V_{ao} corresponds to V_{C2} in this example and $\partial V_{C2}/\partial V_{cc} = 1$; combining this with (2) and (3) gives $d\ln I_o/dV_{cc} \approx 1/V_{ref}A_2(R_{ai} \to \infty) = 0.3\%/V$. The measured results agree with the predicted supply rejection. By reducing the voltage variation at the collector of Q_2 using the second pnp in the CA3096 array as a cascode buffer, the rejection was subsequently improved to $\leq 0.06\%/V$, as noted in the table.

The intermediate amplifier must provide signal inversion in addition to current gain when circuit 2(b) is used to implement circuit 1(b). The inverter will decouple R_{ai} from Q_0 and consequently the degradation of A_2 by R_{ai} will be significant. This is more than compensated by the gain A_{int} provided by the inverter, however. Fig. 5 is an example of this application using a minimum complexity intermediate amplifier ($n = 2$). Typical performance data is also shown. This circuit was used in a 250 Mb/s twisted pair wire line driver where I_1 and I_2 are derived using $V_{low} = -1.8$ V from an unused ECL gate output. K and R_3 were selected to compensate for the $-2/\beta$ base current error produced by Q_0 and the current switch Q_s. Base current error compensation is important here and would be awkward to achieve using conventional op-amp circuits. Note that placing the inverter Q_4 at the output of the intermediate amplifier (after the voltage follower) presents Q_0 with a well-behaved low source impedance at high frequencies. By observing that R_{ai} has a dominant effect on A_2 and $\partial V_{ao}/\partial V_{ee} = -1$, the supply rejection is found to be:

$$\frac{\partial \ln I_o}{\partial |V_{ee}|} = \frac{1}{V_{ref}} \frac{\partial V_{ref}}{\partial I_{12}} \frac{dI_{12}}{d|V_{ee}|} + \frac{1}{\beta^2 g_{m2} R_4 V_{ref}} \tag{4}$$

The intrinsic regulation of the intermediate amplifier only contributes 0.013%/V through the second term in (4). This could be reduced by replacing R_4 with a current source, although the additional complexity is not warranted here. The first term, corresponding to ΔV_{ref} in (2), is (1/150 mV)(10



I_o	32 mA
V_{ee}	−4.5 to −7V
$\max \Delta I_o \mid_{20°}^{85°}$	0.13% (V_{ee} = −4.5V)
	0.2% (V_{ee} = −6.0V)
$d\ln I_o / d\lvert V_{ee}\rvert$	0.3%/V (20 − 85°C)

Fig. 5. Line driver bias circuit using new topology. This circuit demonstrates that intermediate amplifier does not compromise simplicity.

Ω)(0.04 mA/V) = 0.27%/V. The omission of Q_3 increases $\partial V_{\text{ref}}/\partial I_{12}$ by 70%(10 Ω vs 5.8 Ω).

The benefits of the extended common mode range of circuit 2(b) are clearly demonstrated in Fig. 6, where it is used to implement a low voltage "floating" reference for a 100 mA current source in a 155 Mb/s LED transmitter [6]. The feedback circuit $Q_1 - Q_4$ rides on the output of the converter, which varies between 0.5–1.5 V below ground. The converter provides polarity inversion and the entire circuit operates from a single V_{cc} = 4–6 V supply. An additional V_{ee} supply or carefully matched resistors would be required using a conventional op-amp implementation. The intermediate amplifier input consists of difference amplifier Q_3 and Q_4. Q_3 therefore performs a dual function. The supply and load rejection are greatly enhanced by providing a differential current error signal to the current differencing amplifier controlling the converter. R_4 provides frequency and offset compensation but does not alter the overall loop gain since $A_{\text{int}} \propto 1/R_4$ and A_2 is limited by $R_{\text{ai}} \approx \beta_4 R_4$. This circuit has the same performance as reported in Fig. 3.

The voltage followers $Q_1 - Q_2$ in the second topology in Figs. 2(c) and (d) reduce the offset from I_2 at the expense of greater overall intermediate amplifier complexity. The addition of V_{BE} scaling and appropriate control of bias current ratios converts the traditional circuit 2(c) into a bandgap reference in 2(d). A unity gain amplifier A_3 isolates I_1 from divider $R_1 - R_3$. Based on nodal analysis, the performance of circuit 2(d) is also described by (1). The measured transfer function for an implementation of this circuit using an MPQ3906 pnp array and a dual op-amp was similar to that shown in Fig. 3. The intermediate amplifier in circuit 2(d) must provide both current and voltage gain and is essentially a complete op-amp, for which the tradeoffs are well known.

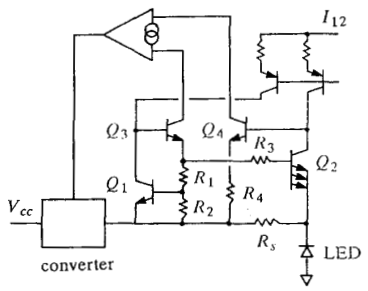


Fig. 6. Feedback circuit for biasing LED which further improves common mode rejection.

We have described two novel current regulator circuits which are ideal for many low voltage applications where voltage drops must be minimized. Simplicity and good performance are achieved by merging a bandgap voltage reference with an optimized error amplifier. As a result, only one compensated circuit is required. This approach is attractive for bipolar, CMOS, and BiCMOS IC implementations and can also be used effectively with commercial transistor arrays in prototype and discrete applications.

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