Low-Voltage Fully Differential Switched-Current Filters

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Abstract— **An accurate high-frequency switched-current integrator based on low-voltage fully-differential folded-cascode current copiers is presented. A five-pole lowpass ladder filter has been integrated using a 1.2 μm n-well CMOS process without floating precision linear capacitors. Experimental results show an accurate filter response for sampling frequencies up to 5 MHz. Using a nominal 3.3 V power supply, the measured dynamic range is 66 dB and the power dissipation is 10 mW/pole.**

I. Introduction

SINCE its introduction in 1988 [1], the current copier technique has been used in many applications including precision Nyquist rate [2] and oversampled data converters [3], [4], and video-rate finite-impulse-response (FIR) CMOS switched-current (SI) filters [5]. In first-generation SI infinite-impulse-response (IIR) filters [6], single-ended [7] and fully balanced [8] clocked current mirrors were used to implement the current-domain track-and-hold (T/H) function. Consequently, the measured frequency responses often exhibited passband droop and cutoff frequency errors. The deviations—as large as 20% in the single-ended versions—were traced to integrator quality factor (Q) errors owing to several factors including MOSFET mismatches, clock-feedthrough/charge-injection effects, and a design error that allowed signal-dependent nonsaturated operation of some current mirror devices [9].

Hughes *et al.* [10] subsequently suggested second-generation SI integrators [Fig. 1(a)] which used current-copier T/H stages [1], [11] to eliminate device mismatch effects. Single-ended folded-cascode current copiers [2] and regulated-gate-cascode (RGC) [12] copier-based SI integrators [Fig. 1(b)] [13] were developed to reduce channel-length modulation and capacitive coupling effects; fully differential integrators [4] and delay stages [5] were proposed to reduce clock-feedthrough/charge-injection effects. In Section II, we propose new fully differential folded- and regulated-gate folded-cascode copier-based SI integrators for precision low-voltage applications in standard digital CMOS technologies. Design considerations are described in Section III, and experimental results from low-voltage (3.3 V) low-pass prototypes integrated in a 1.2 μm CMOS process are presented in Section IV. Conclusions comprise Section V.

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II. Fully Differential Folded-Cascode SI Integrators

In addition to reducing device mismatch effects due to the incorporation of current copiers, the second-generation SI integrator [10] [Fig. 1(a)] has several other advantages: simplicity—it can be implemented using only 11 devices[1]; low-power operation—the total dissipation is $(2+K)IV_{dd}$; and low-voltage operation—$V_{dd} > (V_T + 2V_{\text{dsat}})$. It has several disadvantages. Most notably, the ratio of the input conductance (g_m) to the output conductance (g_{ds}) is relatively low due to channel-length modulation effects. Hence, significant errors in i_{out} occur due to loading effects and output voltage variations.

By using regulated-gate-cascode circuits [12] as in Fig. 1(b) [13], errors in i_{out} are reduced as the output conductance is reduced to $g_{ds}/(g_m/g_{ds})^2$. This approach, however, has several disadvantages: it is difficult to bias and maintain all MOSFET's in saturation; complexity—26 devices are required; high-power dissipation—the total power is $(2 + K)IV_{dd}$ plus the power required for the five common-source amplifiers used in the five RGC stages.

The single-ended folded-cascode copier-based SI integrator shown in Fig. 1(c) offers several advantages: high accuracy—the input/output conductance ratio is given by $(g_m/g_{ds})^2$ (although the output conductance is g_{ds}, the output current errors are negligible since the input conductance is increased to $(g_{ds})(g_m/g_{ds})^2$); input current range—the input current modulation index $(i_{\text{peak}}/I_{\text{bias}})$ over which the MOSFET's remain in saturation is increased considerably; simplicity—only 14 devices are required; low power—the total dissipation is $((2 + K)I + I_C)V_{dd}$; low-voltage operation—$V_{dd} > (V_T + 3V_{\text{dsat}})$.

The single-ended regulated-gate folded-cascode copier-based SI integrator shown in Fig. 1(d) offers higher accuracy—the input/output conductance ratio is given by $(g_m/g_{ds})^3$. Compared to the folded-cascode implementation of Fig. 1(c), its disadvantages are: higher complexity—it uses 18 devices; higher power—the total dissipation is $((2 + K)I + I_C)V_{dd}$ plus the power dissipation of two common-source RGC amplifiers; and higher minimum supply voltage—$V_{dd} > (2V_T + 3V_{\text{dsat}})$.

In order to minimize the total power dissipation and die area using a nominal 3.3 V power supply, and to reduce clock-feedthrough/charge-injection effects to maximize accuracy, we chose to develop fully differential filters based on the folded-

[1] Switches that carry currents are implemented as CMOS transmission gates, and switches that sample voltages onto MOSFET gates are implemented as pass transistors.

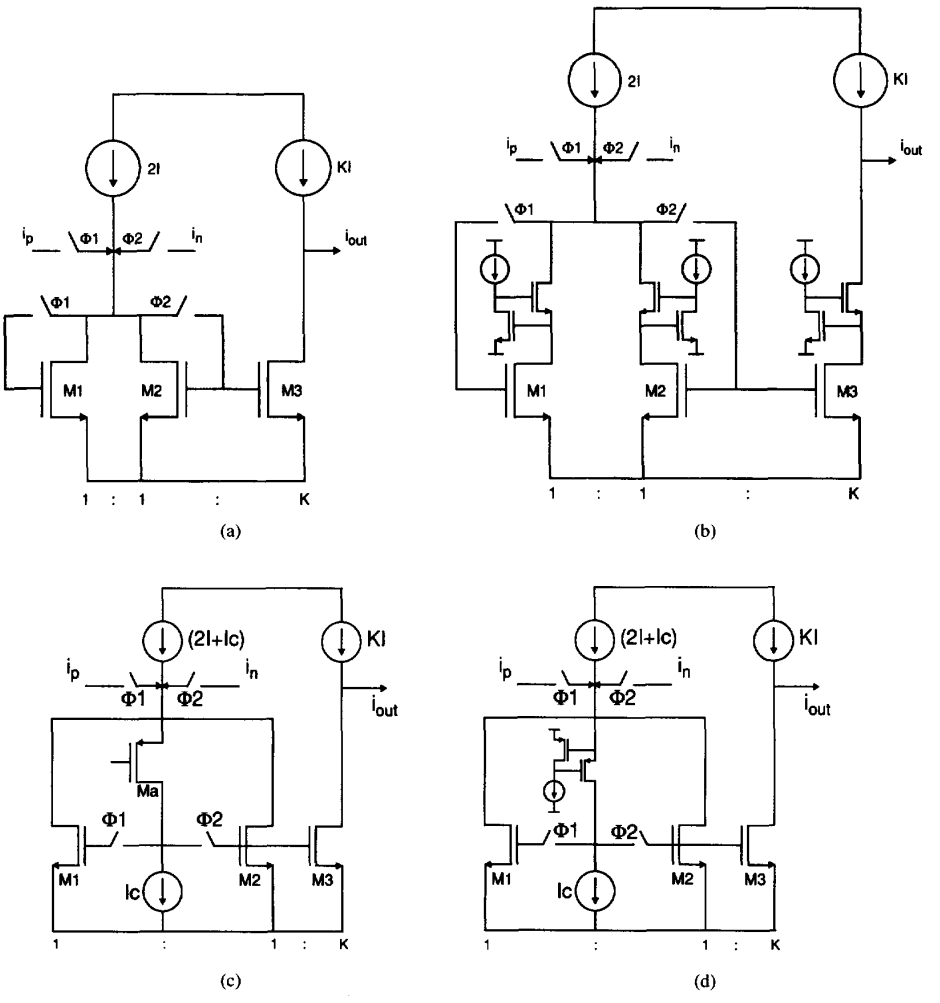


Fig. 1. Single-ended SI integrators based on (a) simple, (b) regulated-gate cascode, (c) folded-cascode, and (d) regulated-gate folded-cascode current-copiers, i_p and i_n represent positive and negative current inputs, respectively.

cascode SI integrator of Fig. 1(c). An attractive alternative, the regulated-gate folded-cascode copier-based SI topology, has been developed independently and used to implement SI filters, and to provide a direct comparison to the switched-capacitor approach for a commercial dual-tone multifrequency (DTMF) application [14].

A folded-cascode copier-based SI integrator using PMOS storage devices is shown in Fig. 2(a). As a result of the negative feedback loop around $M_1 - M_a(M_2 - M_a)$, the input impedance is low (typically 5–20 Ω), which facilitates input voltage-to-current conversion using on-chip polysilicon resistors characterized by low temperature and voltage coefficients of resistance. Note that the cascode stage is shared between the two copier stages to minimize area and power. In Fig. 2(a), with the input sampled during Φ_1 and output during Φ_2, the current "stored" by M_1 at the end of $\Phi_1(t - T/2)$ is

$$i_{M1}\left(t - \frac{T}{2}\right) = i_{\text{in}}\left(t - \frac{T}{2}\right) + i_{M2}(t - T). \tag{1}$$

At the end of phase $\Phi_2(t)$,

$$i_{M2}(t) = i_{M1}\left(t - \frac{T}{2}\right). \tag{2}$$

From (1) and (2),

$$i_{M2}(t) = i_{\text{in}}\left(t - \frac{T}{2}\right) + i_{M2}(t - T). \tag{3}$$

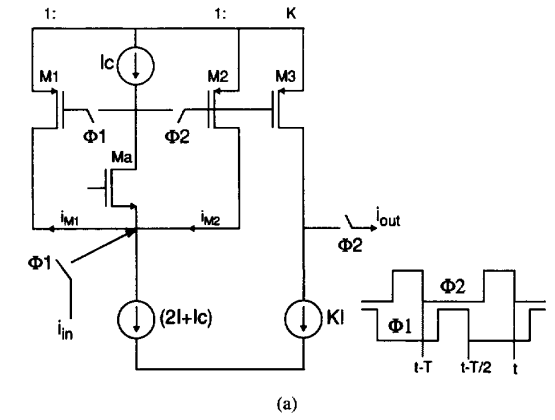
Taking z transforms,

$$i_{M2} = z^{-1/2} i_{\text{in}} + z^{-1} i_{M2} \tag{4}$$

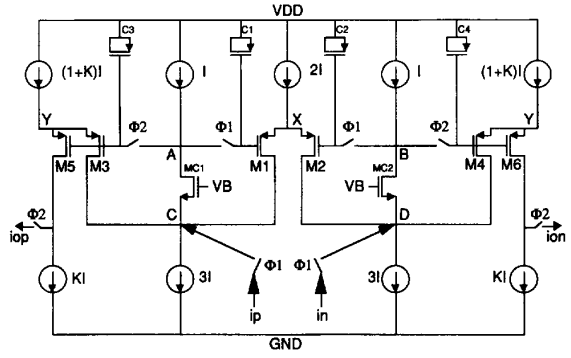
$$i_{\text{out}} = K i_{M2} = K\left(\frac{z^{-1/2}}{1 - z^{-1}}\right) i_{\text{in}}. \tag{5}$$

If the input and output are both sampled during Φ_1, then

$$i_{\text{out}} = K i_{M2} = K\left(\frac{z^{-1}}{1 - z^{-1}}\right) i_{\text{in}}. \tag{6}$$



(a)



(b)

Fig. 2. (a) Single-ended and (b) fully differential SI integrators using folded-cascode current copiers with PMOS storage devices (Note: The nodes labeled Y are connected together.)

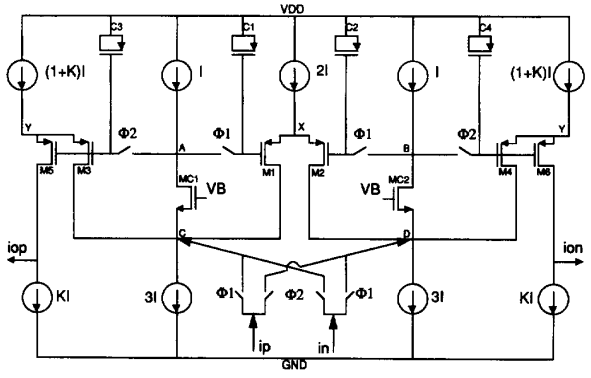
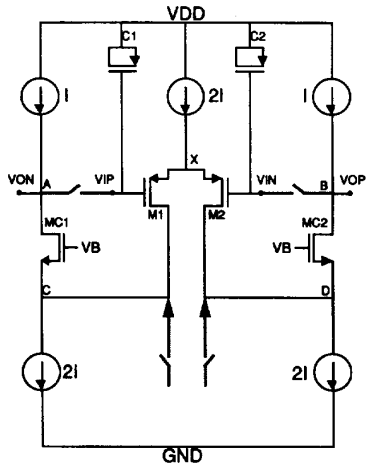


Fig. 3. A bilinear fully-differential SI integrator using folded-cascode current copiers with PMOS storage devices.

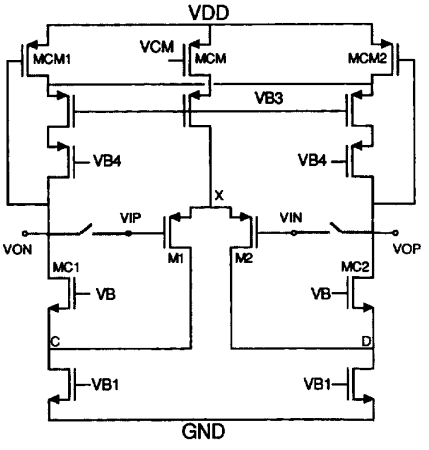
If the input and output are both sampled during Φ_2, then

$$i_{\text{out}} = Ki_{M2} = -K\left(\frac{1}{1-z^{-1}}\right)i_{\text{in}}. \tag{7}$$

Equations (5)–(7) show that half-, one-, and zero-delay integrators are realized by appropriate control of the clock cycles. If



(a)



(b)

Fig. 4. (a) A fully-differential folded-cascode opamp forms the core of the fully differential SI integrator. Either continuous- (b) or discrete-time common-mode feedback is required to maintain dc bias stability.

each memory transistor in the circuit of Fig. 2(a) is replaced by a differential pair, we obtain the fully differential SI integrator as shown in Fig. 2(b). The $+/-$ input and output currents are i_p/i_n and i_{op}/i_{on}, respectively. Noncritical MOSFET gate capacitances C_1– C_4 are added to reduce the common-mode clock-feedthrough/charge-injection effects and to optimize the closed-loop small-signal settling time [15]. The differential pair M_5– M_6 is used to generate scaled (K) differential current outputs. A common-mode feedback circuit (not shown) provides overall common-mode stability. The differential output currents obey the same sampling relationships as in (5)–(7). By sampling the positive and negative inputs during alternate clock phases as shown in Fig. 3, a fully differential bilinear SI integrator is obtained:

$$(i_{op} - i_{on}) = K\left(\frac{1+z^{-1}}{1-z^{-1}}\right)(i_p - i_n). \tag{8}$$

It is well known that the bilinear s-to-z transform has several important advantages, the most important one being that aliasing is avoided due to the one-to-one mapping of the $j\omega$ axis onto the unit circle [16], [17]. Moreover, due to the exact nature of the bilinear transformation, the filter bandwidth to sampling frequency ratio can be higher, allowing higher frequency filter realizations.

In fully differential circuits, the common-mode clock-feedthrough/charge-injection voltage is rejected by the input differential pair, in contrast to balanced circuits wherein the common-mode error voltages are converted nonlinearly into currents which are then subtracted at the outputs using current mirrors. The differential topology offers other important advantages such as increased common-mode (CMRR) and power-supply rejection (PSRR) ratios and increased dynamic range. A drawback is the required common-mode feedback network.

III. Integrator Design Considerations

The fully differential SI integrator of Fig. 2(b) can be viewed as two folded-cascode opamps [Fig. 4(a)] that share the folded-cascode output branches during the two clock phases. Consequently, its performance can be optimized by optimizing the opamp gain–bandwidth performance. It can be easily shown that the current flowing through the input transistor M_1 as a function of the differential input current i is given by

$$i_{M1} \cong \frac{\omega_0^2 i}{\omega_0^2 + 2k\omega_0 s + s^2} \tag{9}$$

where

$$\omega_0 = \sqrt{\frac{g_{mM1}}{C_1}\frac{g_{mMC1}}{C_{gsMC1}}} \tag{10}$$

$$k = \frac{1}{2}\sqrt{\frac{g_{mMC1}}{g_{mM1}}\frac{C_1}{C_{gsMC1}}}. \tag{11}$$

The minimum settling time (MST) condition [15] for the current to settle to within an error tolerance D of its final steady-state value is

$$D = \exp\left(\frac{-\pi k}{\sqrt{1-k^2}}\right). \tag{12}$$

For example, for a 0.1% settling error ($D = 0.001$), $k = 0.91$. The total capacitance C_1 needed to meet this condition is calculated using (11) and (12), and the MST is

$$t_s < \frac{\pi}{\omega_0\sqrt{1-k^2}} \tag{13}$$

which can be used to determine the maximum sampling frequency of the SI integrator. The common-mode feedback network used in this design is shown in Fig. 4(b) [18].

Active ladder filters maintain the low sensitivity to component variations characteristic of their passive doubly terminated LC prototypes [19]. Starting with an LC prototype that meets the desired frequency-domain specifications, a signal flow-graph is constructed [20], [21] and mapped into an SI filter [Fig. 5(a)] using the fully differential integrators described in the previous section. The integration constants K_i that determine the output stage scaling factors are given by

$$K_i = \frac{\omega_{co}}{f_s X_i} \tag{14}$$

where X_i is the passive component value of the ith branch, ω_{co} is the filter cutoff frequency, and f_s is the sampling frequency.

Dynamic Range Scaling: The dynamic range of an SI filter is defined as the ratio of the rms output current at a given total harmonic distortion (THD) level to the total rms noise current within a specified bandwidth. The THD generated by an SI integrator is determined by the input current modulation index ($i_{\text{signal}}/I_{\text{bias}}$) [9]. Similar to the scaling SC circuits, the dynamic range of an SI filter is maximized by scaling so that all integrators have the same modulation index.

For a typical SI filter implementation, $f_{co}/f_s = 1/20$. Hence, the integration constants are

$$K_i = \frac{2\pi}{20X_i} = \frac{0.314}{X_i}. \tag{15}$$

For most practical filter implementations, it is generally true that $X_i \geq 1$ and $K_i \leq 1$. Hence, to scale an SI filter for maximum dynamic range, the following procedure is followed.

1) Simulate the LC prototype to find peak values of the capacitor voltages and the inductor currents. This determines the bias current needed in the output branch [Fig. 5(a)] such that the modulation index is the same for all integrator output branches.

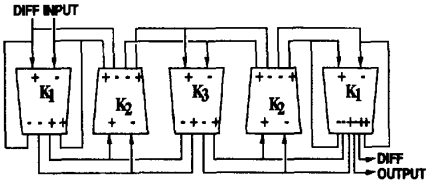
2) After the bias current in the output branch is determined, the core integrator cell [M_1, M_2, and I in Fig. 2(a)] is scaled by $1/K_i$.

3) An additional output branch is added to the last integrator to compensate for the insertion loss.

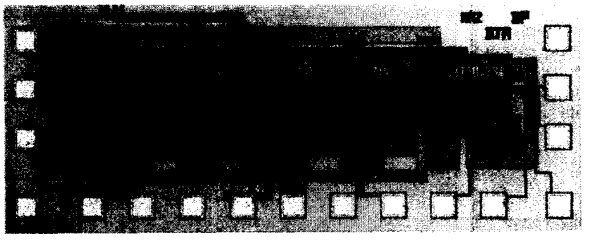
This scaling procedure illustrates an important difference between the SC and SI techniques. In SC filters, dynamic range is maximized by scaling capacitance ratios. Hence, the core operational amplifiers remain identical for all SC stages, which facilitates the computer-aided design and the layout of SC filters. SI filters require customization of each cell in both layout and design.

IV. Experimental Results

A die microphotograph of a five-pole fully differential SI low-pass ladder filter integrated in a 1.2 μm n-well CMOS process is shown in Fig. 5(b); the total active die area was 0.8 mm^2 [22]. To determine its viability for low-voltage operation, the filter uses a single 3.3 V power supply. With a sampling frequency of 5 MHz, the -3 dB cutoff frequency was designed for 280 kHz. The filter has a provision for comparing performance with and without input clock-feedthrough cancellation dummy switches. Nonoverlapping and overlapping clock signals are generated on-chip using static CMOS logic driven from an external master clock source. An overlapping clock phase is used to operate the dummy switches, and to open the sampling switches before the input current to individual cells is disconnected. All integrator output branches have current bypass paths to the supply when the output current is not being sampled, which prevents any



(a)



(b)

Fig. 5. (a) A fully differential five-pole low-pass ladder filter wherein each symbol represents an SI integrator scaling coefficient K_i. (b) A microphotograph of the 480 × 1800 μm die integrated using a 1.2 μm n-well CMOS process.

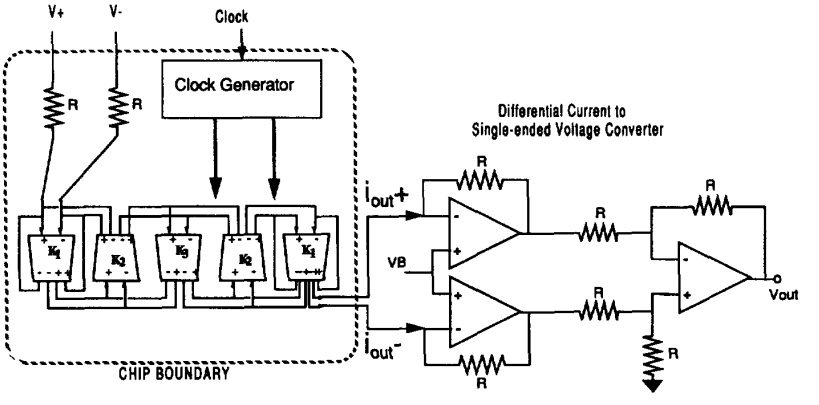


Fig. 6. The experimental setup showing the output off-chip I–V converter.

large voltage swings at the output nodes. The experimental test setup is shown in Fig. 6. The input voltage-to-current conversion was performed using on-chip polysilicon resistors, and the output voltage-to-current conversion was performed using off-chip circuitry. The measured frequency responses of the filter with and without clock-feedthrough cancellation are shown in Fig. 7. The detailed passband responses show that the 0.1 dB ripple Chebyshev response is accurately realized with and without dummy switches, indicating that clock-feedthrough cancellation is not required in the fully differential implementation. Measured passband responses for different clock rates ranging from 500 kHz to 20 MHz are shown in Fig. 8. In contrast to many previous SI filters, the measured responses are comparable in accuracy to the SC approach for clock rates up to 5 MHz. At higher clock rates, the passband errors increase because of incomplete small-signal settling in the folded-cascode opamp stages. Fig. 9 shows the measured passband responses for variations in the power supply voltage from 3.0 to 5.0 V. The small passband gain errors observed in the figure are comparable to those typically seen in SC implementations.

The measured THD of the five-pole low-pass filter as a function of the input current modulation index is shown in Fig. 10. The measured dynamic range, defined as the ratio of the rms input current at 1% THD to the total input-referred noise in the filter bandwidth, was 66.2 dB. Fig. 11 shows that within the filter passband, 80 dB CMRR is achieved. A complete summary of the filter performance characteristics is given in Table I.

V. Conclusions

A 3.3 V fully differential switched-current IIR filtering technique based on current copiers has been described. Experimental results from prototype low-pass filters are comparable in accuracy to switched-capacitor implementations. Thus, the

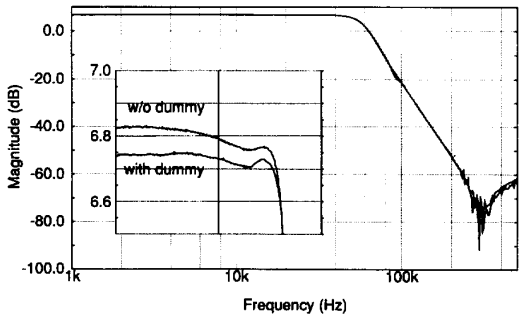


Fig. 7. A measured frequency response for the five-pole Chebyshev low-pass ladder filter of Fig. 5. The nominal passband ripple and ripple bandwidth are 0.1 dB and 50 kHz, respectively, with a 1 MHz sampling frequency. $V_{dd} = 3.3$ V.

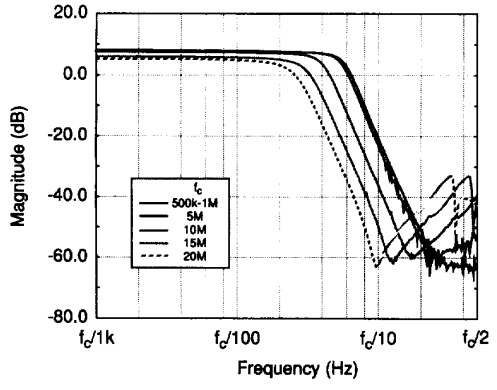


Fig. 8. Measured frequency responses for sampling frequencies from 500 kHz to 20 MHz. Since the frequency scale is normalized, the traces should ideally coincide. The deviations at high sampling rates are due to insufficient small-signal settling times. $V_{dd} = 3.3$ V.

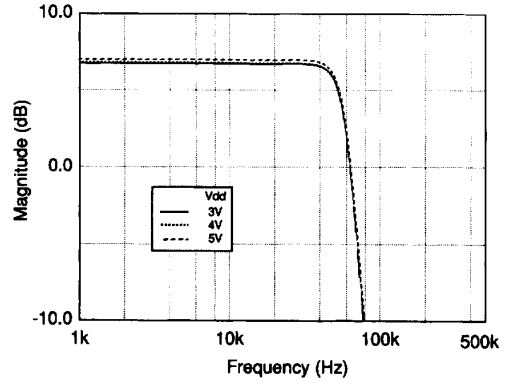


Fig. 9. Measured frequency responses for supply voltages ranging from 3.0 to 5.0 V with a 1 MHz sampling frequency.

fully differential SI filtering technique based on folded-cascode current-copier-based integrators is a viable option for precision high-frequency filtering using standard digital CMOS technologies.

TABLE I
SUMMARY OF THE MEASURED RESULTS FOR THE FIVE-POLE CHEBYSHEV FILTER

Clock Frequency	5 MHz
−3 dB Frequency	280 kHz
Passband Ripple	0.1 dB
CMRR (Passband)	80 dB
Input Impedance	16 Ω (dc-1 MHz)
I/p Noise Current	59.1 nA rms
Max. i/p Current (40 dB THD)	120 μA rms ($i_{\rm rms}/I_{\rm bias} = 0.6$)
Dynamic Range	66.2 dB
Power Supply	3–5 V
Power Dissipation	9–15 mW/pole
Die Area (Five Pole)	0.86 mm^2 (0.17 mm^2/pole)

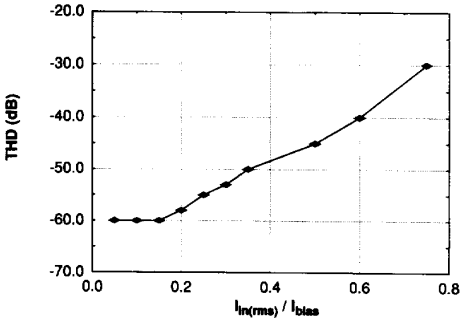


Fig. 10. Measured total harmonic distortion versus input current modulation index. The input frequency was 10 kHz with $V_{dd} = 3.3$ V.

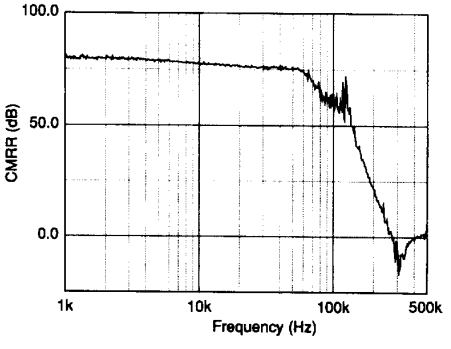


Fig. 11. Measured common-mode rejection ratio versus frequency. The modulation index for the common-mode input current was 0.5 with $V_{dd} = 3.3$ V.

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