Cell-Based Fully Integrated CMOS Frequency Synthesizers

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Abstract— **A family of standard cells for phase-locked loop (PLL) applications is presented. The applications are processed using a 1.5 μm, n-well, double-polysilicon, double-layer metal CMOS process. Applications include frequency synthesis for computer clock generation, disk drives, and pixel clock generators for computer monitors, with maximum frequencies up to 80 MHz. The synthesizers require no external components since the loop filter and oscillator are on chip with the phase ferquency detector and the charge pump. Special voltage and current reference cells are discussed. Analysis of noise sources in the PLL demonstrates the need for reducing the phase noise of the system. A low phase noise is achieved through supply rejection techniques and by placing the oscillator in a high-gain feedback loop to minimize its noise contributions. Laboratory measurements of completed silicon show synthesizers with exceptionally linear gain, as well as transient responses and phase noise similar to predicted results.**

I. Introduction

TO meet the requirements of computer and pixel clock frequency synthesizers, five key design goals are outlined. First, the PLL architecture must be fully integrated and include the oscillator and loop filter. Second, the maximum output frequency must be at least 80 MHz. Third, frequency synthesis with 50 kHz resolution is needed. This results in a phase detector input frequency on the order 140 kHz and forces the PLL bandwidth to be as low as 7 kHz (Fig. 1). Fourth, phase noise must be low, as dictated by the pixel clock applications for high-resolution computer monitors. This requires distinguishing between period jitter and low-frequency phase noise. Recently reported work [1], [2] in this area concentrates solely on reducing period jitter. Lastly, the circuit must be capable of performing in the noisy on-chip environment of mixed signal integrated circuits. Since these design goals produce a conflicting set of requirements, special design solutions are used. For example, the low PLL bandwidth necessary for high-resolution synthesis conflicts with the low phase noise specification. The low bandwidth also requires large loop filter time constants, which are difficult to realize on chip.

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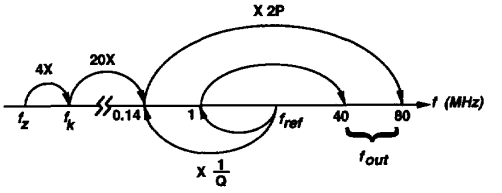

Fig. 1. Relationship of critical frequencies.

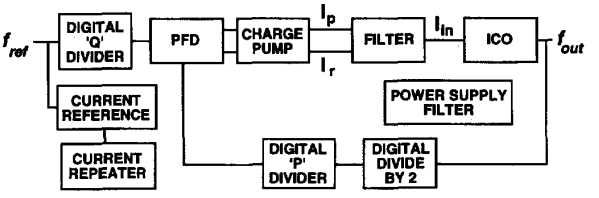

Fig. 2. PLL block diagram.

The basic PLL architecture is represented in Fig. 2. The output frequency is given by

$$f_{\text{out}} = f_{\text{ref}} \frac{2P}{Q} \tag{1}$$

where P is the modulus of the feedback counter, Q is the modulus of the input divider, and all frequencies (f_x) are in hertz (Hz). These digital dividers are constructed for each application using a digital cell library. The phase frequency detector (PFD), charge pump, loop filter, and current-controlled oscillator (ICO) can be modified depending on the desired output frequency range, frequency synthesis resolution, and loop bandwidth. Since the loop is actually a sampled time loop, and hand calculations are performed assuming a continuous time loop, the calculated design parameters are verified using a mixed mode behavioral simulator. Time domain simulation of the PLL is impractical using a purely analog circuit simulator. Behavioral simulations are performed using models written at the cell level, not the transistor level, and the high-frequency portions of the PLL are modeled digitally. This mixed-mode modeling greatly reduces the number of time steps that the analog portion of the simulation requires, and therefore offers run time savings of two to three orders of magnitude over transistor level simulations.

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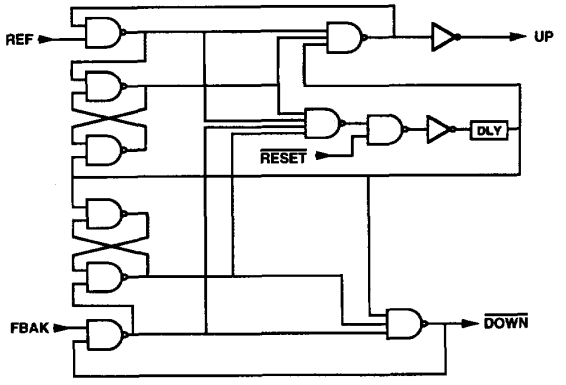


Fig. 3. Phase frequency detector block diagram.

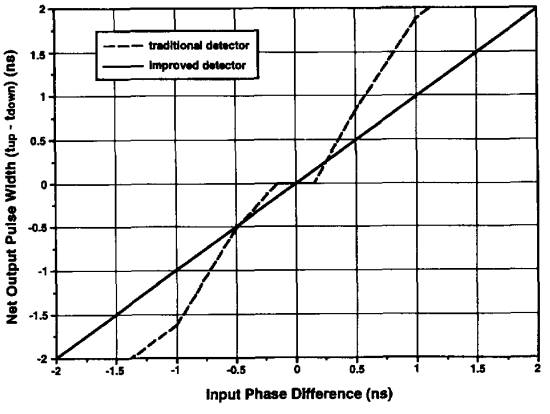


Fig. 4. Phase frequency detector transfer characteristic.

II. PLL Cells

The individual analog cells are designed and independently verified using a SPICE-like analog circuit simulator. Cell performance is simulated over process, voltage, and temperature variations (PVT). Process variations are simulated by using extracted and skewed models of the process. Supply voltage and temperature variations are typically specified to be between 4.5 and 5.5 V and from 0 to 70°C (T_A).

A. Phase Frequency Detector

The digital PFD is a type-four detector [3], [4], and is designed to eliminate the region of low gain near phase lock (Fig. 3). The elimination of this "dead zone" is accomplished by producing an "up" current pulse and a "down" current pulse during each cycle. In lock, both pulses are coincident and have a designed minimum width. The transfer characteristic of the PFD is shown in Fig. 4. One version of the detector can be held reset to allow switching between reference frequency sources without disturbing the loop.

B. The Charge Pump and Loop Filter

The charge pump cell [5] contains two charge pump circuits which are driven by the same digital signals, UP, DWN, and their complements (Fig. 5). These pumps produce two similar output currents, I_p and I_r. The current I_p drives the integrator portion of the loop filter, while I_r bypasses the integrator and provides a stabilizing zero in the transfer function [6]. These currents are on the order 1–10 μA, where the minimum charge pump current is limited by the switching speed requirement. In order to avoid the dead zone, the final current values must be reached during the UP/DWN pulse. By using these small current values, the loop filter can be placed on chip. However, careful design and layout techniques must be used to minimize the capacitive coupling, thereby reducing charge injection at the output of the charge pump. The voltage swing at the charge pump control inputs is the minimum swing required to completely turn off the switching devices. The output of the I_p charge pump is held at virtual V_{ref} by the amplifier in the loop filter. Since the output of the filter is held at V_{ref} by the operational transconductance amplifier (OTA) in the ICO and no dc current flows through $R3$ while the loop is in lock, the output of the I_r charge pump is also held at V_{ref}. In order to minimize unwanted charge transfer, nodes $DP1$ and $DR1$ are also held at V_{ref}. The third pole in the open-loop transfer function, which reduces ripple at the ICO input, is realized in the I_r path by $R3$ and $C3$. The resistor R_T accomplishes the voltage-to-current conversion required to drive the ICO.

The PLL open-loop gain is

$$A_{ol}(s) = \frac{K_i I_p}{2\pi 2P} \cdot \frac{1 + \left(R_3C_3 + \frac{I_r}{I_p}R_TC\right)s}{R_TCs^2(1 + R_3C_3s)} \tag{2}$$

where K_i, in rad/(A $\cdot$ s), is the gain of the ICO. In addition to two poles at the origin, this function exhibits a stabilizing zero at

$$f_z = \frac{1}{2\pi\left(R_3C_3 + \frac{I_r}{I_p}R_TC\right)} \approx \frac{1}{2\pi\frac{I_r}{I_p}R_TC}. \tag{3}$$

Making $I_r/I_p > 1$ helps reduce the on-chip size of components R_T and C. The third pole is located at

$$f_{p3} = \frac{1}{2\pi R_3C_3}. \tag{4}$$

The PLL bandwidth is found from $|A_{ol}(j2\pi f_k)| = 1$ as

$$f_k = \frac{K_i I_r}{4\pi^2 2P}. \tag{5}$$

The Bode plot of $|A_{ol}|$ is shown in Fig. 6.

C. The Current-Controlled Oscillator

The ICO consists of an OTA, a ring oscillator, a frequency-to-current converter, and a clean supply generator (Fig. 5). The ICO frequency range of one octave was chosen to be 40–80 MHz since all lower octaves can be obtained by means of digital division. A ring oscillator structure is used because of its high-frequency capability. However, from previous experience and first-order analysis, the noise in the ring oscillator is too high for these applications. Attempts to reduce the noise within the ring lead to unacceptably high penalties in power and size. The large transistor gate areas required

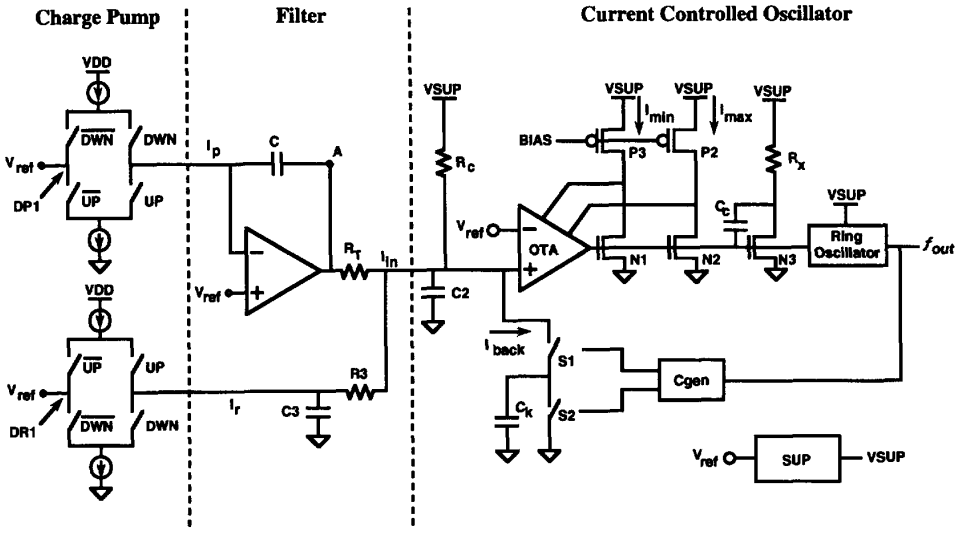


Fig. 5. PLL charge pump, loop filter, and current-controlled oscillator.

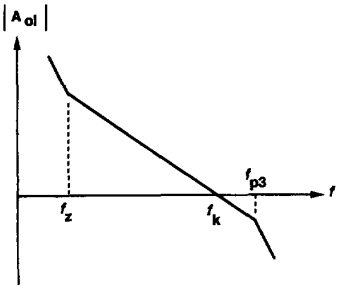


Fig. 6. Bode plot of PLL open-loop gain.

for low noise conflict with the high-frequency requirements. Therefore, the inherently high phase noise of the ring oscillator is suppressed by a high gain feedback loop in which the output frequency f_{out} is converted to current I_{back} and compared with the ICO input current I_{in}. The resistor R_c provides the center current to the ICO. The ring oscillator control current is limited to the range defined by $I_{\min}$ and $I_{\max}$. When the control current mirrored by $N2$ exceeds $I_{\max}$, the drain of $P2$ is pulled toward ground, turning on a device in the OTA which limits further increase in control current. A similar mechanism using $N1$ and $P3$ controls excessive decreases in control current. The components $N3, R_x$, and C_c compensate the ICO loop. The block SUP uses V_{ref} to generate a clean supply, $VSUP$, for the ICO.

The ring oscillator is a three-stage differential circuit [Fig. 7(a)]. The output of the third stage is converted into a single-ended signal by the differential to single converter, $D2S$, and subsequently ac-coupled to level shift and preserve a 50% duty cycle. Biasing circuitry for the ring oscillator and one stage are shown in Fig. 7(b). Transistors $N1, N2, N3, P1$, and $P2$ form the differential stage. The maximum voltage of the oscillator waveforms at OP and OM is limited by $P4$ and $P3$, respectively. Similarly, $N4$ and $N5$ limit the minimum voltage at these nodes. During their limiting action, these four devices conduct the variable control current. The gate voltages of these devices must vary with the control current to maintain the desired clamping levels. Transistor $P5$ conducts current proportional to the control current, and provides it to $P6$ which is matched to $P3$ and $P4$. The operational transconductance amplifier (OTAP) develops V_{tp1} needed to keep the source of $P6$ at V_{tp}. This value for V_{tp1} ensures that the maximum voltage at OP and OM is clamped at V_{tp} and is independent of the control current. Precision clamping is possible because $\partial V/\partial t = 0$ at peak values of the ring oscillator waveform. Since no current is delivered to capacitive loads at these instants, the peak voltage values are determined by transistor dc characteristics and bias voltages.

Clamping the waveform to constant amplitude does not eliminate the nonlinearity in the ring oscillator. As the control current increases, the voltage overdrive needed at IP and IM to switch the current increases. This results in an increased switching time at higher currents (frequencies) and would cause severe nonlinearity of the ring oscillator gain. Waveforms at IP and IM are linear during the transition through the switching region. Therefore, the switching time is proportional to the excess voltage V_{sat} of the switching transistor, $N2$ or $N3$. This excess voltage is a result of current $2I_{\text{control}}$ flowing through the device. It is assumed that the time lost in the switching process also tracks V_{sat}. Reducing the signal swing by an amount proportional to V_{sat} of the switching device compensates for this lost time. While $P6$ provides a constant clamping level, $N7$ is weaker than $N4$ and $N5$ such that the minimum voltage at OP and OM slightly increases as the control current increases. The result is a smaller waveform amplitude at higher control currents which compensates for a large portion of ring oscillator nonlinearity.

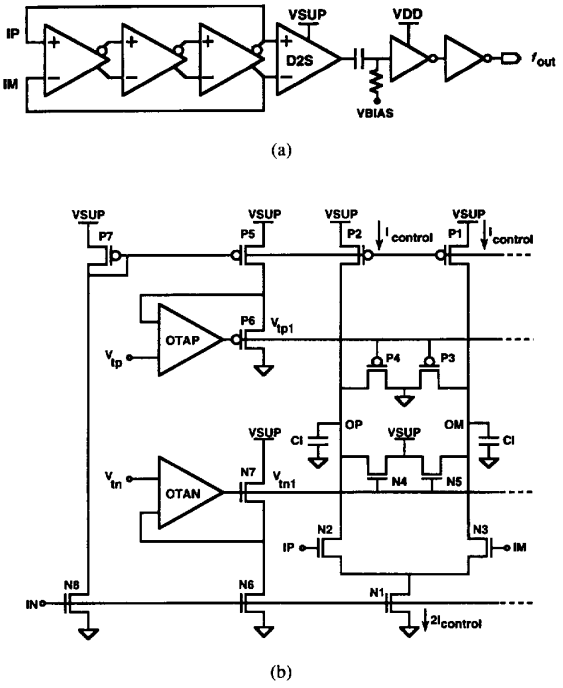


Fig. 7. (a) Ring oscillator. (b) Ring oscillator detail.

By using this variable clamping technique, the frequency and the gain of the ring oscillator from Fig. 7(a) and (b) are given by

$$f_{rng} = S\frac{I_{\text{control}}}{C_l(V_{tp} - V_{tn})} \tag{6}$$

and

$$G_{rng} = \frac{\partial f_{rng}}{\partial I_{\text{control}}} = \frac{S}{C_l(V_{tp} - V_{tn})} \tag{7}$$

where V_{tp} and V_{tn} track V_{ref} and S is a proportionality constant. The load C_l consists of 70% double poly capacitance and 30% parasitics. Simulations using I_{control} proportional to the product of V_{ref} and double polysilicon capacitance C_{dp} yield frequency variations of $\pm 3\%$ over PVT. The gain is verified by observing the product $G_{rng}V_{\text{ref}}C_{dp}$, which varies $\pm 11\%$ over the frequency range and PVT. While differential delay stages based on triode-biased loads [7], [8] are simpler and potentially faster, the resulting oscillator gain varies more over PVT and control current. At a given load current and voltage, the resistive component of a triode-biased load varies over PVT, changing the output waveform and stage delay.

Frequency-to-current conversion is accomplished by means of the switched capacitor resistor formed by $C_k, S1, S2$, and the nonoverlapping clock generator C_{gen} (Fig. 5). Two such converters, driven by opposite polarity clocks, are used in the actual circuit and their outputs are connected in parallel. Each converter contains switched capacitance $C_k/2$. This technique improves the stability of the ICO loop in two ways. First, the value of $C2$ needed for filtering of the switched current I_{back} is reduced by two. Since $C2$ is responsible for the lowest nondominant pole in the ICO loop, the frequency of that pole is increased by two. Second, the phase shift due to the digital nature of this loop is halved. The gain K_i of the ICO is a function of the feedback circuit, and is

$$K_i \equiv 2\pi\frac{\partial f_{\text{out}}}{\partial I_{\text{in}}} = \frac{2\pi}{C_k V_{\text{ref}}} \tag{8}$$

since $I_{\text{in}} + I_{RC} = f_{\text{out}}C_kV_{\text{ref}}$.

Evaluating the transfer function of the converter yields

$$K_f \equiv \frac{\partial V_{\text{out}}}{\partial f_{\text{in}}} = \frac{-C_kV_{\text{ref}}}{C_kf_{\text{out}} + \dfrac{R_c + R_T}{R_cR_T}} \approx -C_kV_{\text{ref}}\frac{R_cR_T}{R_c + R_T}. \tag{9}$$

Using (7) and (9) and selecting the size of $N3$ to conduct I_{control}, the unity-gain bandwidth of the ICO loop is

$$f_u = \frac{S}{2\pi}\cdot\frac{g_m}{C_c}\cdot\frac{R_cR_T}{R_x(R_c + R_T)}\cdot\frac{V_{\text{ref}}}{V_{tp} - V_{tn}}\cdot\frac{C_k}{C_l}. \tag{10}$$

Here, g_m is the transconductance of the OTA in the ICO. Resistors R_c, R_T, and R_x track each other, as do voltages V_{ref}, V_{tp} and V_{tn}. As previously mentioned, two thirds of C_l tracks C_k, leaving most of the bandwidth variations in the g_m/C_c term. The bandwidth of the ICO loop is therefore proportional to the bandwidth of the op amp, and is consequently well defined and nominally 1 MHz. The ICO loop introduces a pole into the main loop at approximately 1 MHz. Since this pole is well above the unity-gain bandwidth of the main loop, its impact on the stability of the latter is negligible. Noise generated within the ICO loop is suppressed by the open-loop gain. The OTA has a folded cascode configuration in order to provide high loop gain at low frequencies, which is important for the suppression of flicker noise.

Since each application may require different output frequency ranges, frequency synthesis resolution, and loop bandwidth, the loop parameters can be optimized by recalculating the I_r/I_p ratio, R_T, R_c, R_x, R_3, C_3 and C. In some cases, it may also be necessary to adjust the limiting currents I_{min} and I_{max}. The result of these recalculations is slight modifications of the charge pump, the loop filter, and the ICO.

III. Biasing Cells

In order to meet the low noise requirements, three cells are used to bias the PLL. Since frequency components in the power supply can modulate the ICO frequency, good supply rejection is crucial in achieving low phase noise. A two-pole low-pass filter cell with a cutoff frequency of 30 Hz is utilized (Fig. 8). The diodes represent appropriately connected MOS transistors. $D1 - D4$ are matched. $D5$ and $D6$ are matched, and their W/L is about 1000 times larger than the W/L of $D1 - D4$. The small current I_0 keeps all diodes in the subthreshold region. The high impedance of $D1$ and $D4$, along with C, determine the pole location. An OTA forces V_{back} to be equal to $VDD/2$. By virtue of diode matching, the output reference voltage is also $VDD/2$. Source and drain diffusions connected to V_{ref} and V_{back} have minimum areas, resulting in a worst case leakage current on the order 1 pA. This leakage current develops a voltage drop of only 0.4 mV

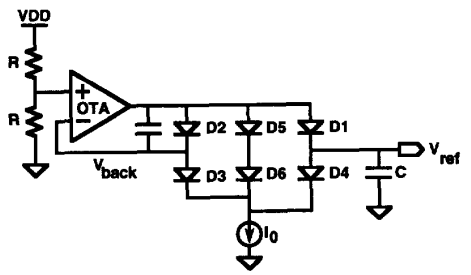


Fig. 8. Low-pass filter.

on the 400 MΩ impedance of these nodes. In addition, leakage phenomena at V_{ref} and V_{back} tend to cancel. Due to device characteristics in the subthreshold region, the variation of the current through $D1$ and $D4$ is larger than that of saturated transistors, resulting in a large but tolerable spread of the pole frequency. Two filter sections in series form the desired second-order filter. The low-pass filter solution is preferred to an untrimmed bandgap reference since the output voltage can be defined more accurately, resulting in a higher value of the clean supply voltage, $VSUP = 4.4$ V. The power supply filter does not provide protection below 30 Hz, but the open-loop gain of the PLL does. The loss of the PLL gain with increasing frequency is compensated by the increasing power supply rejection of the filter.

A current reference cell generates a bias current I_b proportional to V_{ref}, f_{ref}, and on-chip capacitance by means of a switched capacitor circuit similar to the one used in the frequency-to-current converter from Fig. 5. The bias current is then filtered and replicated in a separate cell and used in other cells as needed. The bias current is given by

$$I_b = C_b V_{\text{ref}} f_{\text{ref}} \tag{11}$$

where C_b is the value of the switched capacitor. Charge pump currents, I_p and I_r and frequency-limiting currents $I_{\min}$ and $I_{\max}$ are proportional to I_b. I_r is then

$$I_r = DI_b = DC_b V_{\text{ref}} f_{\text{ref}}. \tag{12}$$

D is a constant of proportionality.

Substituting (8) and (12) into (5) results in

$$f_k = \frac{D}{2\pi 2P} \cdot \frac{C_b}{C_k} \cdot f_{\text{ref}} \tag{13}$$

showing that f_k varies only with f_{ref} and the feedback counter modulus P. Limiting currents $I_{\min}$ and $I_{\max}$ result in ring oscillator frequencies $f_{\min}$ and $f_{\max}$ which are a function only of f_{ref} since the voltage and capacitance variations again cancel. This can be verified by inspecting (6) and (11). The worst case stability of the PLL occurs at the lowest f_k, i.e., when f_k is closest to f_z. At these very low frequencies, the impact of the third and other nondominant poles is negligible. Consequently, at low frequencies, the loop can be treated as a second-order system [5], [6] with a damping factor ξ, which can be represented as

$$\xi = \frac{1}{2}\sqrt{\frac{f_k}{f_z}}. \tag{14}$$

For $f_z = 3$ kHz, $f_k = 7$ kHz, and the worst case spread of the ratio f_k/f_z, the damping factor is 0.623.

IV. Noise Analysis

A noise source with frequency f_m causes frequency deviation Δf_{out} and phase deviation $\Delta\theta_{\text{out}}$ at the output of the PLL. They are related [4] by

$$\Delta\theta_{\text{out}} = \frac{\Delta f_{\text{out}}}{f_m}. \tag{15}$$

For example, if a noise source with an f_m of 10 kHz changes the frequency of a 50 MHz ICO by 0.02%, the resulting phase deviation is 1 rad, an unnacceptably high value. Low-frequency and high-frequency noise are different in terms of their origins, methods of suppression, and importance in various applications. Low-frequency phase noise is caused by power supply noise, random resistor and transistor thermal noise, and random transistor flicker noise. High-frequency phase noise is mainly due to digital switching, and can be considered as predominantly deterministic. High-frequency noise yields low values for $\Delta\theta_{\text{out}}$ due to large f_m. For instance, at frequencies above the PLL bandwidth, the power supply rejection is mainly provided by the op amps in the circuit. The PSRR of an op amp decreases at frequencies above its dominant pole, typically with the slope of -20 dB/dec. This results in Δf_{out} increasing in proportion to f_m. Therefore, $\Delta\theta_{\text{out}}$ does not increase due to the loss of PSRR in the op amps.

Period jitter, or edge-to-edge jitter, can be used to characterize the high-frequency noise. Period jitter is, in fact, a measure of the frequency deviation since

$$\frac{\Delta T_{\text{out}}}{T_{\text{out}}} = -\frac{\Delta f_{\text{out}}}{f_{\text{out}}} \tag{16}$$

holds for $\Delta f_{\text{out}} \ll f_{\text{out}}$. In combination with (15), this yields the relationship between the phase deviation and the period jitter as

$$\Delta\theta_{\text{out}} = -\frac{\Delta T_{\text{out}} \cdot f_{\text{out}}^2}{f_m}. \tag{17}$$

This suggests that it is meaningful to observe the phase deviation for low values of f_m and use the period jitter when f_m is large.

The fundamental method for the treatment of noise in PLL's and oscillators can be found in [4]. Accurate formulas for some cases of noise exist in [4] and [9]. However, these expressions cannot be applied to all cases required by this design. Therefore, accuracy is traded for insight by developing a set of simplified approximate expressions for the phase noise. The phase noise power spectrum density (PSD) at the output of the PLL in the open-loop configuration is given by

$$\phi_{ol} = G_{ol}^2(f_m) \cdot \phi_{\text{in}}(f_m) \tag{18}$$

where $\phi_{\text{in}}(f_m)$ is the voltage or current PSD of some noise source, $G_{ol}(f_m)$ is the modulus of the corresponding transfer function, and $f_m = \omega/2\pi$ is used as the variable, as is often

done in noise calculations. The output phase PSD with the loop closed is then

$$\phi_{\text{out}}(f_m) = \frac{\phi_{ol}(f_m)}{|1 + A_{ol}(j2\pi f_m)|^2} = \frac{G_{ol}^2(f_m)\phi_{\text{in}}(f_m)}{|1 + A_{ol}(j2\pi f_m)|^2} \quad (19)$$

where $A_{ol}(j2\pi f_m)$ is the PLL open-loop gain. The mean-square value of the phase noise is obtained by integrating

$$\overline{\theta_{\text{out}}^2} = \int_0^\infty \phi_{\text{out}}(f_m) df_m. \quad (20)$$

In order to simplify this integration, an approximation based on the Bode diagram from Fig. 6 is used:

$$\frac{1}{|1 + A_{ol}(j2\pi f_m)|^2} \approx \begin{cases} \dfrac{f_m^4}{f_z^2 \cdot f_k^2} & \text{for } f_m \le f_z \\ \dfrac{f_m^2}{f_k^2} & \text{for } f_z < f_m \le f_k \\ 1 & \text{for } f_m > f_k. \end{cases} \quad (21)$$

Besides the obvious inaccuracies at the segment boundaries, the approximation neglects the nondominant effects on the loop. This is justified by the very small device noise contribution at frequencies above 1 MHz. The infinite integration limit for $\overline{\theta^2}$ is kept for simplicity.

$G_{ol}^2(f_m)$ always contributes the term f_m^{-2} due to the frequency-to-phase transition at the output of the PLL. An additional f_m^{-2} terms exists if the noise is low-pass filtered with one pole close to the origin. Finally, in the case of flicker noise, $\phi_{\text{in}}(f_m)$ has a term f_m^{-1}. Therefore, most noise sources in this design result in an open-loop phase noise PSD at the PLL output of the form

$$\phi_{ol}(f_m) = C \cdot f_m^{-n}. \quad (22)$$

This result yields (23) at the bottom of this page. The integral I_n for $n = 2, 3, 4$ is then evaluated as

$$I_2 = \frac{2}{f_k}\left(1 - \frac{f_z}{3f_k}\right) \quad (24)$$

$$I_3 = \frac{1}{f_k^2}\left(1 + \ln \frac{f_k}{f_z}\right) \quad (25)$$

and

$$I_4 = \frac{2}{f_k^3}\left(\frac{f_k}{f_z} - \frac{1}{3}\right). \quad (26)$$

For values of $n > 4$, the integral I_n does not converge.

The most pronounced noise source is the flicker noise generated by the OTA in the ICO, and is mainly due to the noise in the differential pair and load devices. This noise source can be represented as an equivalent voltage source in series with the negative input terminal of the OTA, and has the following transfer function to the PLL output phase:

$$G_{ol}^2(f_m) = \frac{\left[f_{\text{out}} + \dfrac{(R_c + R_T)}{C_k R_c R_T}\right]^2}{V_{\text{ref}}^2} \cdot \frac{1}{f_m^2} = \frac{B}{f_m^2}. \quad (27)$$

The input noise PSD takes the form

$$\phi_{\text{in}}(f_m) = \frac{A}{f_m} \quad (28)$$

and the open-loop output phase PSD becomes

$$\phi_{ol}(f_m) = \frac{AB}{f_m^3}. \quad (29)$$

The expression for $\overline{\theta^2}$ can be written directly as

$$\overline{\theta^2} = \theta_{\text{rms}}^2 = ABI_3 = AB\frac{1}{f_k^2}\left(1 + \ln \frac{f_k}{f_z}\right). \quad (30)$$

Substitution of numerical values with $f_k = 15.57$ kHz (midrange) results in $\theta_{\text{rms}} = 3.3°$ versus the simulated result of 3.1°. To aid the suppression of noise, the OTA is designed with large area transistors which, as previously stated, are impossible to use inside the high-frequency ring oscillator.

The PSD of the noise current injected into the ICO input by the centering resistor R_c is $\phi_{\text{in}} = 4kT/R_c$, and the corresponding output phase PSD becomes

$$\phi_{ol}(f_m) = \frac{4kT}{R_c} \cdot \frac{K_i^2}{4\pi^2} \cdot \frac{1}{f_m^2}. \quad (31)$$

Since (31) is of the form f_m^{-2}, I_2 is used:

$$\overline{\theta^2} = \frac{4kT}{R_c} \cdot \frac{K_i^2}{4\pi^2} \cdot \frac{2}{f_k}\left(1 - \frac{f_z}{3f_k}\right). \quad (32)$$

θ_{rms} is calculated to be 0.62°, and simulation of θ_{rms} yields 0.59°.

In some PLL designs [1], [2], the gain of the oscillator is purposely made low in order to reduce the noise due to other PLL components. The resulting reduction of the frequency control range usually requires a coarse control of the center frequency. This approach is justified if the oscillator is not the dominant noise source, and if the mechanism defining the center frequency has better noise performance than the rest of the PLL. Neither is the case in this design; therefore, this approach is not used.

It should be noted that defining the center current of the ICO with a transistor current source increases θ_{rms} of the PLL three to five times. Flicker noise in that and other devices in the bias chain is eliminated when a resistor is used. Additionally, the thermal noise current PSD of the transistor is about five times larger than that of the resistor for device parameters within the design limits.

The thermal noise generated by the $R_F = 400$ MΩ output impedance of the VDD filter also deserves attention. The second filter section generates a white PSD which is subjected to a single pole roll-off at $f_p = 30$ Hz:

$$\phi_{\text{in}}(f_m) \approx 4kTR_F\frac{f_p^2}{f_m^2}. \quad (33)$$

$$\overline{\theta_{\text{out}}^2} = \int_0^\infty \phi_{\text{out}}(f_m) df_m = C\left(\int_0^{f_z} f_m^{-n} \cdot \frac{f_m^4}{f_z^2 \cdot f_k^2} df_m + \int_{f_z}^{f_k} f_m^{-n} \cdot \frac{f_m^2}{f_k^2} df_m + \int_{f_k}^\infty f_m^{-n} df_m\right) = CI_n \quad (23)$$

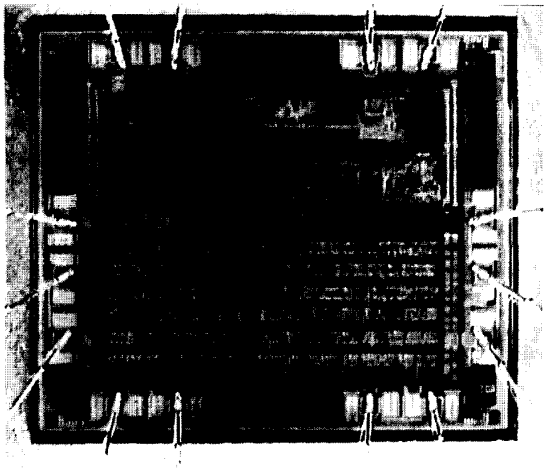


Fig. 9. Photomicrograph of a cell-based PLL application.

By taking into account the impact of V_{ref} on V_{sup}, the ICO, and the loop filter, $G_{ol}^2(f_m)$ is found to be

$$G_{ol}^2(f_m) = \frac{(f_c - f_{\text{out}})^2}{V_{\text{ref}}^2} \cdot \frac{1}{f_m^2} \tag{34}$$

where f_c is the center frequency of the ICO and f_{out} is the ICO output frequency. Since ϕ_{ol} contains an f_m^{-4} term, this case calls for I_4:

$$\overline{\theta^2} = 4kTR_F f_p^2 \frac{(f_c - f_{\text{out}})^2}{V_{\text{ref}}^2} \cdot \frac{2}{f_k^3}\left(\frac{f_k}{f_z} - \frac{1}{3}\right). \tag{35}$$

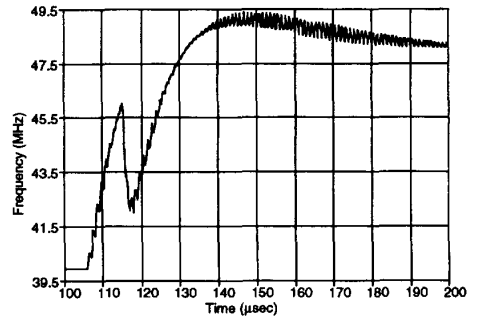
This expression yields $\theta_{\text{rms}} = 0.063°$ versus a simulated 0.057°.

The remaining noise sources are analyzed using the same approach. Transistor switches $S1$ and $S2$ in the ICO only contribute sampled thermal noise since their flicker noise is heavily attenuated in the linear region of operation. The contribution of the sampled thermal noise can be modeled with a resistor

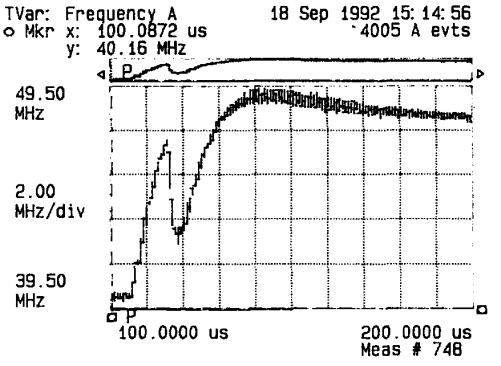
$$R \propto \frac{1}{C_k f_{\text{out}}} \tag{36}$$

connected between the ICO input and ground. The resulting phase noise is lower than that due to R_c or R_T. Sampled noise calculation principles can be found in [10]. The op amp and voltage-to-current conversion resistor are the main noise contributors in the loop filter (Fig. 5). Therefore, the op amp is designed for low noise. Charge pump noise is negligible due to the very low output duty cycle when the loop is in lock.

Contributions of all noise sources are calculated, and then simulated using a special transistor level noise model of the PLL developed in support of this design. Individual noise sources are modeled at the transistor level and linked to the ideal, noise-free model of the PLL by means of dependent voltage and current sources. Discrepancies between analytic expressions and simulation for this design are within 28% for $\overline{\theta^2}$ and 14% for θ_{rms}. While the simulation results are accurate for a limited number of points within the multidimensional parameter space, analytic expressions provide orientation and enable decision making at early stages of the design.



(a)



(b)

Fig. 10. Simulated versus measured transient step response of PLL.

V. Results

Five applications are complete. A photomicrograph of one of the applications containing a frequency synthesizer is shown in Fig. 9. The analog area of the chip is approximately 2.36 mm^2. Characterization is performed in both the time and frequency domains. Measured PLL behavior is close to the predicted values in all cases. The measured frequency step response (Fig. 10) is very similar to the response predicted by simulation. Samples from a production lot of silicon demonstrate that the gain of the ICO is exceptionally linear and slightly higher than predicted, but well within the specification. The measured transfer characteristic of Fig. 11 depicts the lot mean, with the error bars representing one standard deviation of the data. These measurements are accomplished by observing the voltage at node A (Fig. 5) for a number of programmed output frequencies. Seen from node A, the oscillator behaves like a voltage-controlled oscillator (VCO).

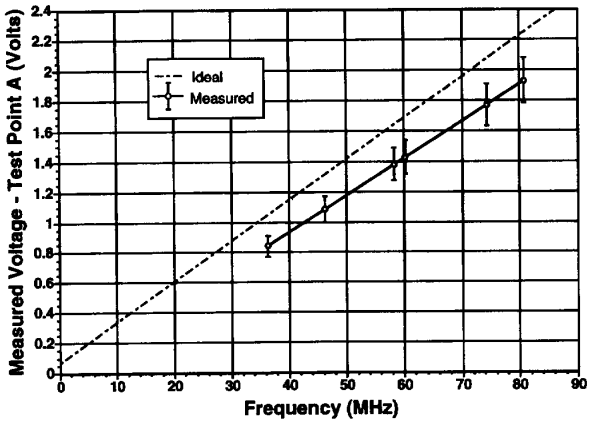


Fig. 11. VCO transfer characteristic: measured versus ideal.

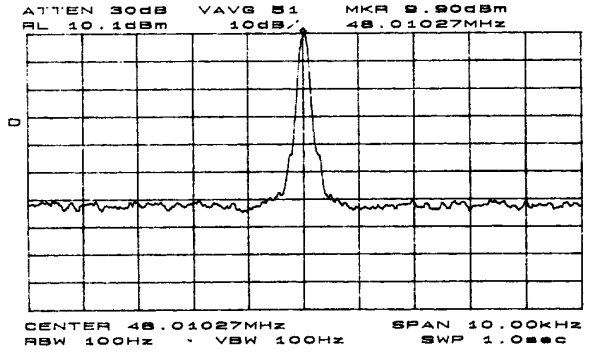


Fig. 12. Spectral analysis of synthesized frequency.

TABLE I
SUMMARY OF PLL FUNCTIONALITY AND PERFORMANCE

Maximum output frequency	80 MHz
Reference frequency	14MHz–18MHz
Frequency programming resolution	~0.1%
PLL bandwidth	7kHz–26kHz
Loop filter	Internal
DC power dissipation	30 mW
Total power dissipation (f_{out} =80 MHz, C_{load} = 25 pF)	125 mW
Period jitter	100 ps
Phase noise (Bandwidth dependent)	4°–7.5° rms

The phase noise and period jitter are measured using a time interval analyzer. The low-frequency phase noise is a combination of flicker and thermal noise. Measurements yield rms values between 4° and 7.5°, depending upon the actual PLL bandwidth. The period jitter is measured at 100 ps. The results of the spectral analysis are shown in Fig. 12. For a summary of results, see Table I.

VI. CONCLUSIONS

The development of a family of standard cells for PLL applications has been presented. The loop cells, which include the PFD, the charge pump, the filter, and the ICO, are all on chip and are designed to reduce phase noise and process parameter dependence. If necessary, the loop characteristics can be adapted to each application with a minimum of modifications to these cells. Three biasing cells: a power supply filter, a capacitive bias generator, and a current repeater, supplement the loop cells. Because the applications using these PLL's require low phase noise, special emphasis is placed on the analysis of the noise sources and their contributions to the overall noise performance of the PLL. Results from laboratory measurement of completed silicon are consistent with hand calculations and both behavioral and transistor level simulations.

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