Special Brief Papers

3.3-V BiCMOS Circuit Techniques for a 120-MHz RISC Microprocessor

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Abstract— **This paper describes 3.3-V BiCMOS circuit techniques for a 120-MHz RISC microprocessor. The processor is implemented in a 0.5-μm BiCMOS technology with 4-metal-layer structure. The chip includes a 240 MFLOPS fully pipelined 64-b floating point datapath, a 240-MIPS integer datapath, and 24KB cache, and contains 2.8 million transistors. The processor executes up to four operations at 120 MHz and dissipates 17 W. Novel BiCMOS circuits, such as a 0.6-ns single-ended common base sense amplifier, a 0.46-ns 22-b comparator, and a 0.7-ns path logic adder are applied to the processor. The processor with the proposed BiCMOS circuits has a 11%–47% shorter delay time advantage over a CMOS microprocessor.**

I. Introduction

BiCMOS circuits using 0.5-μm BiCMOS technology have been applied to a 120-MHz microprocessor at 3.3-V power supply [1]. The processor includes an integer datapath, a fully pipelined 64-b floating point datapath, a 16KB data cache, an 8KB instruction cache, translation lookaside buffers, and control units. The chip can execute up to four operations at 120 MHz [2]. The adder and multiplier in the floating point datapath are fully pipelined at 120 MHz independently, and the resulting peak performance is 240 MFLOPS. Power dissipation of the chip is 17 W.

The three concepts behind the proposed high speed circuit techniques at low voltage implemented in the microprocessor are summarized as follows. There are a number of heavy load paths in a microprocessor, and these become critical paths that determine chip performance. To achieve high speed characteristics under heavy load conditions without increasing circuit area, low voltage swing operation of a circuit is effective. By exploiting the high conductance of a bipolar transistor, instead of using an MOS transistor, low swing operation can be achieved. This first concept is applied to a single-ended common-base sense circuit with small swing data lines in the register file of a floating point datapath and an integer datapath. The second concept is using BiCMOS circuits which have higher driveability than CMOS circuits when the area sizes of each circuit are equal. But, for this, a severe problem is encountered under low supply voltage where the voltage drop by V_{be} of the bipolar transistors degrades the speed performance of the next circuits connected to the BiCMOS circuits. Then in the second concept, the voltage drops by V_{be} are overcome by addition of a pull up PMOS to the BiNMOS logic gate to ensure the circuits have full swing operation. The third concept uses the functions of bipolar circuits, such as their emitter coupled circuit technique. These are applied to a multi-input comparator circuit in the translation lookaside buffers.

The effects of these proposed BiCMOS circuits on microprocessor performance are evaluated in this paper. The BiCMOS circuits offer several advantages over CMOS circuits in a microprocessor operated at 3.3 V.

TABLE I
0.5-mm BiCMOS Technology

Emitter Size	0.6 μm × 4.0 μm
h_{FE}	100
f_T	15 GHz
L_{eff}	0.45 μm
T_{ox}	9 nm
Metal 1, 2, 3	2 μm/pitch
Metal 4	4 μm/pitch
Supply voltage	3.3 V

II. BiCMOS Process Technology

The processor is implemented in 0.5-μm BiCMOS technology. The effective gate length of the MOS transistor is 0.45 μm and the thickness of the gate oxide is 9 nm. Design of the MOS transistor is very important, because circuit performance strongly depends on it. Bipolar transistors are combined in the internal circuits with fast MOS transistors, so high performance bipolar transistors are necessary. Cut off frequency of the bipolar transistors must be 15 GHz.

A 4-metal-layer structure is adopted to achieve high integration. The first metal layer is used for internal wiring in the cells and the other three metal layers are dedicated to global wiring such as signal lines, source/ground lines, clock distribution lines and some kinds of buses.

The chip contains 2.8 million transistors and operates at 120 MHz. Therefore, a low supply voltage (3.3 V) is adopted to reduce power dissipation of the chip. The 0.5-μm BiCMOS technology is summarized in Table I.

III. Macrocell Architecture

The processor includes an integer datapath, a fully pipelined 64-b floating point datapath, a 16KB data cache, an 8KB

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Fig. 1. Chip microphotograph.

TABLE II
PROCESSOR CHARACTERISTICS

Clock frequency	120 MHz
Peak performance	240 MIPS
	240 MFLOPS
Floating latency	
Adder	4 cycles
Multiplier	4 cycles
Divider	19 cycles
Power dissipation	17 W

instruction cache, translation lookaside buffers, an instruction control unit, and memory interface unit. The chip microphotograph is shown in Fig. 1. The integer datapath has two ALU's, two shift/merge units, and a branch adder. The register file has 4-read ports, 3-write ports, and 32 b × 32 word registers. It executes two instructions every cycle. The floating point datapath consists of an adder, a multiplier with radix-4 Booth's algorithm and Wallace tree, and a divider with radix-4 SRT. Their latencies are 4, 4, and 19, respectively. The floating point register file has 4-read ports, 3-write ports, and 64 b × 32 word registers. It executes two floating point instructions every cycle. The characteristics of the processor are summarized in Table II.

A block diagram of the floating point datapath and cache memory is shown in Fig. 2. There are four main critical paths in the blocks and BiCMOS circuits are applied to them. They are 1) Adder path, 2) Multiplier path, 3) Divider path, and 4) Register read path. BiCMOS circuits are used in most of the blocks, except the cache memory cell and register cell blocks. Bipolar transistors are useful for saving area in circuits with high driveability, as mentioned in Section IV. But for the circuits without high driveability, MOS transistors are better for saving macrocell area. As it is necessary to minimize the

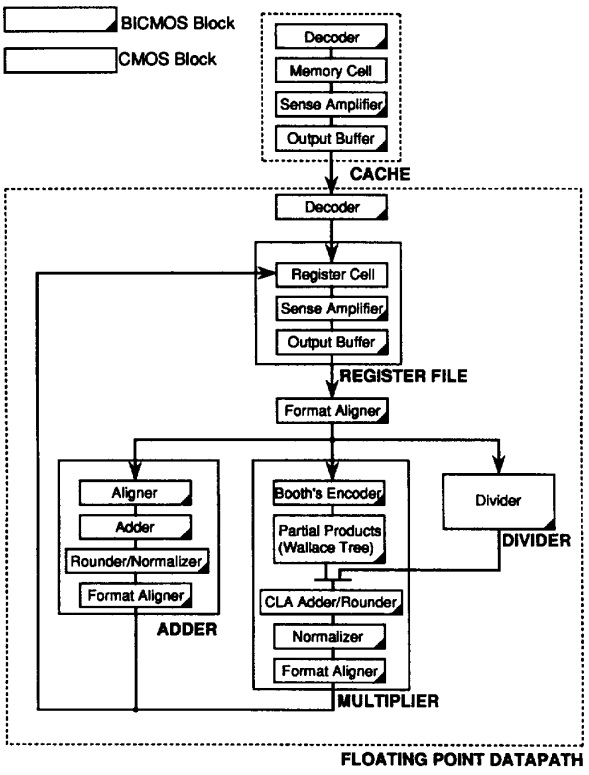

Fig. 2. Floating point datapath and cache block diagram.

number of BiCMOS circuits to save area, they are used only in the critical paths. Bipolar transistors are applied to 20% of the circuits in each block.

BiCMOS buffers with high driveability are effectively used in blocks which have many fanouts and long wires such as decoders, output buffers, and Booth's encoder. BiCMOS circuits which consist of BiCMOS buffer circuits and CMOS logic circuits, including latches, are properly used instead of power-CMOS circuits in other blocks. To access the data from the memory cell and the register cell blocks, BiCMOS circuits are used which have low swing operation due to the high conductance of bipolar transistors such as in the sense amplifier circuit. Bipolar differential amplifier circuits are applied to the cache and bipolar common-base sense circuits are applied to the register file of the floating point datapath. BiCMOS circuits are also used in the translation lookaside buffer. In the TLB block, BiCMOS circuits are used most effectively in the chip, because the TLB critical path has more bipolar circuits than the other critical paths. The BiCMOS circuits include a bipolar differential sense amplifier circuit and a multi-input comparator with an emitter coupled bipolar circuit.

IV. CIRCUIT IMPLEMENTATION

A. Basic Gates

Three types of gates are evaluated here, a standard CMOS gate, a power CMOS gate, and a BiNMOS gate. The power

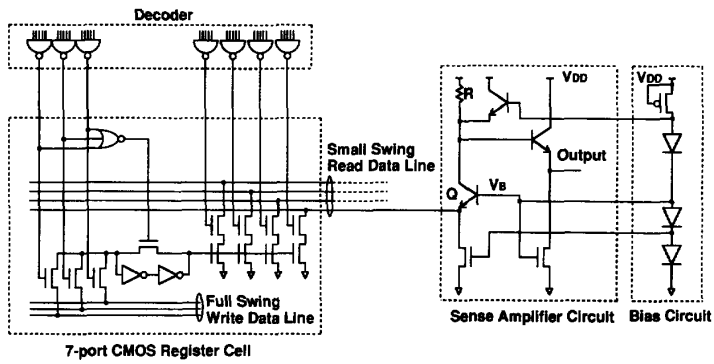

Fig. 3. Register file with single-ended common-base sense circuit.

TABLE III
CELL SIZE

Cell	Standard CMOS	Power CMOS	BiNMOS
Cell area size ratio	1.0	2.0	2.0
Channel width ratio (P/N)	1.0/1.0	1.7/2.6	1.0/2.0

CMOS and BiNMOS gates are designed to have higher driveability than the standard CMOS gate. As supply voltage is reduced from 5 to 3.3 V, the BiNMOS gate is used instead of the totempole type BiCMOS gate, because the former is superior at low voltage [3]. A comparison of cell size and MOS channel width of the CMOS and BiNMOS 3-input gate circuits are shown in Table III. The channel width of the power CMOS gate is the largest. The delay time is estimated by circuit simulations using 3NAND gates at 3.3 V. The delay time dependency of the BiNMOS gate on capacitance load is 31% of the standard-CMOS gate and 67% of the power-CMOS gate. There is an advantage using BiNMOS gates instead of power-CMOS gates, because the former have higher driveability when the cell area size of both types is equal. On the other hand, as the difference in delay time of the BiNMOS and standard-CMOS gates is small in the light capacitance load region, the standard-CMOS gates are used in most of the logic units in the chip to save area. The cell library of the chip consists primarily of standard-CMOS circuits and BiNMOS circuits. The power-CMOS circuits are only used in some of the clock drivers which are required to balance performance of rising and falling times of the circuits.

B. Register File

A multiport register file is needed in a superscalar microprocessor for parallel execution. To realize a small multiport register file cell, a single-ended bit line is used [4]. The register file with the proposed single-ended common-base sense circuit is shown in Fig. 3. Small signal operation is possible by exploiting high conductance of the bipolar transistor, which shortens access time of the circuit. The voltage amplitude of the read data line ΔV is 100 mV and it is amplified to 1.6 V by the sense circuit. When the word length of the register file is 32, the access time from the read address to the output of the sense circuit is 0.6 ns and power dissipation is 2.0 mW at 3.3 V. As the proposed sense circuit exploiting high conductance of the bipolar transistor retains high speed characteristics below 3.3 V, it should be applicable to a sub-3.3 V processor in the future. The bias voltage V_B of the bipolar transistor Q in the sense amplifier circuit is constant when the source voltage V_{DD} changes, because V_B is determined from the ground by the bias circuit. As the operating characteristic of the sense amplifier circuit depends on V_B, the dependence of the access time of the circuit on supply voltage is very small.

The dependency of the characteristics of the sense amplifier circuit on temperature is small. As the bias voltage V_B of the base of the bipolar transistor which is determined by the bias circuit has negative dependency on temperature, the collector current of the bipolar transistor decreases when the temperature increases. On the other hand, the load resistance R has positive dependency on temperature. As the dependency effects of resistance and collector current are cancelled when temperature changes, the voltage amplitude of the output does not depend on temperature.

The sense amplifier circuit is sensitive to noise of the data line. The largest data line noise is the coupling noise propagated from adjacent full swing data lines. Therefore, the layout design of the register file must be carefully made to achieve high tolerance.

C. Multi-Input Comparator Circuit

A multi-bit comparator circuit which is applied to hit check of the translation lookaside buffers is shown in Fig. 4. The 22-b comparator circuit can be made up with just 2 stages by using the wired-OR bipolar transistors. When all the bits match, as no transistor is on, output is normally high. There is no dc current in this case. When only data mismatch occurs, the corresponding bipolar transistor with the mismatch bit turns on and output becomes low. High speed characteristics are achieved because the delay time of the circuit only depends on fall time of the output which is accelerated by the bipolar transistors. The delay time of the 22-b BiCMOS comparator is 0.46 ns at 3.3 V.

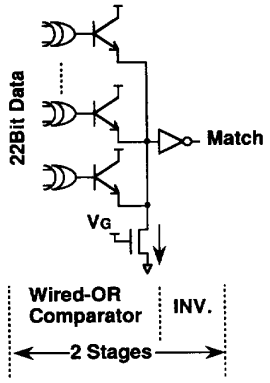

Fig. 4. Twenty-two bit comparator circuits for TLB.

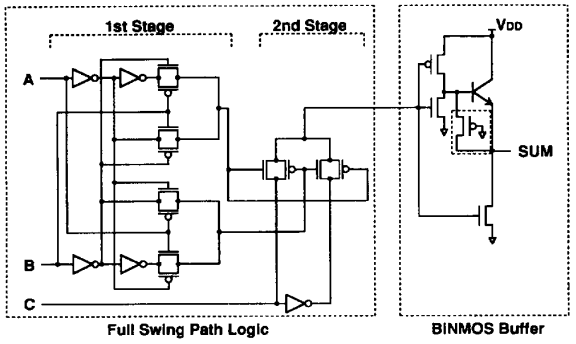

Fig. 5. Adder circuit for multiplier.

D. Path Logic Adder

The full swing path logic adder is connected to the BiNMOS buffer to drive heavy loads fast (Fig. 5). But the high level of the output signal of the conventional BiNMOS buffer is limited to V_{DD}-V_{BE}. This output voltage drop degrades the performance of the next gate. When the 3-input NAND CMOS gate is driven by the conventional BiNMOS gate, the operating speed of the CMOS gate is degraded 36% by the voltage drop. So it is important to connect the PMOS transistor between the base and emitter of the bipolar transistor for full swing operation. This type of full swing BiNMOS gate is applied to all units of the proposed processor.

V. Evaluation

The BiCMOS circuits proposed in Section IV are applied to a floating point datapath, an integer datapath and translation lookaside buffers. Five critical paths including a multiplier, an adder, a divider, a register file and TLB are evaluated. BiNMOS buffers are applied to all these five critical paths instead of power-CMOS gates. The BiCMOS common-base sense amplifier circuits are used in the register file in both the floating point datapath and integer datapath. The path logic adder circuit with BiNMOS buffer is applied to the multiplier in the floating point datapath. The multi-input BiCMOS comparator circuit is used in the TLB path. First, comparison of the delay times of BiCMOS and CMOS circuits is summarized in Table IV. The CMOS circuits are designed with an area size equal to that of the BiCMOS circuits. The delay time of each BiCMOS circuit is 30%–83% the delay time of the CMOS circuits. The delay times of the critical paths using the proposed BiCMOS circuits are summarized in Table V. The area sizes of the CMOS and the BiCMOS paths are equal. The BiCMOS circuits are applied to 20% of the circuits of the processor, but in these critical paths, over 50% of the circuits are BiCMOS circuits. The effect of using BiCMOS circuits for these critical paths is 11%–47% shorter delay time.

TABLE IV
Delay Time Comparison Between BiCMOS and CMOS Circuits V_{DD} = 3.3 V

Circuit	BiCMOS	CMOS*	Delay Time Ratio (BiCMOS/CMOS)
Basic logic gate (3NAND, C_L = 0.5 pF)	0.33 ns	0.40 ns	0.83
Sense amp. cir. for register file	0.60 ns	2.01 ns	0.30
22-b Comparator	0.46 ns	0.94 ns	0.49
Path logic adder (FO = 12)	1.26 ns	1.54 ns	0.82

*Area size (CMOS) = Area size (BiCMOS).

TABLE V
Effect of BiCMOS Circuit for Critical Paths. V_{DD} = 3.3 V

Path	BiCMOS	CMOS*	Delay Time Ratio (BiCMOS/CMOS)
Multiplier	18.1 ns	21.1 ns	0.86
Adder	18.5 ns	22.4 ns	0.83
Divider	5.5 ns	6.2 ns	0.89
Register file (Address-BUS)	1.8 ns	3.4 ns	0.53
TLB	5.1 ns	7.6 ns	0.67

*Area size (CMOS) = Area size (BiCMOS).

VI. Conclusion

BiCMOS circuits using 0.5-μm BiCMOS technology have been applied to a 120-MHz RISC microprocessor at 3.3-V power supply. The chip operates at 120 MHz and the peak performance of the floating point operation is 240 MFLOPS. Power dissipation of the chip is 17 W.

Five new BiCMOS circuits were implemented in the chip. The BiCMOS circuits are applied to a floating point datapath, an integer datapath, translation lookaside buffers and control units. Each BiCMOS circuit is 1.2–3.3 times faster than corresponding CMOS circuits. The processor with the proposed BiCMOS circuits has a 11%–47% shorter delay time advantage over a CMOS microprocessor.

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