Design Techniques for Low-Voltage High-Speed Digital Bipolar Circuits

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Abstract— **This paper describes design techniques for multigigahertz digital bipolar circuits with supply voltages as low as 1.5 V. Examples include a 2/1 multiplexer operating at 1 Gb/s with 1.2 mW power dissipation, a D-latch achieving a maximum speed of 2.2 GHz while dissipating 1.4 mW, two exclusive-OR gates with a delay less than 200 ps and power dissipation of 1.3 mW, and a buffer/level shifter having a delay of 165 ps while dissipating 1.4 mW. The prototypes have been fabricated in a 1.5-μm 12-GHz bipolar technology. Simulations on benchmarks such as frequency dividers and line drivers indicate that, for a 1.5-V supply, the proposed circuits achieve higher speed than their CMOS counterparts designed in a 0.5-μm CMOS process with zero threshold voltage.**

I. Introduction

OVER the past few years, supply voltages below the 5-V standard have been emerging in many electronic systems. The demand for lower power dissipation and fewer batteries in applications such as wireless and personal computing has motivated the scaling of supply voltage of digital circuits down to 1.5 V [1], [2]. This trend is augmented by the fact that silicon devices are fundamentally constrained by a (cutoff frequency) × (breakdown voltage) of approximately 200 GHz·V [3], thus requiring lower supplies if their dimensions are scaled down.

This paper presents design techniques for multigigahertz digital bipolar circuits that operate with supply voltages as low as 1.5 V. These techniques are described in the context of several circuit topologies, namely, a 2/1 multiplexer (MUX), a D-latch, two exclusive-OR (XOR) gates, and a buffer/level shifter. Fabricated in a 1.5-μm 12-GHz bipolar technology, the multiplexer operates at 1 Gb/s with 1.2 mW power dissipation, the latch achieves a speed of 2.2 GHz while dissipating 1.4 mW, the exclusive-OR gates exhibit a delay less than 200 ps and power dissipation of 1.3 mW, and the buffer/level shifter has a delay of 165 ps while dissipating 1.4 mW.

In order to demonstrate the speed advantage of bipolar transistors over CMOS devices even at low supply voltages, the performance of the proposed D-latch and buffer/level shifter is compared to that of their CMOS counterparts. This comparison is based on the speed of simple benchmarks such as frequency dividers and line drivers.

The next section of this paper reviews the design issues of low-voltage digital bipolar circuits. In Section III, the low-voltage techniques and circuit configurations are described, and in Section IV their performance is compared to that of CMOS circuits. Experimental results are presented in Section V.

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II. Low-Voltage Design Issues

Reduction of the supply voltage (V_{EE}) of digital bipolar systems entails several device and circuit issues, some of which become particularly important if $|V_{EE}| < 2$ V. In this section, we review these issues and calculate the minimum supply voltage for representative conventional ECL circuits.

The principal difficulty in scaling V_{EE} is that the "turn-on" potential, i.e., the base-emitter voltage (V_{BE}) of bipolar transistors in forward active region, does not scale linearly with technology. Since

$$V_{BE} \approx V_T \ln \frac{I_C}{I_S} \tag{1}$$

where $V_T = kT/q$, I_C is the collector current, and I_S is the reverse saturation current, we note that device parameters and current levels have only a weak influence on the magnitude of V_{BE}. In practice, current density of bipolar transistors (I_C/I_S) has either remained constant or increased, leading to the same trend for V_{BE}. Since in current technology, $V_{BE} \approx 0.8$ V, in a 1.5-V system any dc path from ground to V_{EE} must include no more than one base-emitter junction, thus prohibiting the use of topologies in which emitter followers drive differential pairs or other emitter followers.

Another difficulty in designing low-voltage digital bipolar circuits is that the voltage swings typically employed in conventional ECL circuits cannot be arbitrarily scaled because the minimum value of these swings is determined by noise margin and error budget considerations. For example, as shown in the Appendix, a bipolar differential pair requires a minimum input voltage swing of approximately $5.5\,V_T$ to reach its unity-gain points, a value that does not easily scale with technology. In reality, the voltage drop across the emitter resistance must be added to this value and errors due to incomplete switching, finite current gain, and voltage drops along supply lines must be taken into account, thereby dictating minimum voltage swings of several hundred millivolts.

In order to maintain a high speed, bipolar transistors must not enter heavy saturation, i.e., their base-collector forward bias voltage must not exceed approximately 400 mV. This constraint translates into a minimum collector-emitter voltage (V_{CE}) of about 400 mV, and together with a V_{BE} of 800

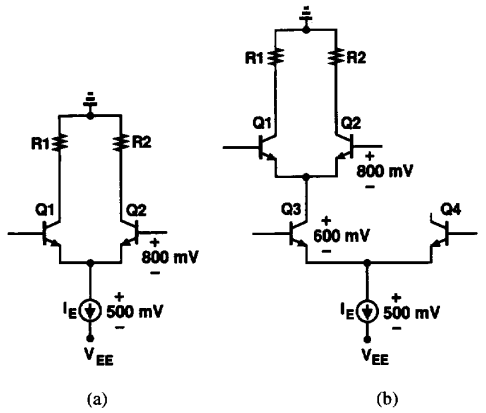

Fig. 1. Representative conventional ECL circuits: (a) inverter, (b) stacked differential pairs.

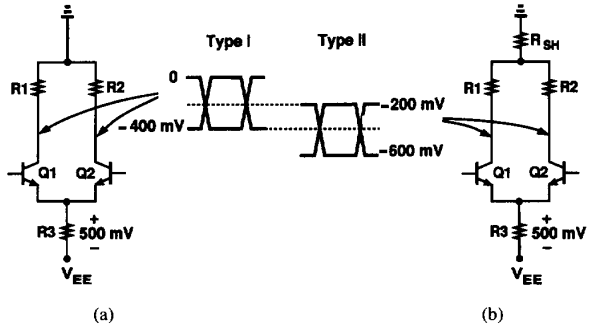

Fig. 2. Signal levels and swings used in the proposed circuits: (a) Type I signals, (b) Type II signals.

mV, prohibits the use of stacked differential pairs or cascode configurations in a 1.5-V system. As a consequence, operations such as clocking and multiplexing cannot be implemented using conventional ECL topologies.

To demonstrate the above issues further, we calculate the minimum supply voltage required for two representative ECL circuits, depicted in Fig. 1(a) and (b). In the simple inverter of Fig. 1(a), if the voltage swings across $R1$ and $R2$ remain less than 400 mV, the base voltage of $Q1$ and $Q2$ can reach the ground potential with no substantial degradation in speed. Assuming a minimum voltage of 500 mV across the tail current source, we note that the minimum $|V_{EE}|$ is approximately 1.3 V.

Fig. 1(b) illustrates two stacked differential pairs, a topology often employed in ECL latches, multiplexers, XOR gates, etc. If the base voltage of $Q1$ and $Q2$ is allowed to reach the ground potential, then the minimum supply voltage of this circuit is given by the sum of V_{BE} of $Q1$ (or $Q2$), V_{CE} of $Q3$, and the voltage across the tail current source. If $Q1$ and $Q2$ are driven by differential signals, their emitter voltage drops by approximately half the input voltage swing when the pair is switching. The minimum V_{CE} allowed for $Q3$ must therefore take this drop into account so as to keep the transistor out of heavy saturation. For $V_{CE3} = 600$ mV, the minimum supply voltage of this circuit is approximately 1.9 V.

While the choice of the voltage drop across the tail current source in the above circuits is somewhat arbitrary, the approximate value of 500 mV represents a practical minimum in many systems. This point is discussed further in the next section.

III. Low-Voltage Circuits

A. Signal Levels and Voltage Swings

The signal levels and voltage swings employed in this work are depicted in Fig. 2. These levels are similar to those used in [4]. All circuits generate 400-mV (single-ended) or 800-mV (differential) outputs. To perform functions such as clocking and multiplexing, two types of signals—herein called Type I and Type II—are used. In Type I, the signals swing between 0 V and −400 mV, and in Type II between −200 and −600 mV. As will be seen in the actual circuits later, the 200-mV difference between the common-mode levels of Type I and Type II in essence provides a half logic level [4], allowing the control of differential pairs by means of clamp devices. For reliable operation, the high level of Type I must be sufficiently *higher* than the high level of Type II, and the low level of Type I must be sufficiently *lower* than the high level of Type II.

In order to establish the level shift required for Type II signals, a resistor R_{SH} is used as shown in Fig. 2(b). The designs presented here generate Type II outputs; if Type I is needed, R_{SH} can be set to zero.

The bias currents of differential pairs and emitter followers are produced using resistors tied from their respective emitters to $V_{EE}(= -1.5\text{V})$, with approximately 500 mV drop across each. If NMOS devices are available, they can replace these resistors to provide much higher immunity to variations in the supply voltage and the input common-mode level. This is possible because, if properly sized, MOS transistors can remain in saturation even with a drain-source voltage of 500 mV. This value usually provides a reasonable compromise between the loss in voltage headroom and the size of the MOS transistors. If the saturation behavior of bipolar transistors is characterized and modeled accurately, they may be used as current sources here with a slight speed penalty.

B. 2/1 Multiplexer

Shown in Fig. 3 is a circuit diagram of the 2/1 multiplexer. It consists of two differential pairs $Q1$-$Q2$ and $Q3$- $Q4$ that sense the inputs A and B and are controlled by CK and $\overline{CK}$ through clamp devices $Q5$ and $Q6$, respectively. The output currents of the two pairs are summed at nodes X and Y, and flow through resistors $R1$ and $R2$. Note the CK and $\overline{CK}$ are Type I while other signals are Type II.

The circuit operates as follows. When CK is low, $Q5$ is off, allowing $R3$ to draw current from $Q1$ and $Q2$, while $\overline{CK}$ is high, and $Q6$ pulls the node N high, turning off $Q3$ and $Q4$. Thus, the pair $Q1$-$Q2$ is enabled, the pair $Q3$-$Q4$ is disabled, and the output is equivalent to the A input. Similarly, when CK goes high, the pair $Q1$-$Q2$ is disabled, the pair $Q3$-$Q4$ is enabled, and the output becomes equivalent to the B input.

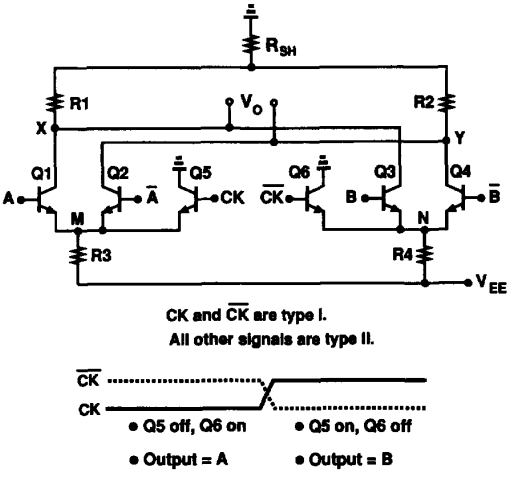

Fig. 3. 2/1 multiplexer.

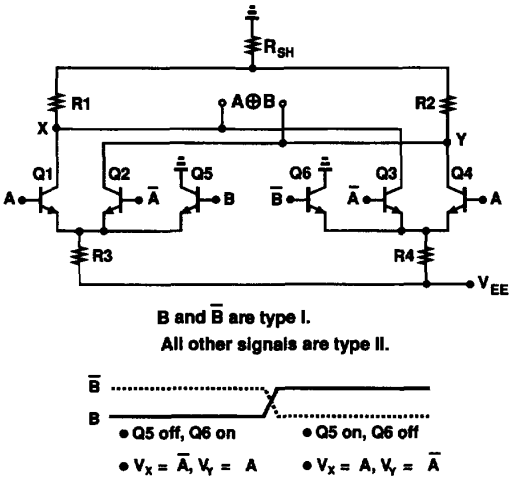

Fig. 5. Exclusive-OR gate derived from MUX of Fig. 3.

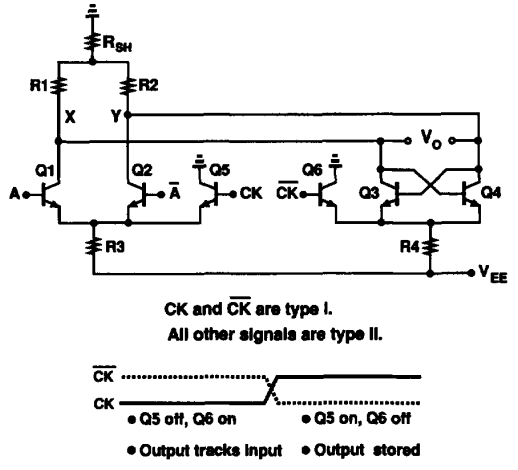

Fig. 4. D-latch circuit diagram.

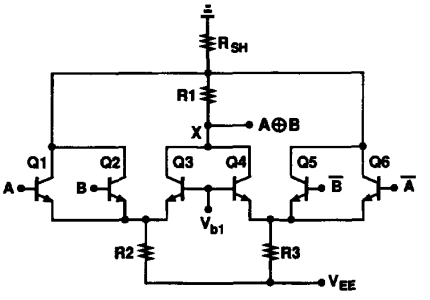

Fig. 6. Symmetric XOR gate.

Note that $Q1$-$Q4$ experience a base-collector forward bias of 400 mV and hence enter soft saturation.

C. D-Latch

The concept used in the MUX of Fig. 3, namely, controlling differential pairs by means of clamp transistors, can be applied to the design of several other circuits as well. For example, if one of the differential pairs in the MUX is reconfigured into a cross-coupled pair, then a D-latch results, as shown in Fig. 4. This circuit comprises an input differential pair $Q1$- $Q2$ and a latch pair $Q3$-$Q4$, which are controlled by CK and $\overline{CK}$ in a manner similar to that described for the MUX of Fig. 3. When CK is low, the input pair is enabled, nodes X and Y track the input, and $Q3$ and $Q4$ are off. When CK goes high, the input pair turns off, the latch pair turns on, and the instantaneous state at X and Y is stored in the loop around $Q3$ and $Q4$.

D. XOR Gates

The MUX of Fig. 3 can perform an XOR function if configured as in Fig. 5. Here, both of the differential pairs sense the A input but with a reversal in polarity, while the clamp devices sense the B input. When B is low, the pair $Q1$-$Q2$ is enabled and $V_X = \overline{A}$ and $V_Y = A$. When B is high, the pair $Q3$- $Q4$ is enabled and $V_X = A$ and $V_Y = \overline{A}$. Thus, the logical output is equal to $A \oplus B$.

In contrast with the conventional ECL XOR gate, where one of the inputs propagates through level-shift emitter followers and stacked differential pairs, the XOR cicuit of Fig. 5 exhibits shorter delay for both of its inputs. Simulations indicate a delay of 130 ps with a power dissipation of 1.4 mW for the proposed XOR, and a delay of 150 ps for the conventional XOR having the same voltage swings and collector resistors.

In the XOR of Fig. 5, the signal paths of A and B are not exactly identical, thereby introducing a slight phase error between A and B at high frequencies. In applications where this error is crucial—such as in phase-locked loops—the symmetric XOR of Fig. 6 can be utilized. This circuit consists of two similar sections ($Q1$-$Q3$ and $R2$, $Q4$-$Q6$ and $R3$) with their outputs summed at node X. The reference voltage V_{b1} is equal to the common-mode level of the input signals

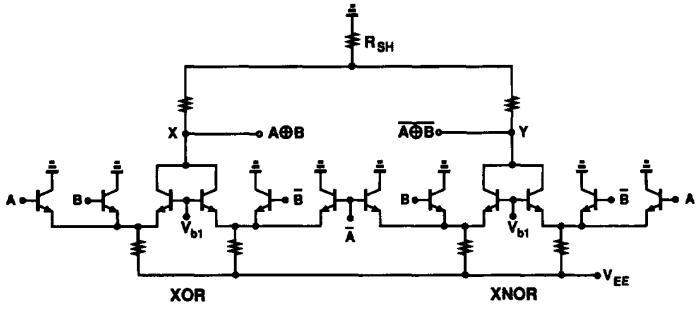

Fig. 7. Symmetric XOR gate with differential output.

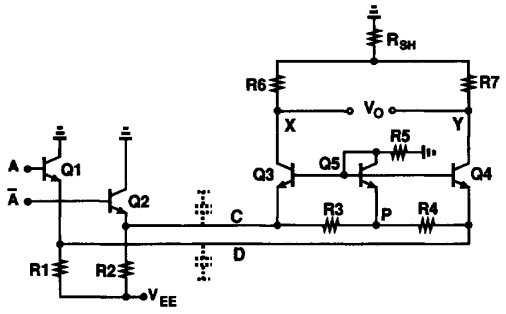

Fig. 8. Buffer/level shifter.

$(A, \overline{A}, B,$ and $\overline{B})$. The operation of the circuit can be explained by noting that $Q3$ is on only if both A and B are low and, similarly, $Q4$ is on only if both $\overline{A}$ and $\overline{B}$ are low. Thus, $I_{C3} = \overline{A} \cdot \overline{B}$ and $I_{C4} = A \cdot B$, where I_{C3} and I_{C4} represent the logical value of collector currents of $Q3$ and $Q4$, respectively. The summation of these two currents at X is equivalent to a logical OR function, and the conversion of the resulting current to a voltage below ground (by $R1$) is equivalent to a logical inversion. Thus, the output is equal to $\overline{A \cdot B + \overline{A} \cdot \overline{B}} (= A \oplus B)$.

The circuit of Fig. 6 provides a single-ended output. If differential outputs are required, the circuit can be replicated with the inputs A and $\overline{A}$ interchanged in the replica, hence producing an exclusive-OR and an exclusive-NOR gate (Fig. 7).

E. Buffer/Level Shifter

Distribution of signals across a large chip often entails the use of long interconnects having substantial capacitance to the substrate. To drive these interconnects, a buffer with low output impedance is required. While emitter followers can provide such an output impedance, they also shift the common-mode level down by one V_{BE}. Consequently, in a 1.5-V system, they must be followed by a level shift circuit at the end of the interconnects to shift the common-mode level up.

Fig. 8 illustrates a configuration wherein input transistors $Q1$ and $Q2$ drive the interconnects, and the circuit consisting of $Q3$-$Q5$ and $R3$-$R7$ performs sensing, level shift, and amplification. Note that the circuit can be viewed as emitter followers ($Q1$ and $Q2$) driving common-base transistors ($Q3$ and $Q4$) or simply as two differential pairs ($Q1$-$Q4$ and $Q2$-$Q3$). The input is assumed to be differential.

An important issue in the design of the buffer circuit is that the bias voltage at the base of $Q3$ and $Q4$ must track the common-mode voltage of A and $\overline{A}$ so that the ratio of collector currents of $Q1$-$Q4$ is stable and well defined. Since, in practice, the input emitter followers may be located far from the sense and level shift circuit, a bias voltage generated locally in the vicinity of $Q3$ and $Q4$ may not track the input common-mode level in the presence of voltage drops along supply lines.

To alleviate the above problem, the circuit of Fig. 8 recovers the common-mode level of the signals received from the interconnects and biases transistors $Q3$ and $Q4$ according to that level. Reproduced by (equal) resistors $R3$ and $R4$, the common-mode level is established at node P and shifted up by $Q5$. The base voltage of $Q5$ is therefore a close approximation of the common-mode level of A and $\overline{A}$, hence providing the proper bias for $Q3$ and $Q4$. The collector currents of $Q1$-$Q4$ are set by sizing them with respect to $Q5$ and by the values of $R1$-$R5$.

Analysis of the buffer/level shifter circuit indicates that, for 400-mV swings at A and $\overline{A}$, transistors $Q3$ and $Q4$ limit the voltage swings at nodes C and D to approximately 200 mV, thereby improving the speed substantially.

Fig. 9 shows the simulated delay of the circuit as a function of the load capacitance while the circuit dissipates 1.4 mW. The delay increases by 170 ps for a 1-pF increase in the load capacitance.

IV. Comparison to CMOS

As mentioned in Section II, the unscalable V_{BE} of bipolar transistors raises serious concern about the scalability of the supply voltage of bipolar circuits—an issue that, in principle, does not exist in CMOS technology because the threshold voltage (V_{TH}) of MOS devices can be lowered during fabrication. Thus, it is important to compare the performance of the proposed bipolar circuits to that of their CMOS counterparts at a supply voltage of 1.5 V.

In order to perform a meaningful, easy-to-reproduce comparison, we consider two simple benchmarks: a frequency

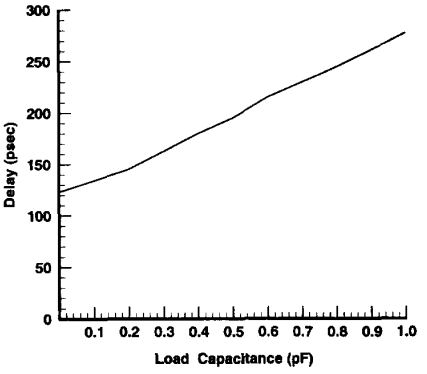

Fig. 9. Simulated delay of buffer/level shifter versus load capacitance.

divider and a line driver. Using simulations, we compare the speed of these circuits in 1.5-V bipolar and CMOS systems. To obtain comparable speeds, the simulations incorporate AT&T's 0.5- μm CMOS device models (whereas the proposed circuits are built in a 1.5-μm bipolar technology). To make the simulations even more favorable to CMOS, V_{TH} of both NMOS and PMOS transistors is deliberately set to zero, thereby providing a rail-to-rail gate-source overdrive for these devices. In practice, nonidealities such as subthreshold conduction, variation of threshold voltage with temperature, and more pronounced short-channel effects with increased channel implant dose impose a lower bound of several hundred millivolts upon V_{TH}. Reference [2] discusses some of these issues in detail.

In this comparison, we have used an unrealistically "good" CMOS process to demonstrate the speed advantage of the bipolar circuits. Nonetheless, comparing the power dissipation of 1.5-μm bipolar to that of 0.5-μm CMOS would not be fair. Note that the emphasis of the paper is more on low voltage than low power. In many systems (such as the phase-locked loop in [7]), these circuits dissipate only a small fraction of the overall power, but it is important that they operate with low voltages.

A. Frequency Divider

The bipolar D-latch of Fig. 4 can be utilized in a master-slave flipflop with negative feedback to provide a $\div 2$ circuit. Such an arrangement is depicted in Fig. 10, wherein the output of the divider is sensed by means of a differential pair.

A CMOS $\div 2$ circuit is illustrated in Fig. 11 [5], wherein a cascade of two dynamic inverters controlled by CK and $\overline{CK}$ is followed by a static inverter, thus producing a state that experiences one net inversion around the loop on every clock cycle. The logic levels at the divider's output are restored by a minimum-size inverter.

Circuit simulations indicate that for a 1.5-V supply, the bipolar divider achieves a maximum clock frequency of 2.5 GHz, whereas the CMOS divider cannot operate faster than 1.7 GHz. To gain more insight, we plot the maximum clock frequency of each circuit as a function of supply voltage, as

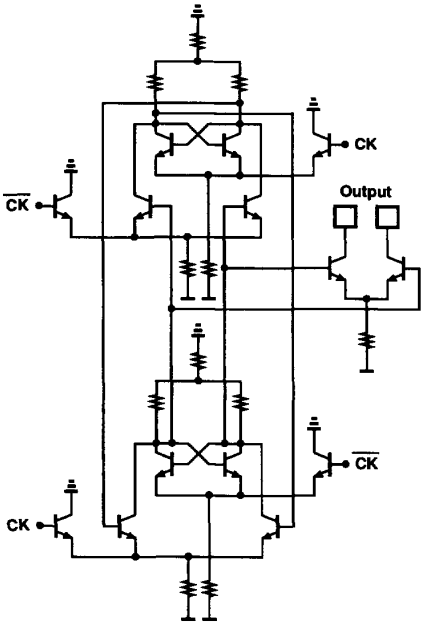

Fig. 10. Bipolar frequency divider.

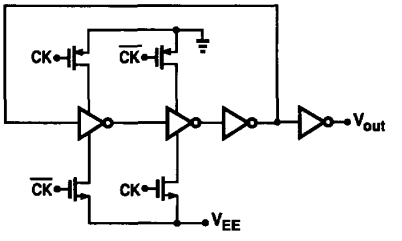

Fig. 11. CMOS frequency divider.

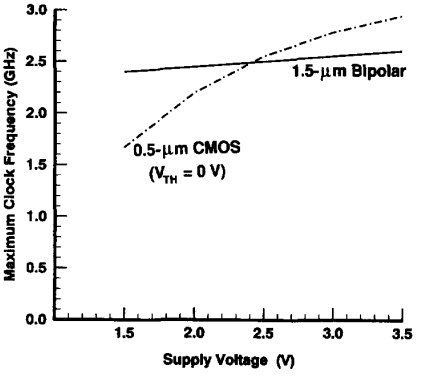

Fig. 12. Maximum clock frequency of bipolar and CMOS dividers versus supply voltage.

shown in Fig. 12. In this simulation, the bias currents of the bipolar divider are generated using ideal current sources so as to maintain constant voltage swings when the supply voltage varies. This plot indicates that, even with $V_{TH} = 0$ V, the 0.5-μm CMOS divider is slower than its 1.5- μm bipolar

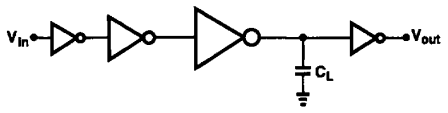

Fig. 13. CMOS tapered buffer.

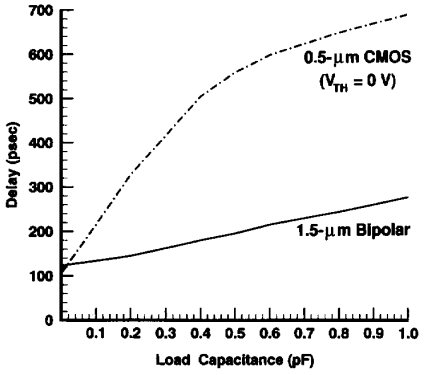

Fig. 14. Delay of bipolar and CMOS line drivers versus load capacitance.

counterpart for $|V_{EE}| < 2.5$ V. Note that the maximum speed of the CMOS divider approaches a limit for $|V_{EE}| > 3$ V because, due to velocity saturation, the increase in current drive of MOS devices simply balances the increase in voltage swings.

The maximum speed of the bipolar divider increases slightly as $|V_{EE}|$ increases because the collector-substrate capacitance of transistors decreases.

B. Line Driver

The buffer/level shifter of Fig. 8 has been designed to provide high-speed drive for heavily loaded busses. As such, this circuit can be compared to CMOS tapered buffers often used to drive large capacitances. Fig. 13 illustrates a CMOS buffer wherein the first stage is driven by a minimum-size inverter and each stage is scaled up in device width so as to minimize the total delay.

Fig. 14 plots the overall delay of the bipolar and CMOS line drivers versus the load capacitance with $V_{EE} = -1.5$ V. The design of the CMOS buffer is optimized as a function of the load capacitance, thus yielding a logarithmic (rather than linear) variation for the delay. This plot indicates that the bipolar buffer proves superior to the CMOS driver if the load capacitance is greater than a few tens of femtofarads.

V. Experimental Results

In order to demonstrate the feasibility of the proposed techniques, a number of test circuits have been fabricated in a 1.5-μm 12-GHz bipolar technology [6]. Fig. 15 shows a die photograph of the prototypes. All the circuits have been tested with a supply voltage of 1.5 V.

The 2/1 multiplexer has been built along with a 1/2 demultiplexer to facilitate testing. The demultiplexer splits its input signal into two, applying the resulting waveforms to the two

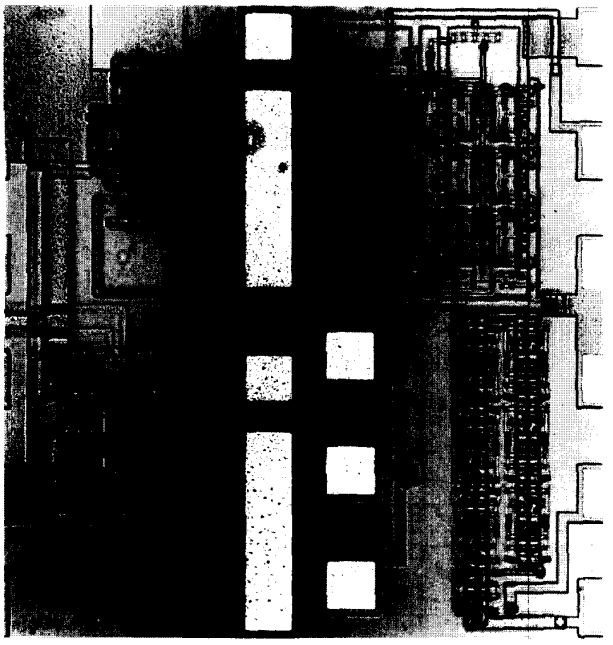

Fig. 15. Die photograph of fabricated prototypes.

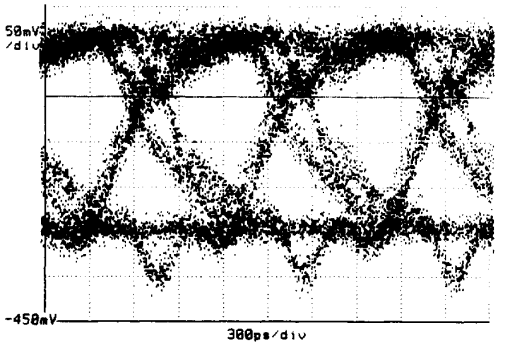

Fig. 16. Measured MUX output at 1 Gb/s.

inputs of the multiplexer. Shown in Fig. 16 is the measured output of the MUX at 1 Gb/s with a power dissipation of 1.2 mW. In this test, a pseudorandom binary sequence is applied at the input to obtain an eye diagram at the output. The pattern-dependent delay observed in this waveform is attributed to soft saturation effects in bipolar transistors.

The D-latch has been employed in a $\div 2$ circuit similar to that of Fig. 10. The measured input and output waveforms of the divider at $f_{in} = 2.2$ GHz are depicted in Fig. 17. Each latch in the divider dissipates 1.4 mW.

The symmetric XOR and the buffer/level shifter have been used in ring oscillators to allow simple measurement of their delay (Fig. 18). It is interesting to note that these two circuits are inherently noninverting, i.e., if a prime number of each circuit is employed in a ring, the overall circuit finds a point at which two independent, stable loops exist, and hence does not oscillate. To overcome this problem, the ring oscillators

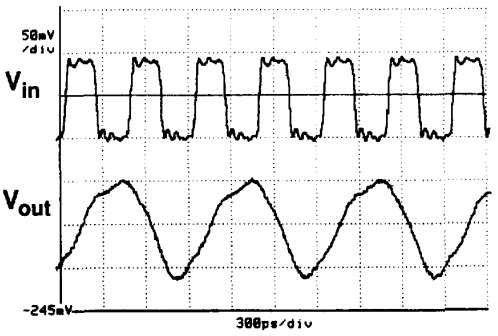

Fig. 17. Measured bipolar divider waveforms at $f_{in} = 2.2$ GHz.

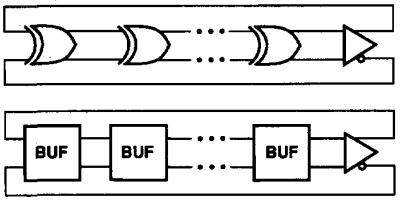

Fig. 18. Ring oscillators used to measure delay of symmetric XOR and buffer/level shifter.

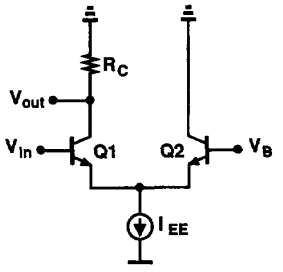

Fig. 19. Single-ended bipolar differential pair.

are designed with 6 stages of the XOR gate or the buffer/level shifter and an explicit inverter.

Measurements indicate a delay of 190 ps for the XOR gate with a power dissipation of 1.3 mW. The buffer exhibits a delay of 165 ps while dissipating 1.4 mW. The measured delay of these circuits is approximately 20% greater than simulation results. This discrepancy is attributed to inaccurate modeling of saturation in bipolar transistors in circuit simulation.

All of the above circuits tolerate a $\pm 10\%$ variation in the supply voltage with no significant degradation in speed.

The symmetric XOR gate has also been successfully incorporated in a 6-GHz phase-locked loop [7].

VI. Conclusion

A number of low-voltage techniques have been introduced for the design of high-speed digital bipolar circuits. Described in the context of several building blocks such as a 2/1 multiplexer, a D-latch, two exclusive- OR gates, and a buffer/level shifter, these techniques allow gigahertz speeds with supply voltages as low as 1.5 V.

Simulations indicate that, although the base-emitter voltage of bipolar transistors does not scale easily, the large transconductance of these devices nonetheless provides substantial speed advantage over MOSFET's even in 1.5-V systems. When used in environments such as frequency dividers and line drivers, the proposed circuits exhibit superior speed in a 1.5-μm bipolar technology compared with their counterparts designed in a 0.5-μm CMOS process with zero threshold voltage.

Appendix
Unity-Gain Points of a Bipolar Differential Pair

We calculate the unity-gain points of a single-ended bipolar differential pair, shown in Fig. 19. The results can be easily extended to fully differential operation as well.

Assuming an infinite β for $Q1$ and $Q2$, we have

$$V_{BE1} - V_{BE2} = V_{in} - V_B \tag{2}$$

$$V_{BE1} - V_{BE2} = V_T \ln \frac{I_{C1}}{I_S} - V_T \ln \frac{I_{C2}}{I_S} \tag{3}$$

$$I_{C1} + I_{C2} = I_{EE}. \tag{4}$$

Thus, if $\Delta V_{in} = V_{in} - V_B$, the output voltage can be expressed as

$$V_{out} = -R_C I_{EE} \frac{\exp \dfrac{\Delta V_{in}}{V_T}}{1 + \exp \dfrac{\Delta V_{in}}{V_T}}. \tag{5}$$

The unity-gain points occur where $\partial V_{out}/\partial V_{in} = -1$. Differentiating the above equation with respect to V_{in} and equating the result to -1, we have

$$\exp \frac{2\Delta V_{in}}{V_T} + \left(2 - \frac{R_C I_{EE}}{V_T}\right) \exp \frac{\Delta V_{in}}{V_T} + 1 = 0 \tag{6}$$

and hence,

$$\exp \frac{\Delta V_{in}}{V_T} = -1 + \frac{R_C I_{EE}}{2V_T} \pm \sqrt{\frac{R_C^2 I_{EE}^2}{4V_T^2} - \frac{R_C I_{EE}}{V_T}}. \tag{7}$$

Since, typically, $R_C I_{EE} \gg V_T$, and for $\epsilon \ll 1$ we have $\sqrt{1-\epsilon} \approx 1 - \epsilon/2 - \epsilon^2/8$, equation (7) can be simplified to yield

$$\exp \frac{\Delta V_{in}}{V_T} \approx -1 + \frac{R_C I_{EE}}{2V_T} \pm \frac{R_C I_{EE}}{2V_T}\left(1 - \frac{2V_T}{R_C I_{EE}} - \frac{2V_T^2}{R_C^2 I_{EE}^2}\right). \tag{8}$$

Assuming

$$\frac{R_C I_{EE}}{V_T} \gg 2 + \frac{V_T}{R_C I_{EE}} \tag{9}$$

we obtain the following solutions:

$$\exp \frac{\Delta V_{in}}{V_T} = \frac{R_C I_{EE}}{V_T} \quad \text{or} \quad \frac{V_T}{R_C I_{EE}}. \tag{10}$$

From the above equations, it follows that the unity-gain points occur where

$$\Delta V_{in} = \pm V_T \ln \frac{R_C I_{EE}}{V_T}. \quad (11)$$

In practice, various error sources impose an $R_C I_{EE}$ of several hundred millivolts; thus, if, for example, $R_C I_{EE} = 400$ mV and $V_T = 26$ mV, then the total input range between unity-gain points is approximately equal to $5.5\,V_T$.

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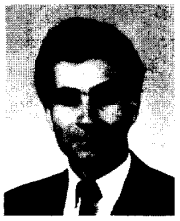
REFERENCES

[1] M. Hiraki *et al.*, "A 1.5-V full-swing BiCMOS logic circuit," *IEEE J. Solid-State Circuits*, vol. 27, pp. 1568–1574, Nov. 1992.
[2] K. Shimohigashi and K. Seki, "Low-voltage ULSI," *IEEE J. Solid-State Circuits*, vol. 28, pp. 408–413, Apr. 1993.
[3] E. O. Johnson, "Physical limitations on frequency and power parameters of transistors," *RCA Rev.*, vol. XXVI, pp. 163–177, June 1965.
[4] K. Nojima and Y. Gendai, "An 8-b 800-MHz DAC," *IEEE J. Solid-State Circuits*, vol. 25, pp. 1353–1359, Dec. 1990.
[5] Y. Kado *et al.*, "A 1-GHz/0.9-mW CMOS/SIMOX divide-by-128/129 dual modulus prescaler using a divide-by-2/3 synchronous counter," *IEEE J. Solid-State Circuits*, vol. 28, pp. 513–517, Apr. 1993.
[6] K. G. Moerschel *et al.*,, "BEST: A BiCMOS-compatible super-self-aligned ECL technology," *Proc. CICC*, pp. 18.3.1–18.3.4, May 1990.
[7] B. Razavi and J. Sung, "A 6-GHz, 60-mW BiCMOS phase-locked loop with 2-V supply," in *ISSCC Dig. Tech. Papers*, Feb. 1994, pp. 114–115.



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