Low-Voltage and Low-Power Circuit Design for Mixed Analog/Digital Systems in Portable Equipment

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Abstract— **This paper describes low-voltage and low-power (LV/LP) circuit design for both analog LSI's and digital LSI's which are used in mixed analog/digital systems in portable equipment. We review some LV/LP circuits used in digital LSI's, such as general logic gate, DSP, and DRAM, and others used in analog LSI's, such as operational amplifiers, video-signal processing circuits, A/D and D/A converters, filters, and RF circuits, along with a wide range of items used in recently developed LSI's. Since analog circuits have fundamental difficulties for reducing the operating voltage and the power consumption, in spite of recent progress in LV/LP circuit techniques, these difficulties will be a major issue for decreasing the total power consumption of some mixed analog/digital systems used in portable equipment.**

I. Introduction

DIGITAL processing technology is going to be widely used in portable electronic equipment, and much more complicated digital processing, such as audio/video compression and decompression technologies, will be used in the future. But the use of analog processing will continue in future portable equipment, even with the use of complicated digital processing. This is because signals to and from I/O devices, such as magnetic recordings, microphones, speakers, CCD's, LCD's, and wireless modulators and demodulators, are analog.

Hence, we must pay much attention to the low-voltage and low-power (LV/LP) design of mixed analog/digital circuits in portable equipment.

In recent years, there has been much discussion on the reduction of operating voltage and power consumption with a focus on digital circuits [1], [2]. The essence of the design of LV/LP digital circuits is how to increase the operation speed of the digital system under the condition that the driving currents of CMOS gates decreases when the operating voltage decreases. The reduction of the design rule is the most effective solution because of its high drivability, also the parallel scheme and optimized pipeline scheme are effective in digital systems compatible with these circuit schemes.

In contrast with digital circuits, it is very difficult to show the general solutions for LV/LP issues in analog circuits. This is because there are many kinds of analog circuit functions. Some examples are the operational amplifier, small signal amplifier, power amplifier, current source, voltage generator, multiplier, modulator, oscillator, filter, and PLL. Also, there are many specifications for analog circuits, such as dynamic range, bandwidth, frequency response, time response, settling time, distortion, accuracy, signal-to-noise ratio (SNR), stability, and efficiency. Furthermore, there are many varieties of circuit topologies for realizing each analog function. Hence, for analog circuits, it would be impossible to show the general or unified solutions for LV/LP design issues.

Therefore, I will present some viewpoints on the design of LV/LP digital and analog circuits which have been used in or will be used in portable equipment, such as the camera recorder, portable tape recorder, and cellular phone, with a focus on analog circuit technology rather than digital.

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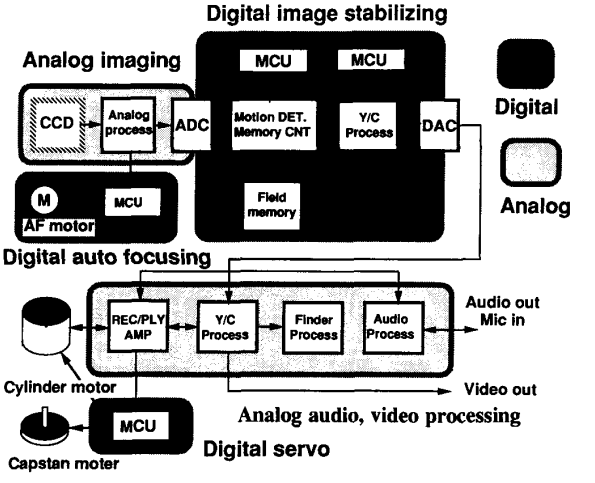


Fig. 1. Block diagram of the camera-recorder.

II. The Present State of Portable Equipment

Fig. 1 shows a block diagram of the camera recorder [3] which uses digital image stabilization. In this figure, dark shaded areas are digital circuit blocks and light shaded areas are analog circuit blocks. Electric zooming, automatic image stabilization, auto-focusing, and auto-white balancing are realized by digital technology. The recording method is still analog, and many analog ICs are used for analog video signal processing in the VTR block.

The camera recorder strongly needs LV/LP LSIs. One reason is to realize long playing time and the other reason

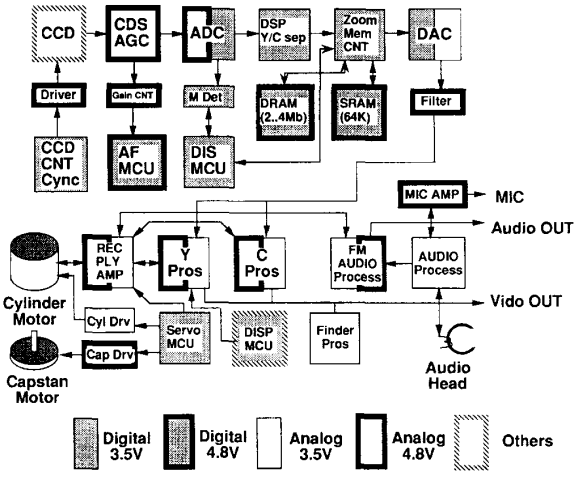


Fig. 2. Organization of chip set of the camera-recorder.

is to reduce the weight and volume of portable equipment and to avoid thermal problems such as degradation of magnetic recording characteristics. The volume of the camera-recorder will become much smaller in the next generation, even if the number of logic gates increases rapidly. Thus, the design of LV/LP LSI is imperative for the future camera-recorder.

The reduction of operating voltage is the most effective solution for realizing low power LSI's. Thus, the logic LSI's are fabricated with 1.2-μm CMOS technology, and the operating voltage is set to 3.5 V. However, 4.8 V is still used for all memory LSI's and some analog IC's. Furthermore, double power supply voltages of 3.5 and 4.8 V are used for several analog IC's and A/D converter to optimize the supply voltage for each circuit block in the same LSI chip, as shown in Fig. 2. The two voltages are generated by switching power supply circuits from a battery unit whose voltage is 6 V.

The total power consumption is 7.7 W, lower than that of all previous analog camera recorders which consume larger than 9 W, in spite of introducing digital technologies. The power consumption ratios for each circuit block are 50% for digital LSI, 25% for analog IC's, and 25% for motor drive IC's.

Next, I will discuss practical solutions and the present state of technologies for realizing lower operating voltage and lower power consumption in both digital and analog circuits.

III. Digital LSI

A. General Logic Gate

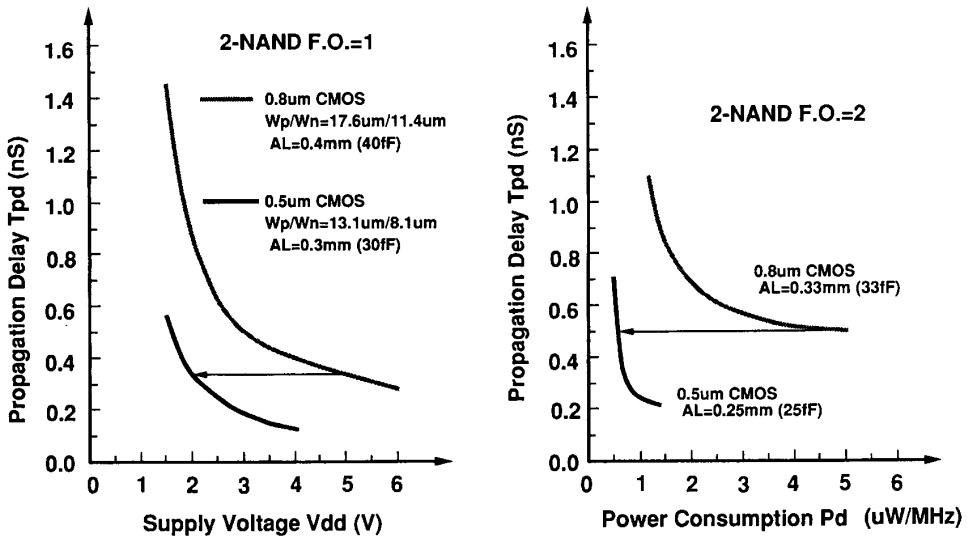
LV/LP logic gates can be attained easily by using short channel CMOS devices. Fig. 3 shows the propagation delay time Tpd versus operating voltage Vdd and the propagation delay time Tpd versus power consumption Pd for 0.8-μm and 0.5-μm CMOS gates. The 0.8-μm CMOS gate needs an operation voltage of 5 V to obtain a propagation delay of 0.35 ns. In contrast, the 0.5-μm CMOS gate can operate with only 2.0 V to obtain same propagation delay. Also, the 0.8-μm CMOS gate consumes about 5 μW/MHz to obtain a propagation delay of 0.5 ns, and the 0.5 μm CMOS gate consumes only 0.6 μW/MHz to obtain the same propagation delay. This result means that short channel CMOS devices will become inevitable in future portable equipment. Other circuit techniques, such as complementary pass-transistor logic (CPL) [4] and parallel processing scheme [1], which can lower the operating frequency and operating voltage with the increase of the number of parallel circuits, would be able to realize low power consumption even if short channel CMOS devices are not used. CPL will be useful for realizing LV/LP digital circuits when it will apply to some special circuits, such as adders and multiplexers; however, it will be very difficult to apply it to general logic gates. Though the parallel processing scheme will also be useful for realizing LV/LP circuits, its application will be limited due to the large cost.

B. DSP

The DSP is a key device for digital cellular telephones. Several circuit and system techniques have been used to realize LV/LP DSP's. Some of its features are the introduction of static circuits, the minimization of frequency of signal transition on bus, a shutdown architecture when the circuit blocks are unnecessary, the optimization of pipeline scheme, and an optimized layout for reducing load capacitance. The DSP [5], which is fabricated with 0.8-μm CMOS technology and consumes only 70 mW with operating voltage of 3.5 V at a operating frequency of 10.7 MHz, has been developed recently. Fig. 4 shows a main circuit block of this DSP. It contains an independent multiply and accumulate (MAC) unit and double data-width memories. The MAC unit can execute two instructions in one machine cycle, also the memories can output twice as much data in one machine cycle.

1) Independent Multiply and Accumulate (MAC) Unit: It was found that the power reduction of the MAC unit is very effective for the reduction of the total power consumption of the DSP. This is because the MAC operation occupies about 80% of the total number of operations, when the DSP executes both coding and decoding programs. The conventional DSP executes MAC operation with a multiplier, a general ALU separated from the multiplier, general registers, and data buses connecting these components. This configuration has a large expandability and flexibility for executing a variety of applications. The power consumption is large, however, due to the large capacitances of the bus-lines. In contrast, the proposed DSP has an independent MAC unit to avoid the extra power consumption of these parts.

2) Double Data-Width Memory: Furthermore, memories are designed to operate at half-frequency by doubling the data-width. The two sets of data coming from one memory block are stored in a temporary register in one machine cycle, and each set of data is sent to the multiplexer every half machine cycle. Since the propagation delay time of the gate is roughly proportional to the operating voltage [1], the operating voltage of this memory block can be reduced by about half of that for the conventional memory block. As a result, the power consumption of the proposed memory can be about a quarter of that for the conventional memory. In general, the parallel



(a) (b)

Fig. 3. Propagation delays versus supply voltage and power consumption for 0.8 μm/0.5 μm CMOS gates: (a) Propagation delays versus supply voltage, (b) Propagation delays versus power consumption.

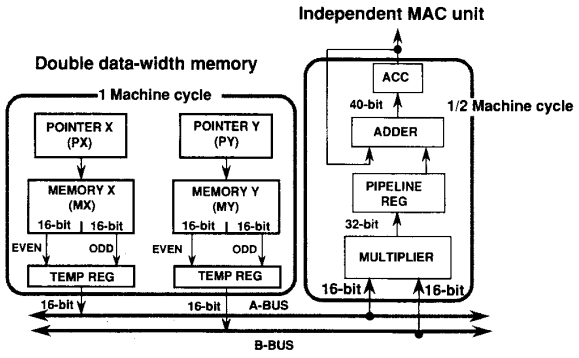


Fig. 4. Main circuit block of the DSP.

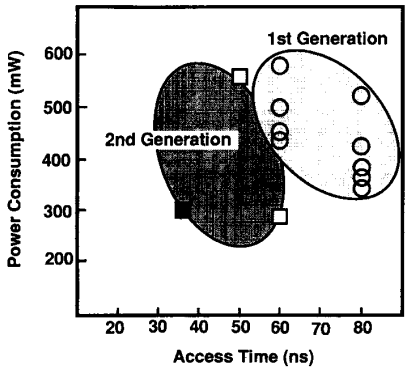


Fig. 5. Power consumption versus access time of 16 Mb DRAM's.

scheme is useful for the reduction of power consumption; however, it has a large area penalty. But in this case the area penalty is only less than 5% for the memory block. This is because it is limited in the peripheral circuits of the memory.

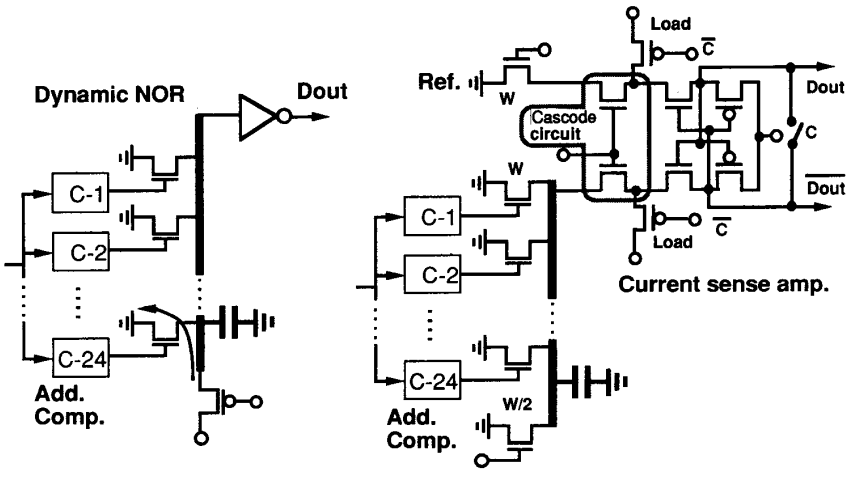
The total power consumption of this proposed DSP can be reduced to 1/7 of that for the previous DSP when the instruction speed is the same.

C. Memory

For portable audio/video equipment, DRAM plays an important role as the picture memory. Presently, the required memory size is about 3 Mb for one TV field. However, 16 M to 64 M bits will be used in future products based on the standard coding algorithms called moving picture experts group (MPEG) or motion joint photographic experts group (JPEG). Hence, the power consumption of DRAM will strongly affect the total power consumption of the equipment. Fig. 5 plots the power consumption versus access time for reported 16-Mb DRAM's. The first generation 16-Mb DRAM's consume much power and have a slow access time of 60–80 ns. In contrast, the proposed second generation 16-Mb DRAM [6] can obtain fast operation speed and small power consumption. Its RAS access time is only 36 ns even at 1.8 V operation.

The keys to this low-voltage operation of DRAM are the current sensing technology applied to the redundant address generator and the reduction of threshold voltage (V_T) of the transistor used in the sense amplifier.

1) Current Sensing Scheme in the Redundant Address Generator: In our recently developed 16 Mb DRAM, the current sensing scheme applies not only to the sensing block for the memory data, but also to the redundant address generator blocks. It is important for the total power reduction of portable equipment to suppress the standby current of DRAMs. Hence, the longer refresh period is so greatly needed that many



(a) (b)

Fig. 6. Redundant address generators: (a) Conventional, (b) Current sensing.

number of redundant circuits should be provided not only to save defective memory cells, but also to save the cells whose pause time is shorter. Hence, the load capacitor of this redundant circuit becomes heavier rapidly with the increase of the redundancy. As a result, the time delay in this circuit tends to be longer.

To address this issue, we use the current sensing scheme in the address generator circuits. Conventionally, the dynamic NOR gates are used as shown in Fig. 6(a). The propagation delay time of this circuit is large due to large load capacitance. Moreover, it becomes longer and longer when reducing the operating voltage. The redundant address generator circuit contains a sensing circuit, load resistor, and cascode circuit, as shown in Fig. 6(b). The data is transferred to the load resistor with small swing voltage and amplified to generate large output voltage in this current sensing circuit. Consequently, the large loading capacitance has not affected the data delay much, and an improvement of 4.8 ns for the delay is obtained at an operation voltage of 1.5 V.

2) Reduction of V_T in the Sense Amplifier Circuit: Another circuit technology is the reduction of V_T in the sense amplifier circuit. The bit-line sensing circuit as shown in Fig. 7(a) will be activated when closing the switches. However, It is difficult for the transistors to be activated when the operating voltage is smaller than 1.8 V. This is because the bit-line voltage is almost equal or smaller than the V_T of the transistor and voltage drop of the common switching node reaches about 0.2 V. The solution is the reduction of the V_T. Fig. 7(b) shows the bit-line sensing delay versus V_T of NMOS in the sensing amplifier. The bit-line sensing delay increases rapidly with increasing V_T. Hence, we set the V_T to 0.42 V.

Fig. 8 shows the sensing delay time versus operating voltage.

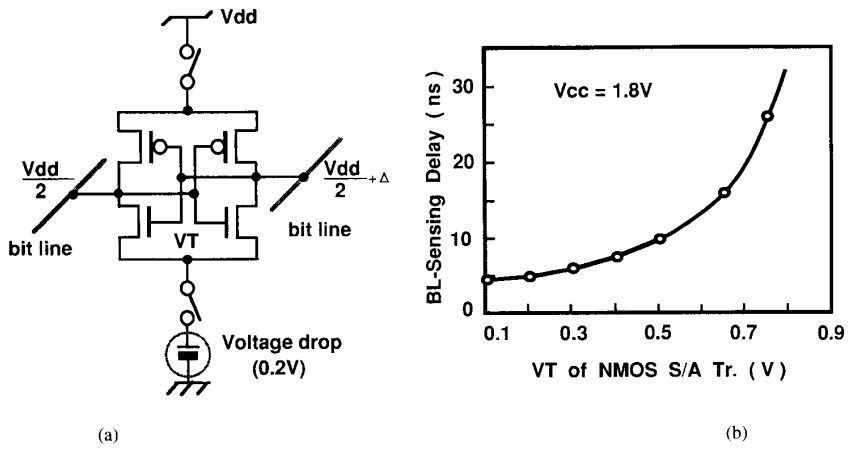
The sensing delay increases rapidly as the operating voltage decreases.

The sense delay can be reduced 15 ns compared to that for the use of a conventional V_T of 0.75 V at the operating voltage of 1.8 V. The sense delay is only 7 ns. These circuit techniques are based on analog technology rather than digital technology. The idea of the current sensing scheme is almost the same as a cascode circuit which can increase the bandwidth or decrease the response time of an amplifier circuit by suppressing the voltage swing on the load capacitance. Hence, it suggests that the introduction of analog circuit techniques to digital circuits is one effective solution that addresses the LV/LP issues for the digital LSI"s.

IV. Low Voltage Analog Circuits

As mentioned before, it is very difficult to discuss LV/LP issues for analog circuits in general. However, there are the two following common issues for the analog circuits:

1) Degradation of SNR and accuracy.
   One issue for low voltage design of analog circuits is the degradation of Signal-to-Noise Ratio (SNR) and the accuracy. The SNR and the accuracy are likely to degrade when signal dynamic range reduces according to the reduction of operating voltage because the noise level is constant even when reducing the operating voltage.
2) Degradation of the performance by the simplification of circuits.
   Another issue is how to realize high performance in analog circuits with a small element count in the current path between the power supply terminal and ground. The lowest operating voltage is mainly determined by the element count in the current path, the necessary applied voltage for each element, and the dynamic range of signals. This means, however, we can not use several circuit techniques, such as a cascode circuit, emitter follower circuit, or Darlington circuits to improve the circuit performance. These are useful for increasing the bandwidth and the linearity, and for reducing the signal distortion.



(a) (b)

Fig. 7. Bit-line sensing circuit and its delay time: (a) Bit-line sensing circuit, (b) BL-sensing delay versus V_T of NMOS S/A Tr.

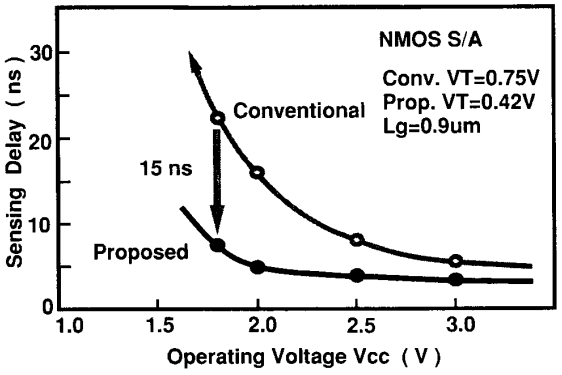


Fig. 8. Sensing delay versus operating voltage.

Thus, I will show some examples of low voltage analog circuit design which are currently used or will be used in portable equipment. They suggest typical low voltage techniques and their limitations.

A. Operational Amplifier

The operational amplifier is the most basic circuit for analog IC. Hence, the discussion of how circuit performance of the operational amplifier will be affected by the reduction of the operating voltage will indicate some basic viewpoints of low-voltage analog circuit design.

1) CMOS operational amplifier: Fig. 9(a) shows a basic circuit of the CMOS operational amplifier. The minimum operating voltage can be given by the following equation:

$$Vdd = VT_p + Vdss1 + Vdss2 + Vdss3 \qquad (1)$$

VTp is a threshold voltage of the PMOS transistor, $Vdss1$, $Vdss2$, and $Vdss3$ are the voltages defined as follows:

$$Vdssi = \mathbf{Vgsi} - VTi \qquad i = 1, 2, 3 \qquad (2)$$

where **Vgsi**, VTi are the **gate-source** voltage and threshold voltage of the ith transistor. $Vdss$ means the minimum drain-source voltage for the transistor which can be operated in the saturation region. This $Vdss$ can be described as *the following equation approximately as long as the current-voltage characteristic of the transistor exhibits a basic square-law characteristic*:

$$Vdss = (2Id/(\mu Cox(W/L)))^{0.5} \qquad (3)$$

where μ is a mobility, Cox is the unit gate capacitance, W is the channel width, and L is the channel length. Hence, there are the three ways to reduce the minimum drain-source voltage $Vdss$:

(i) Reduce the drain current Id

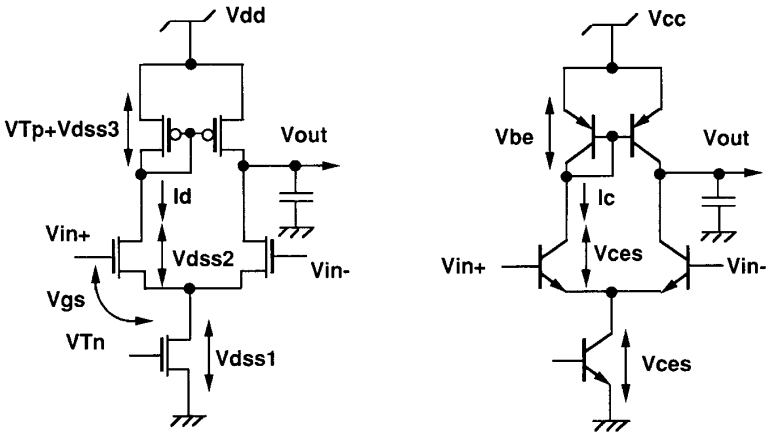
(ii) Increase the channel width W

(iii) Decrease the channel length L.

However, it is obvious that the reduction of the drain current, Id, will decrease the slew-rate and cutoff frequency of the amplifier. Also, wider channel width will decrease the cutoff frequency of the amplifier due to the increase of gate capacitance and drain junction capacitance. The shorter channel length will increase the band-width of the amplifier, even when using a low operating voltage. However, that will degrade DC characteristics such as VGS mismatch voltage, output resistance, and flicker noise level.

Fig. 10 shows the measured VGS mismatch voltage and output resistance versus channel length, where the channel width is 40 μm, the thickness of the gate-insulating oxide is 20 nm, and the drain current is 50 μA. The VGS mismatch voltage increases and the output resistance decreases with decreasing channel length. The increase of the VGS mismatch voltage will decrease the conversion accuracy of the A/D converter. Also, the decrease of the output resistance will decrease the conversion accuracy of the current-controlled D/A converter. Thus, it is obvious that the analog performance of the CMOS operational amplifier will degrade with reducing the operating voltage.

2) Bipolar operational amplifier: In contrast, the bipolar operational amplifier can operate without serious degradation of the analog performance, even when using low operation voltage. Fig. 9(b) shows a basic bipolar operational amplifier.



(a) (b)

Fig. 9. Basic CMOS and bipolar operational amplifiers: (a) CMOS operational amplifier, (b) Bipolar operational amplifier.

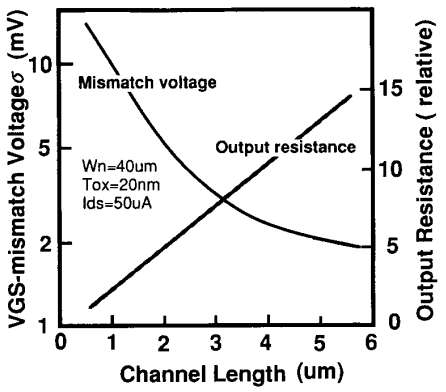


Fig. 10. VGS-mismatch voltage and output resistance versus channel length.

The minimum operating voltage Vcc can be described as following equation:

$$Vcc = Vbe + 2Vces \tag{4}$$

where Vbe and $Vces$ are the base-emitter voltage and the saturation voltage in collector region. The Vbe and $Vces$ can be set to 0.7 and 0.1 V, respectively, and Vcc can be obtained as only 0.9 V.

The cutoff frequency of this circuit will be mainly determined by the operating current and will decrease slightly as the operating voltage decreases due to the increase of junction capacitances such as Cjc and Ccs. Fig. 12 shows the bipolar operational amplifier used in portable tape-recorders [7]. The minimum operating voltage is only 0.9 V. The smart use of the complementary circuit realizes the low-voltage operation for the audio circuits.

B. Recording/Playback Amplifier

The inductor can generate a high voltage by driving in AC current. Hence, by changing the driving mode from the voltage-control to the current-control, the power supply voltage of recording/play back amplifier can be reduced [8].

Magnetic recording heads need high driving voltage. This is because voltage induced in the magnetic video-recording head, Vh, can be described as follows:

$$Vh = 2\pi f L Io \tag{5}$$

where f is the frequency of the driving signal, L is the inductance of the magnetic recording head, and Io is the driving current. In the SVHS system, the frequency f is 7 MHz, the inductance L is 9 μH, and the driving current Io = 15 mA; hence Vh is 5.9 Vpp. A conventional voltage controlled driving circuit of the magnetic recording head uses the push-pull output stage, as shown in Fig. 11(a). In this circuit, the output voltage, Vo, swings from $Vces$ of the output NPN transistor to Vcc-$Vces$ of the output PNP transistor. If both $Vcess$ are 0.5 V, the Vcc needs more than 6.9 V. Hence, this conventional voltage-controlled driving circuit is improper to the battery operated products.

On the other hand, the current-controlled driving circuits used in this camera-recorder system, as shown in Fig. 11(b) can reduce the power supply voltage to 3.5 V. The output voltage, Vo, swings between $Vcc \pm \pi f L Io$. Hence, Vcc needs more than only $\pi f L Io + Vces$. As a result, Vcc in these driving circuits can be reduced to 3.5 V.

C. Analog Video Signal Processing

In contrast with the fact that analog audio circuits have already attained the reduction of operating voltage to 1.5 V, the operating voltage of analog video processing circuits has not been reduced to less than 5 V. One reason for this is that balanced modulation circuits are used in analog video signal processing to realize many functions, such as electric volume, FM demodulator, gain controller of both audio signal and video signal, phase comparator, automatic phase controller of color signal, color killer, and multiplier.

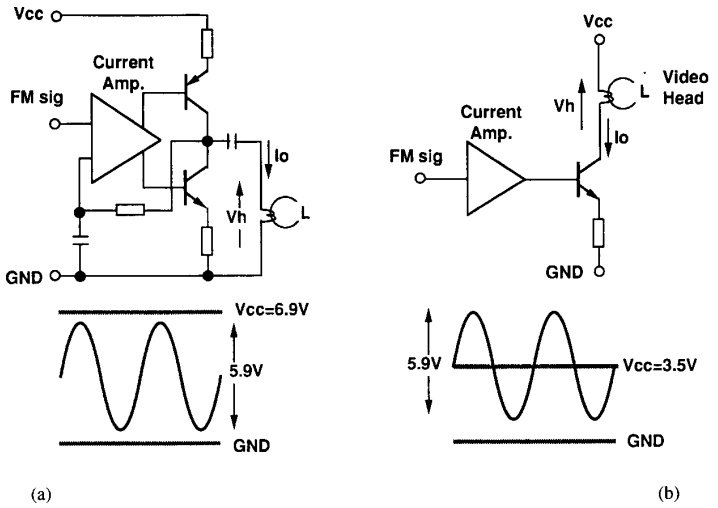


Fig. 11. Driving circuits for magnetic recording head: (a) Voltage drive, (b) Current drive.

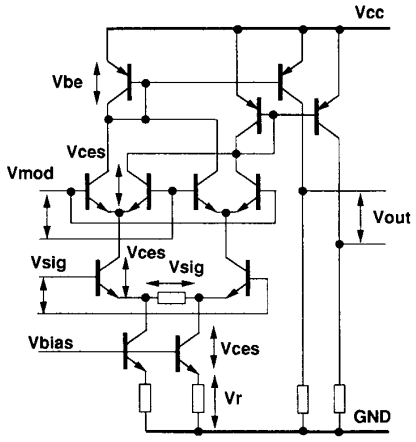


Fig. 12. Basic balanced modulation circuit.

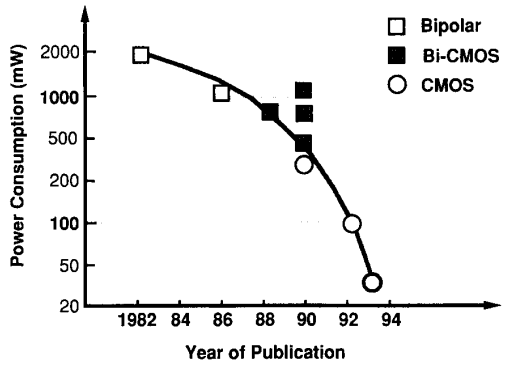


Fig. 13. Progress in power consumption of video-rate 10-b ADC.

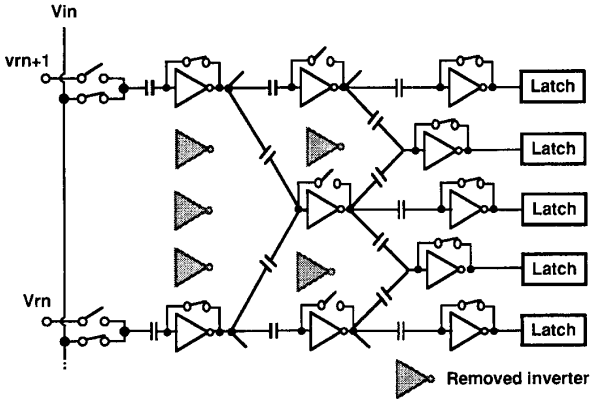


Fig. 14. Main circuit scheme of the A/D converter.

About 20 balanced modulation circuits are used in the color signal processing IC. Thus, the reduction of the operating voltage of the balanced modulation circuit is a key point for reducing the operating voltage in an analog video signal processing IC [8].

Fig. 12 shows the basic balanced modulation circuit. The required power supply voltage Vcc of this circuit can be described as

$$Vcc = Vr + Vsig + 3Vces + Vbe \tag{6}$$

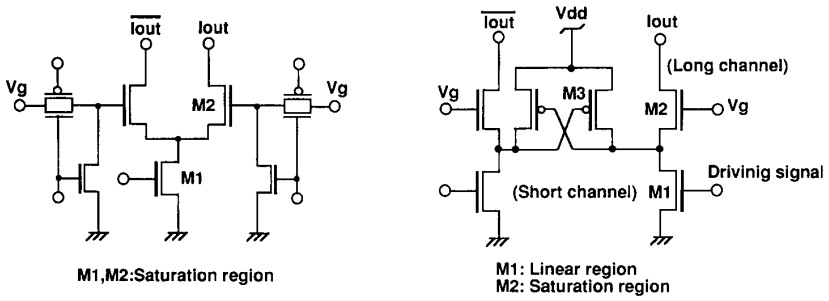
where, Vr is the common emitter biasing voltage of transistors forming current sources, and $Vsig$ is the swing voltage of the analog input signal.

Vcc of 2.8 V can be obtained when Vr is 0.2 V, $Vsig$ is 0.4 V, $Vces$ is 0.5 V, and Vbe is 0.7 V.

This analog video signal processing circuit is constructed with stacked connections of transistors so that a higher power supply voltage of about 3 V is needed.

D. A/D Converter

A/D converters are indispensable to digital signal processing, and the LV/LP circuit design is strongly needed.



(a) (b)

Fig. 15. Current sources of video-rate DAC: (a) Conventional, (b) Proposed.

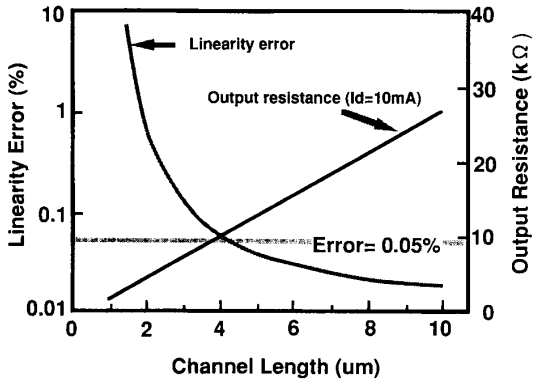


Fig. 16. Output resistance and the linearity error versus channel length.

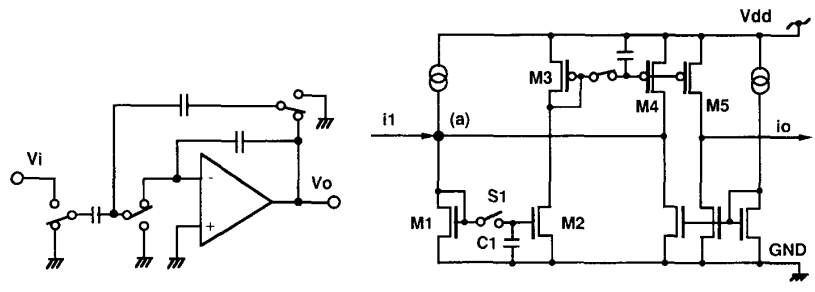
Presently, 8-b video-rate A/D converters are used, and 10-b resolution will be needed for future products. However, it has been impossible to use the video-rate 10-b A/D converter in portable equipment due to its large power consumption. Fig. 13 shows the progress in power dissipation of the video-rate A/D converter. Until 1990, they have had unacceptable power consumption of more than 250 mW [9]. However, recently, a very low power A/D converter consuming only 100 mW has been announced [10]. But it needs dual power supply voltages of 3.5 V and 5.0 V. This somewhat higher power supply voltage is due to the CMOS operational amplifier circuits, used in sample-and-hold circuits and subranging/amplifier circuits in the sub-ranging A/D conversion scheme. Hence we have developed the video-rate 10-b A/D converter whose power consumption is only 30 mW with a single power supply voltage of only 2.5 V [11]. We achieve this LV/LP operation by using chopper/inverter circuits, instead of operational amplifiers. Although the chopper/inverter circuit has a somewhat large offset voltage caused by the charge feed-through and is likely to suffer from a noise problem, we have improved this issue by using a capacitive interpolation scheme which can reduce the contribution of the offset voltage to the differential nonlinearity error (DNL) and by reducing the operating voltage for the suppression of the noise voltage.

Fig. 14 shows the main circuit diagram of the 10-b A/D converter. The conversion scheme of the A/D converter is based on the two-step parallel conversion scheme [12] and modified with the new circuit technique called capacitive interpolation. This new circuit scheme can be obtained to remove the gray inverters from the conventional three-stage chopper/inverter circuit and to connect the residual one and the adjacent output terminals to the input terminals of the next stage inverters through the capacitors. In this scheme, a series of reference voltages divided equally by four between the reference voltages can be obtained by the interpolation. This circuit scheme can suppress the influence of the offset mismatch of the inverter on the differential non-linearity error by a factor of four without any operational amplifier. Furthermore, this circuit scheme can reduce both operating voltage and the power consumption. This is because it contains only inverters, switches, and capacitors and these elements can be operated with a low power supply voltage of 2.0–2.5 V. Also, the reduction of the number of inverters contributes to the reduction of power consumption. As a result, this video-rate 10 b A/D converter can operate with a power supply voltage of 2.5 V and consumes only 30 mW at the conversion frequency of 20 MHz. The combination of the simplification of the circuit with a simple correction scheme is one way to realize high performance LV/LP data-converter circuit design.

E. D/A Converter

Video-rate 8-b D/A converters have already attained 3.5 V operation. Recently, a video-rate 10-b D/A converter with 2.7 V operation has been reported [13]. In the D/A converter, the lowest operating voltage is mainly determined by the current-constancy of the current source which will degrade rapidly when the operation mode of MOS transistor forming current source falls into the linear region. Hence, it is important for design of D/A converter to keep the transistor that forms the current source in the saturation region, under a low operating voltage condition.

Fig. 15(a) shows the conventional current source of the video-rate D/A converter. In this scheme, the lower limit of the bias voltage, Vg, is determined by the sum of threshold voltages of $M2$ and the saturation voltage of $M2$ and $M1$. Assuming the saturation voltages are all 0.8 V, and the threshold voltage of $M2$ modulated by a back-gate bias effect is 1.3 V, the voltage Vg becomes 2.9 V. As a result, it is very difficult to reduce the operating voltage of less than 3 V.



(a) (b)

Fig. 17. Switched capacitor filters: (a) Voltage mode SC filter, (b) Current mode SC filter.

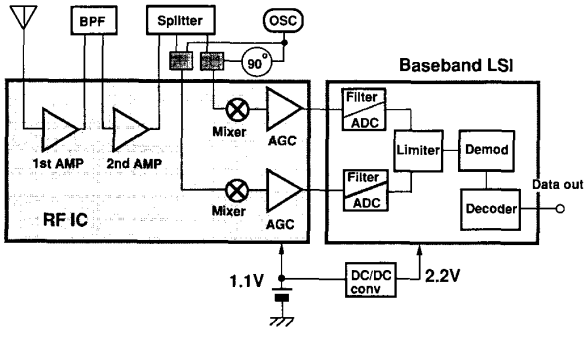


Fig. 18. Block diagram of paging receiver system.

To address this difficulty, $M1$ is allowed to operate in linear region and the gate length of $M2$ is increased to maintain the constancy of the current source. Fig. 16 shows the output resistance and linearity error versus the channel length of the transistor. The output resistance is proportional to the channel length, and the linearity error in log scale is inversely proportional to the channel length. Fig. 15(b) shows the new current source where $M2$ is operated in the saturation region, and $M1$ is operated in the linear region. In contrast with the conventional current source, the gate voltage of $M2$ is fixed and the gate of $M1$ is switched in order to avoid heavy gate capacitance of $M2$. Moreover, transistor $M3$ is used to decrease the settling time. As a result, this video-rate 10-b D/A converter can operate with a power supply voltage of 2.7 V, even when the conversion frequency is 50 MHz.

F. Filter

Analog pre- and post- analog filters are indispensable for digital signal processing, so that these circuits will remain even when almost all the analog signal processing circuits change to digital signal processing circuits. Fig. 17(a) shows a conventional switched capacitor circuit which is currently used for pre- and postfilters. This circuit operates in voltage control mode, so that the operating voltage can not be reduced due to large signal swing.

Fortunately, a new analog filter circuit which operates in current control mode with low operating voltage has recently emerged [14].

Fig. 17(b) shows the emerged analog filter circuit. Signals are added or subtracted at point (a) in current mode and are converted to the small voltage, whose magnitude reflects the processed current, by the diode-connected transistor $M1$. This voltage is sampled with capacitor $C1$ and transferred to transistor $M2$ through switch $S1$. As a result, the current flowing through transistor $M2$ has equal magnitude to the current being added or subtracted at point (a). The information of the processing signal transfers to transistors $M4$ and $M5$ in current mode, and the magnitude of output currents from transistors $M4$ and $M5$ are proportional to the current flowing through the transistor $M1$.

The transfer function of this circuit can be described as

$$H1(z) = io(z)/i1(z) = Az^{-1}/(1 - Bz^{-1}) \qquad (7)$$

which corresponds to a forward Euler transformation of a non-inverting lossy integrator. Also, some other functions such as the backward Euler transformation and bilinear-z transformation can be easily obtained.

This analog filter circuit has a hopeful potential for realizing low voltage operation due to its small signal swing and small number of elements between the power supply and ground.

This technology has not matured, and more investigations for realizing high accuracy, high SNR, high stability, and high tolerance for the fluctuation of device parameters shall be accomplished. However, the idea of processing analog signal in current mode may indicate the future direction of analog circuit design for realizing low voltage operation.

G. RF circuits

Wireless communication is a key technology not only for future personal telecommunication systems but also for personal multimedia systems. Thus, low-voltage RF circuits become more important for future portable equipment. Some wireless communication products have already realized one-battery operation. Fig. 18 shows the block diagram of a low voltage paging receiver system [15]. The system contains an RF chip and a baseband chip. The RF chip fabricated with bipolar technology can operate with one-battery voltage of 1.1 V and the baseband chip fabricated with CMOS technology can operate with up converted voltage of 2.2 V. The RF chip contains the first and the second amplifiers, mixers, and

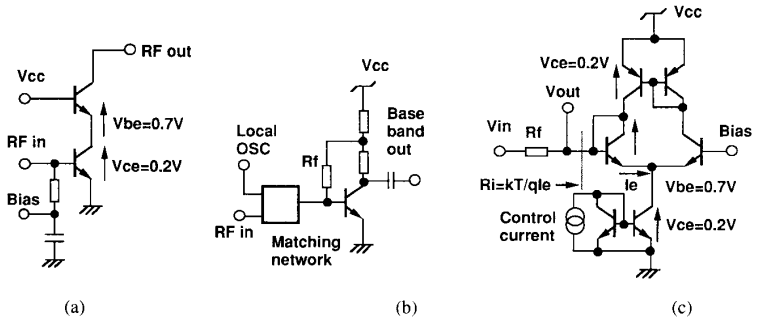


Fig. 19. Low-voltage RF circuits used in the paging system: (a) RF amplifier, (b) Mixer, (c) AGC.

AGC's. Fig. 19 shows the low-voltage RF circuits. The small signal RF amplifier is constructed with **cascode**-connected transistors. The mixer is realized with only one transistor. The two input signals drive the base of transistor through the matching network and the lower beat component between two signals is output to obtain baseband signal. The AGC function is obtained with the combination of the fixed resistance with operational trans-conductance circuit. By using a complementary circuit, the low-voltage operation of 1.1 V is realized.

V. Mixed Analog/Digital Technology

Mixed analog/digital circuit is a key technology for portable equipment. Even though much complicated digital circuits will be used, analog circuits will remain for processing or interfacing of the input and output analog signals. However this means that we must address some tough issues.

The main problem of the mixed analog/digital LSI is the invasion of noise from the digital circuits to the analog circuits. This will become serious when the dynamic range of the analog signal is lowered according to the reduction of power supply voltage. One counter measure is the reduction of the logic swing in a digital circuit. This method is very effective for both suppressing internal noise and suppressing an external noise. The measured noise power for an external logic swing of 1.2 V is over 20 dB smaller than that for external logic swing of 5 V, as shown in Fig. 20 [16]. This result indicates that low voltage design for digital circuits will bring many benefits for realizing high performance mixed analog/digital LSIs.

Another problem for mixed analog/digital LSI is the difficulty of reducing operating voltage and power consumption in the analog circuits.

It is obvious that almost all the analog signal processing circuits can be changed to digital signal processing circuits in the future. Digital signal processing can easily attain good processing qualities such as good accuracy, good SNR, and good stability. Also, the chip size and the power consumption will decrease rapidly with the reduction of design rule and followed low voltage. In contrast, analog circuit can not improve its circuit performances by only reducing the design rule. A magnitude of 1/f noise in a MOS transistor is inversely

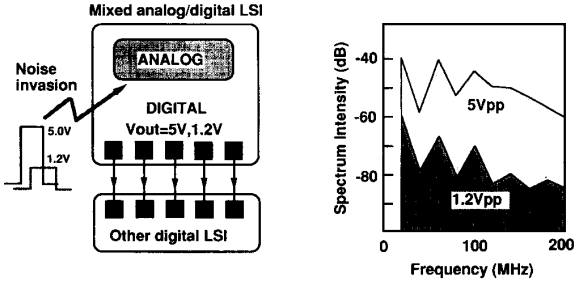


Fig. 20. Noise problem of mixed analog/digital LSI: (a) Experimental setup, (b) Noise spectrum.

proportional to the gate area, and the VGS mismatch voltage of a transistor pair is inversely proportional to the channel length, so that the chip size of an analog MOS circuit can not be reduced drastically with the reduction of the design rule. Consequently, the analog circuits which can not be changed to digital circuits will remain and become main obstacles in the reduction of both operating voltage and power consumption in mixed analog/digital LSI's.

Fig. 21 shows the estimation of power consumption and occupation ratio for categorized circuit blocks in a digital video-camera system with a reduction of LSI design rule. In this system, almost all the analog circuits have been already changed to the digital circuits. Power consumption in digital circuits will decrease rapidly with the decrease in design rule and operating voltage. In contrast with digital circuits, the power consumption of analog circuits will decrease moderately with the progress of LSI technology. As a result, in the first generation system which uses 1.2-μm CMOS, the occupation of digital circuits and analog circuits for total power consumption are 58% and 42%, respectively. Hence, digital circuits are the main issue in saving power. However, in the third generation system which will use 0.5-μm-rule CMOS, the contributions of digital circuits and analog circuits are estimated as 39% and 61%, respectively. Analog circuits will be the main obstacle for saving power in the future. Hence, LV/LP analog circuit design will be strongly needed for future mixed analog/digital LSI's in future portable equipment.

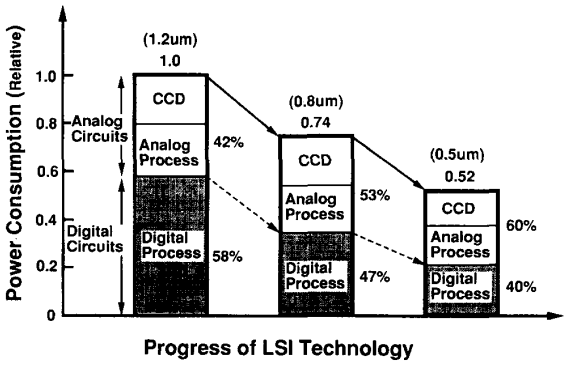


Fig. 21. Estimated and categorized power consumption of the digital camera system with the reduction of design rule of LSI.

VI. Conclusion

The circuit technology used in portable equipment is changing the conventional analog technology to a mixed analog/digital technology. LV/LP circuit design is strongly needed for both analog and digital circuits to increase playing time and to decrease the number of batteries and the weight, volume, and operating temperature of the equipment. In the digital LSI, short channel devices, independent operational blocks which can exclude the heavy load capacitances on the bus line in particular, and parallel schemes which can operate with the slower clock, are useful for the reduction of operating voltage and power consumption. Also, implementations of some analog circuit techniques such as current mode operation with a cascode circuit and the partial reduction of the threshold voltage are useful and may indicate the future direction of the LV/LP circuit techniques in digital LSI.

In analog LSI, complementary circuits, and optimized and simple circuit design are useful for LV/LP circuits. Also, novel circuit schemes such as capacitive interpolation and switched current circuit are useful and may indicate the future direction of the LV/LP circuit techniques in analog LSI.

However, there are fundamental difficulties for realizing high performance analog circuits. Examples are the degradation of SNR caused by the small signal dynamic range in the low voltage operation, and a difficulty in how to make high performance analog circuits with few elements between the power supply voltage and ground. As a result, the progress of the LV/LP circuit design will be slower than that of the digital circuit design. The total power consumption of the LSI circuits in some portable equipment will be dominated by analog circuits. One practical solution for this issue is to provide the optimized multiple power supply voltages for the circuit blocks in one LSI.

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