Special Brief Papers

A Self-Biased Feedback-Controlled Pull-Down Emitter Follower for High-Speed Low-Power Bipolar Logic Circuits

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Abstract—**A feedback-controlled active-pull-down emitter follower that is self-biased at a low steady-state current and allows the collector dotting and emitter dotting is proposed for high-speed low-power bipolar/BiCMOS digital logic circuits. The push–pull operation of this emitter follower is precisely controlled by a feedback mechanism and does not require any extra out-of-phase signal other than the emitter-follower input from the logic stage. Simulation results based on a 0.5-μm advanced Si-bipolar technology show that the pull-down delay and drive capability of a loaded 1-mW feedback-controlled pull-down ECL gate are improved to the pull-up levels, 2.7 and 10 times better than those of the conventional resistor-pull-down ECL circuit, respectively.**

I. Introduction

To realize high-performance bipolar/BiCMOS digital VLSI chips with manageable power consumption, individual gates such as emitter-coupled logic (ECL) or non-threshold logic (NTL) need to be fast while consuming little power, especially in the emitter-follower output-driving stages. The conventional resistor-pull-down (RPD) emitter follower (EF) used in bipolar logic circuits (Fig. 1) is not appropriate for VLSI because its pull-down current (i_{PD}) and emitter-follower current (I_{EF}) are equal and not decoupled. Its disadvantage is the reciprocal relationship of pull-down delay and dc power, i.e., either slow pull-down at low power or high dc power at fast speed, although it has advantages in circuit simplicity, gate density, and versatile logic-implementation capability like emitter dotting and collector dotting.

To solve the problem of RPD (or passive-pull-down, in general) emitter follower, various active-pull-down (APD) circuits such as the turbo ECL or ac-coupled APD ECL, super push-pull NTL, and Darlington ECL have been proposed [1]–[3]. A typical technique used in these APD circuits is, as shown in Fig. 2(a) for the ac-coupled case, to set the steady-state emitter-follower current low with extra bias circuitry and momentarily boost the transient pull-down current through the capacitive coupling of out-of-phase signal $\overline{X}$ from the logic stage. Although this APD circuit has advantages of push–pull transient and balanced high-speed pull-up/down with low dc power, it suffers from disadvantages such as circuit or technology complexity and gate area, extra loading on $\overline{X}$ in the logic stage, limited logic implementation without emitter-dot and collector-dot, and no push-pull timing control. For example, if the logic is implemented with collector-dot or cascode, the complementary signals required for the push–pull action are not always available ($Y1$ instead of $\overline{X1}$ in Fig. 2(b)). Also, if the emitter-follower outputs are dotted to implement wired-OR, it is not simple to get a correct out-of-phase signal for pull-down path. Finally, because X and $\overline{X}$ are potentially skewed in time, the pull-down current may be boosted too late or may return to steady-state value prematurely before the output completes a transition. Although the JFET APD circuit [4] using in-phase signal only for the push–pull may solve these problems, its performance improvement is not impressive.

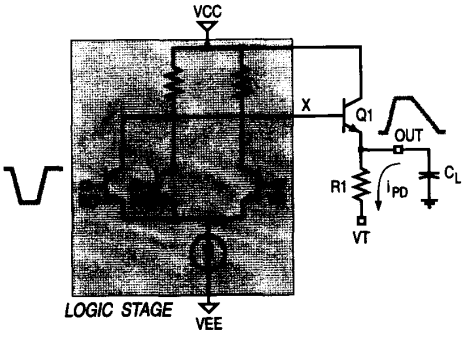

Fig. 1. Conventional resistor-pull-down (RPD) emitter follower (EF) for ECL/NTL.

In this paper, a novel self-biased feedback-controlled pull-down (FPD) emitter follower that solves all the problems of conventional APD circuits and yet demonstrates a superior performance is presented for high-speed low-power bipolar logic circuits [5]. Section II describes the FPD emitter follower with details on self-biasing, push–pull transient behavior, and emitter-dotting. In Section III, simulation results are compared to demonstrate the advantages of the FPD circuit.

II. Feedback-Controlled Pull-Down Emitter Follower

The feedback-controlled pull-down emitter follower with self-biasing is shown in Fig. 3. It consists of an emitter-follower transistor $Q1$, a pull-down transistor $Q2$, current setting resistors $R1$ and $R2$, a level-shifting/coupling diode $D1$, and an optional clamping diode $D2$. The circuit is very effective because biasing, inverting, level-shifting, and

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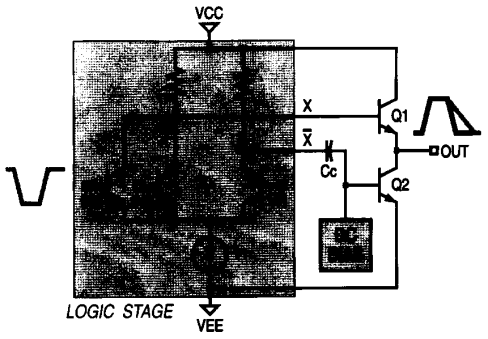
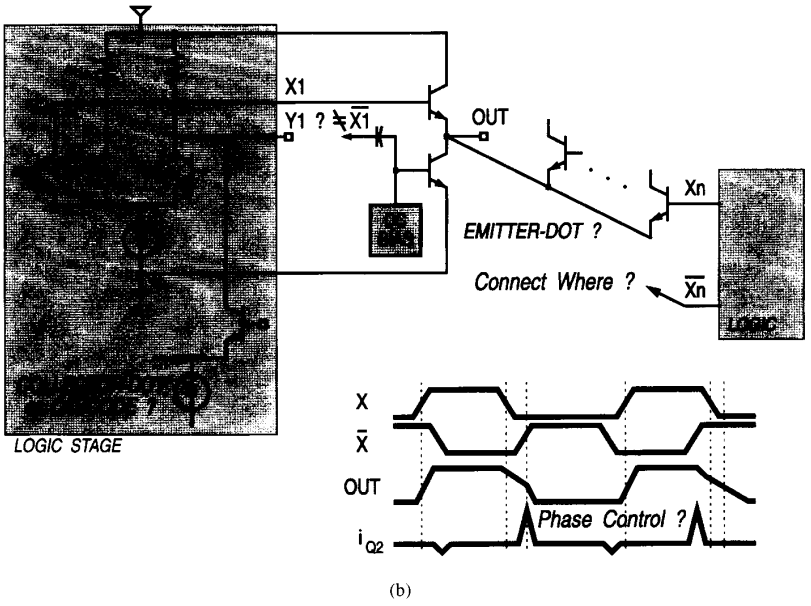


(a)



(b)

Fig. 2. (a) Conventional active-pull-down (APD) emitter follower with ac coupling and (b) its disadvantages of lacking collector dotting, emitter dotting, and push–pull timing control.

coupling functions are merged into this simple topology. It uses only one signal X from the logic stage, does not need capacitors (that means dc-coupled), is self-biased at constant current, and allows VT termination rather than VEE ($V_{CC} - V_T < V_{CC} - V_{EE}$). Its advantages include high-speed pull-up/down with low dc power, feedback-controlled precise push-pull transient, circuit simplicity and gate density, minimum loading on the logic stage, logic versatility like emitter/collector dotting, and low output impedance. Because the circuit requires three more devices than RPD-EF and no area-consuming capacitor (compared to APD-EF) and is topologically simple with one signal (X) involved, it can be easily laid out with reasonable real estate on chip.

The steady-state bias current ($\equiv I_{EF}$) of the FPD circuit is simply self-determined by the resistor values, supply voltages, and diode drops. In normal steady states where $Q1$ and $Q2$ are not saturated for given V_T, V_{CC}, and signal swing, $Q1$ can be considered as a short circuit because it passes all the

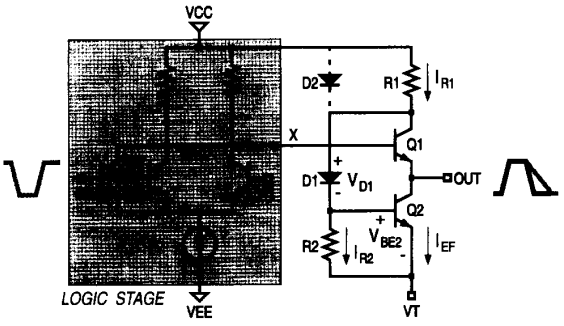


Fig. 3. Feedback-controlled pull-down (FPD) emitter follower circuit.

$Q2$ current I_{EF}, if the base currents are ignored. The voltage across $R1$ is, then, $V_{CC} - V_T - V_{BE2} - V_{D1}$ and I_{R1} is determined accordingly. Because $I_{R2} = V_{BE2}/R2$, I_{EF} which

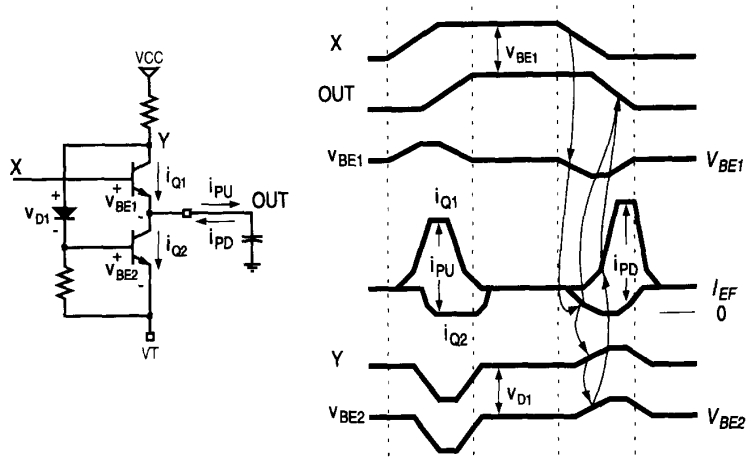


Fig. 4. Feedback-controlled push-pull operation of FPD-EF.

is equal to $I_{R1} - I_{R2}$ becomes $(V_{\rm CC} - V_{\rm T} - V_{\rm BE2} - V_{D1})$ $/R1 - V_{\rm BE2}/R2$.

The push–pull operation of the FPD circuit during transient periods is efficiently controlled through a negative feedback as illustrated in Fig. 4. When X rises from low to high, the output OUT follows with a delay causing an increase of $v_{\rm BE1}$ and corresponding surge of the current i_{Q1}. The surge makes a dip of the voltage at node Y that, in turn, is transferred to the base of $Q2$ through $D1$. As a result, the current i_{Q2} drops and the net pull-up current $i_{\rm PU}$ increases. So the output rises fast and, as it approaches the high state, $v_{\rm BE1}$ and i_{Q1} return to the steady-state values and the push-pull action gradually comes to an end. When X falls from high to low, again because OUT follows with a delay, $v_{\rm BE1}$ is reduced for the transition interval. This successively turns $Q1$ off and raises Y. The surge of Y is coupled to the base of $Q2$, increasing i_{Q2} and the net pull down current $i_{\rm PD}$ substantially. Therefore, the output falls fast to the low state and the circuit returns to the steady-state as before. In net, the FPD-EF output moves much faster than the RPD circuit and its push–pull timing is well controlled unlike conventional APD circuits.

There are some design issues to consider for the FPD emitter follower. The first is a damped output ringing due to the feedback-loop delay. For example, when the output falls, the pull-down current overdischarges OUT and i_{Q1} increases. This, in turn, reduces i_{Q2} through the feedback loop, and OUT is charged up again, and so on. The second is potential saturation of $Q1$ and $Q2$. Here, the optional diode $D2$ can be used for clamping Y and preventing $Q1$ from saturating while $Q1$ serves to clamp OUT and keep $Q2$ from saturating. The third is optimizing the ratio of currents flowing through $R1$ and $R2$ for a given power to maximize the speed. The fourth is choosing a right $V_{\rm T}$ and minimizing noise on VT. VT should be a solid supply with low source impedance. $V_{\rm T}$ needs to be raised to minimize power dissipation but must be low enough not to saturate $Q2$. For a given $V_{\rm T}$, the diode $D1$ can be implemented with, e.g., a Schottky diode, a series of diodes, a MOSFET (in BiCMOS), or a diode-voltage multiplier to properly adjust V_{D1} to prevent saturation of $Q2$.

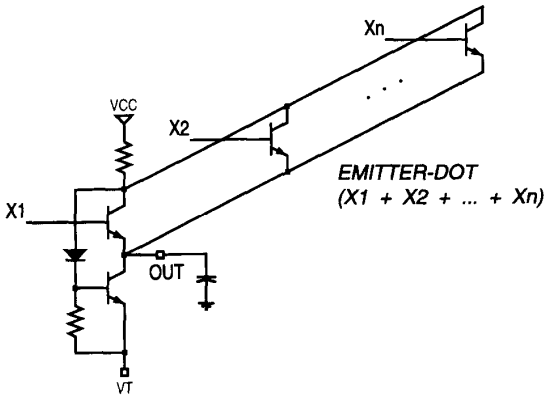


Fig. 5. Emitter-dotting of FPD-EF requires collectors of the emitter-follower transistors to be connected with an additional wire.

Because the FPD circuit needs the in-phase signal X only, collector dotting and cascoding is well permitted. Emitter dotting for FPD-EF is also feasible as depicted in Fig. 5 by separately connecting collectors of the emitter-follower transistors with one extra wire. This emitter-dotted circuit operates like the basic FPD circuit in Fig. 3 with $(X1 + X2 + \cdots + Xn)$ replacing X, although its performance depends on locality of the dots: The speed degrades for wide-spread dots because parasitic capacitance at the collector node increases.

III. Simulation Results and Comparison

To demonstrate the advantages of the FPD emitter follower, the RPD-ECL and FPD-ECL circuits have been compared for a nominal condition of $V_{\rm CC}/V_{\rm EE}/V_{\rm T}/V_{\rm R} = 3.6/0/1.5/2.2$ V (a typically accepted set) and 65°C. Simulated gates include unloaded inverter (Fan-In (FI) = Fan-Out (FO) = 1 and $C_L = 0$) and loaded 3-input NOR (FI = FO = 3 and

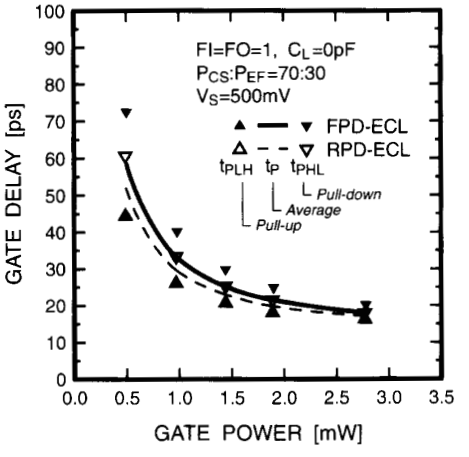


Fig. 6. Unloaded basic ECL (FI =FO = 1, $C_L = 0$) gate delay versus power consumption per gate comparison between RPD and FPD.

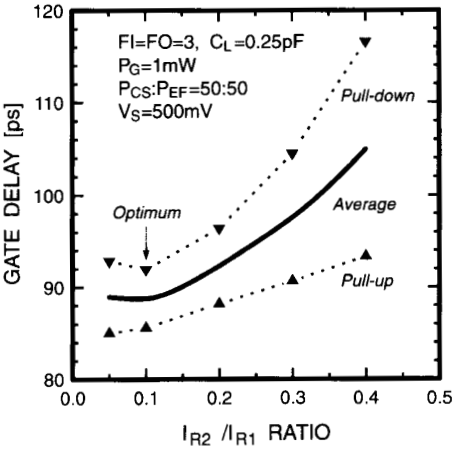


Fig. 7. Loaded FPD-ECL delay versus I_{R2}/I_{R1} current ratio.

$C_L = 0.25$ pF), without and with a 3-way emitter dotting. The signal swing is 500 mV without the emitter-dot and 600 mV with the dot. For the emitter-dot cases, the gates are assumed to be 100 μm apart. The technology assumed is a 0.5-μm double-poly SiGe-base heterojunction bipolar technology similar to [6] with a β of 120, f_T of 60 GHz, and emitter area of 0.5×1.0 μm^2 for the logic-stage devices. The emitter size of push-pull transistors $Q1$ and $Q2$ is 1.0×1.6 μm^2.

Fig. 6 summarizes the delay versus power consumption for the unloaded basic gates. The gate delays are minimized when nearly 30% of the total gate power is allocated in the emitter-follower stages. (P_{CS} refers to the power consumption in the logic stage and P_{EF} is the power in the emitter-follower stage.) The dc current densities for the logic and push-pull transistors are maximum for 3-mW gate and 1.16 and 0.27 mA/μm^2, respectively. Here, the FPD and RPD circuits have comparable delay-power characteristics; the average delay is about 30 ps at 1 mW/gate. Notice a little slower pull-down of FPD-ECL due to a smaller initial EF current when the output starts to fall from high.

For the loaded gates, the delays are minimized if approximately 50% of the gate power is consumed in the emitter-follower stages. In this case, the current densities for the logic and push-pull devices of 3-mW gate are limited to 0.84 and 0.44 mA/μm^2, respectively. As shown in Fig. 7 for a gate power of 1 mW, the FPD-ECL delay is further optimized when I_{R2}/I_{R1} ratio is set to 0.1. Fig. 8 compares the output waveforms and net output currents of the FPD-ECL and RPD-ECL circuits for a typical loaded case at 1 mW. The FPD-ECL output has fast and symmetric slopes for both pull-up and pull-down transitions and has a big and sharp pull-down current.

The performance leverage of the FPD circuit is displayed in the loaded gate delay versus power consumption plot in Fig. 9. Note that the pull-down delay of FPD-ECL is essentially equal to the pull-up delay and, for 1 mW/gate, it is improved from 247 ps of RPD-ECL to 92 ps by a factor of about 2.7. From the power savings point of view, the FPD-ECL circuit

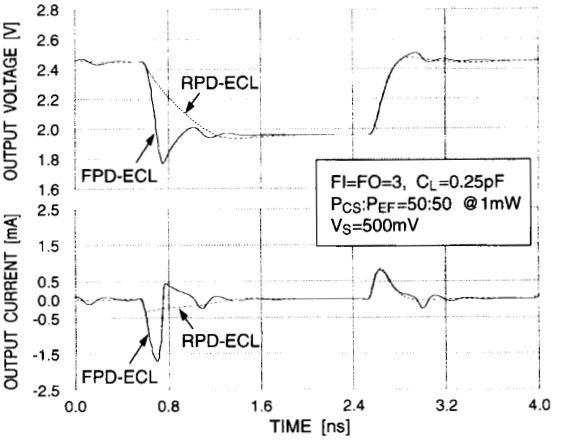


Fig. 8. Output waveforms and currents for loaded RPD and FPD ECL gates.

consumes nearly 2.8× less for the same delay. On the average, the improvement is about 2× for delay or power.

The superior load drive-capability of the FPD-EF circuit is shown in the delay versus load capacitance curve (Fig. 10). At 1 mW/gate, the pull-down drive-capability of FPD-EF is almost identical to the pull-up capability and pull-down is even faster than pull-up for heavy loads. The pull-down drive capability of the FPD circuit is enhanced by about 10× from 916 ps/pF of the RPD circuit. The average drive-capability is improved from 530 to 98 ps/pF by a factor of 5. Of course, the RPD gate at 1 mW would not be optimum for driving a large load capacitance like 1 pF because of the severe pull-down vs. pull-up skew in delay. The gate would be suitable to drive 0.25 pF with a reasonable skew of 2 to 3. For driving a heavier load with an adequate skew, the RPD gate needs to be powered up. Since the power-up will be roughly proportional to the load, the product of drive-capability (as represented by the slope) and power will remain relatively constant. Therefore, it would be more accurate to interpret the result in Fig. 10 in

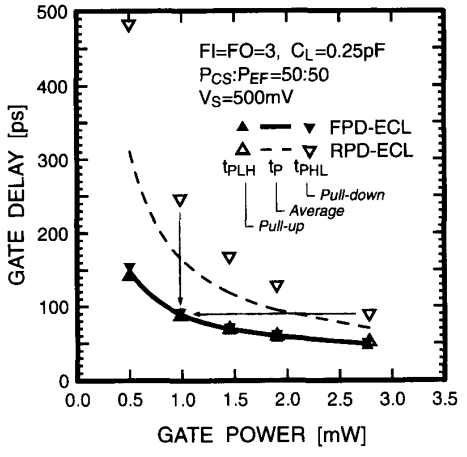


Fig. 9. Loaded ECL (FI = FO = 3, C_L = 0.25 pF) gate delay versus power consumption comparison between RPD and FPD.

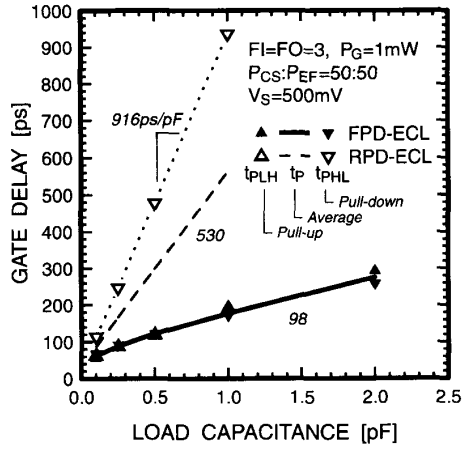


Fig. 10. Loaded gate delay versus load capacitance comparison between RPD and FPD ECL.

terms of drive-capability — power product, and the factors of improvement for FPD-EF are still valid.

The output ringing of the FPD-ECL gate has been observed. The frequency of ringing decreases with the load-capacitance increase, as expected, and the frequency and amplitude increase with the gate power, as shown in Fig. 11. The first cycle is for a 1.5-mW loaded gate, the second, 1-mW, and the last, 0.5-mW. Note that the ringing is not significant to cause any logic change and decays fast. For example, the maximum ringing amplitude for the 1.5-mW gate is about 80 mV, leaving a margin of 170 mV that ensures the logic state of any following ECL gate to be stable. The gate power should not be increased unreasonably for a given load and a transistor size, to prevent the ringing amplitude from becoming excessive.

To see the effect of emitter dotting, delay-power characteristics of the localized, 3-way emitter-dot loaded gates are

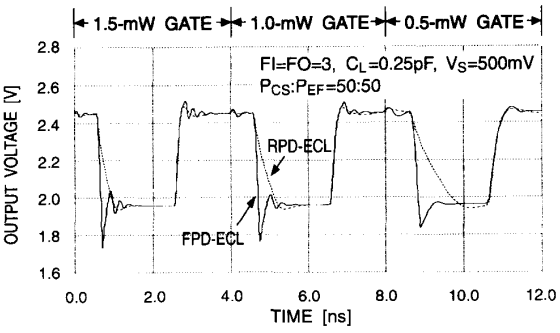


Fig. 11. Output ringing of loaded FPD-ECL gate (FI = FO = 3, C_L = 0.25 pF) for gate-power levels of 1.5, 1.0, and 0.5 mW compared with RPD-ECL.

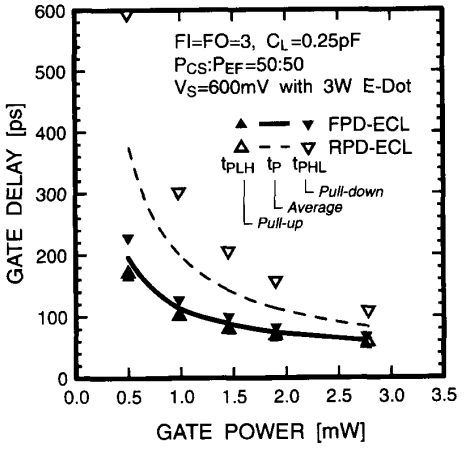


Fig. 12. Delay versus power consumption of 3-way emitter-dot gate with load compared between RPD and FPD ECL.

compared in Fig. 12. Leverage of the emitter-dot FPD-ECL over the emitter-dot RPD circuit is still large and it is roughly 2.4× for the pull-down speed and 1.8× for the average. The emitter-dotting does not affect the ringing characteristics except lowering the frequency due to extra feedback-loop delay.

IV. Conclusion

The self-biased feedback-controlled active-pull-down emitter follower proposed in this paper is a very efficient and superior circuit applicable to high-speed low-power bipolar/BiCMOS digital VLSI's. The circuit implements the biasing, inverting, level-shifting, and coupling functions to precisely control the push–pull operation with a small number of devices in a simple topology and shows a remarkable performance enhancement over the conventional resistor-pull-down circuit: 2.7× simulated pull-down speed and 10× drive capability for 1-mW loaded ECL gate. Also, the circuit allows versatile logic implementations through collector-dotting and emitter-dotting because it does not need any extra out-of-phase signal from the logic stage.

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