An Efficient Back-Bias Generator with Hybrid Pumping Circuit for 1.5-V DRAM's

Yasuhiko Tsukikawa, Takeshi Kajimoto, Yasuhiko Okasaka, Yoshikazu Morooka, Kiyohiro Furutani, Hiroshi Miyamoto, and Hideyuki Ozaki

Abstract—**An efficient back-bias (V_{bb}) generator with a newly introduced hybrid pumping circuit (HPC) is described. This system attains a V_{bb} level of −1.44 V at V_{cc} = 1.5 V, compared to a conventional system in which V_{bb} only reaches −0.6 V. HPC can pump without the threshold voltage (V_{th}) loss that conventional systems suffer. HPC is indispensable for 1.5-V DRAM's, because a V_{bb} level lower than −1.0 V is necessary to meet the limitations of the V_{th} of the access transistor. HPC uses one NMOS and one PMOS pumping transistor. By adopting a triple-well structure at the pumping circuit area, the NMOS can be employed as a pumping transistor without minority carrier injection.**

I. Introduction

In order to reduce power dissipation and improve device reliability, the operating voltage of ultra-high-density DRAM's is expected to be reduced to 1.5 V or further as the scaling proceeds below the half-micrometer region [2]. In previous generations of DRAM's, back-bias voltage (V_{bb}) has been utilized to reduce junction capacitance, improve cutoff characteristics of the transistors, enhance device isolation, enhance latch-up endurance, and take measures against undershoot of external signals. However, an excessively low V_{bb} deteriorates the data-holding characteristics of cell capacitors due to an increase in junction leakage. Until the present, there have been no factors that directly assign the absolute V_{bb} value.

At an operating voltage of 1.5 V, V_{bb} of the access transistor is required to be lower than −1.0 V in order to satisfy the limitations of the transistor threshold voltage (V_{th}). However, the V_{bb} level does not reach the required −1.0 V with conventional V_{bb} generators using two NMOS [3] or two PMOS charge pumping transistors, which suffer a voltage loss due to the V_{th} of the pumping transistors.

This paper describes an efficient V_{bb} generator with a newly introduced hybrid pumping circuit (HPC). This hybrid system uses one NMOS and one PMOS pumping transistor, and can pump as low as the $-V_{cc}$ level without V_{th} loss. HPC adopts a triple-well structure at the NMOS pumping transistor area, which prevents minority carrier injection.

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Y. Tsukikawa, Y. Okasaka, Y. Morooka, K. Furutani, H. Miyamoto, and H. Ozaki are with the ULSI Laboratory, Mitsubishi Electric Corporation, Itami, Hyogo, 664 Japan.

T. Kajimoto is with Kita-Itami Works, Mitsubishi Electric Corporation, Itami, Hyogo, 664 Japan.

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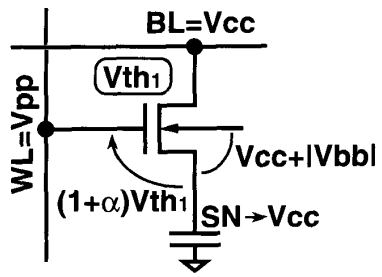


Fig. 1. Restoring operation.

II. Back-Bias Voltage of 1.5-V DRAM's

The requirement for the V_{th} of the access transistor in 1.5-V DRAM's is described. The upper limit of the V_{th} of the access transistor is determined in terms of word-line voltage, and the lower limit is set by the subthreshold leak. V_{bb} should be chosen such that the change of the V_{th} due to body effect is within the upper and lower limits.

Fig. 1 shows the access transistor and storage capacitor in the restoring operation. High level datum is restored from the bit line held at the V_{cc} level to the capacitor, whose storage node rises to the V_{cc} level. Thus this system works as a source-follower. At the end of restoring operation, the access transistor feels $V_{cc} + |V_{bb}|$ as an effective back-bias voltage. In order that the full V_{cc} level is restored to the capacitor, the access transistor is kept turned on during the restoring operation. Hence, for the boosted word-line voltage V_{pp},

$$V_{pp} > V_{cc} + (1 + \alpha)V_{th1} \tag{1}$$

where α is a voltage margin coefficient, assumed here to be 0.2, and V_{th1} is the threshold voltage of the access transistor when the effective back-bias is $V_{cc} + |V_{bb}|$. As long as V_{pp} is generated by a single boosting of V_{cc}, V_{pp} has its ideal value of 2 V_{cc} and is expected to be less than 1.7 V_{cc} in practice. Therefore, according to (1), the upper limit of V_{th1} is 0.88 V in 1.5-V DRAM's.

Fig. 2 shows the unselected access transistor and storage capacitor in the long tRAS ($\overline{RAS}$ active period) operation. The bit line has completed the sensing operation and is at ground level, while the stored charge leaks due to subthreshold leakage current I_L. Assuming a storage capacitance of 30 fF, a data holding time of 100 ms, and a lost charge by I_L within 5% of the stored charge, then subthreshold leakage is calculated to be less than 11 fA in 1.5-V DRAM's. According to Fig. 3, which shows the subthreshold characteristics of the access transistor (W = 10 μm), it can be seen that V_{th0}, the 1-μA-threshold

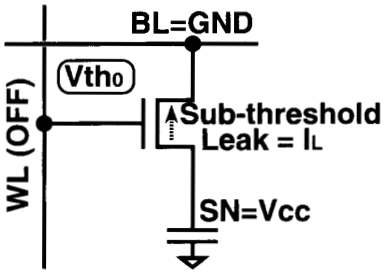


Fig. 2. Long cycle operation.

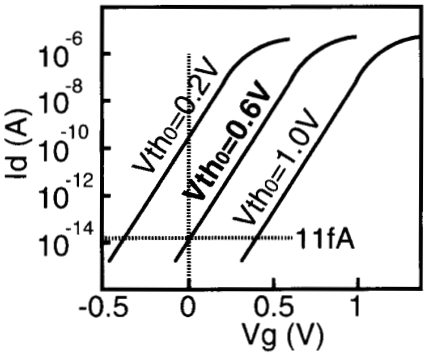


Fig. 3. Subthreshold characteristics of access transistor.

voltage with a grounded source, must be larger than 0.6V in order to satisfy the leakage limitation.

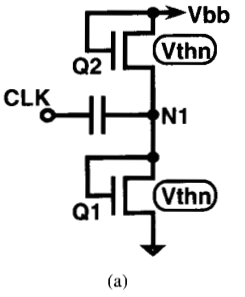
The above two restrictions of $V_{\rm th}$ generate the following equation with regards to $V_{\rm bb}$ [4],

$$K\{\sqrt{|V_{\rm bb}| + V_{\rm cc} + 2\phi B} - \sqrt{|V_{\rm bb}| + 2\phi B}\} < 0.28. \quad (2)$$

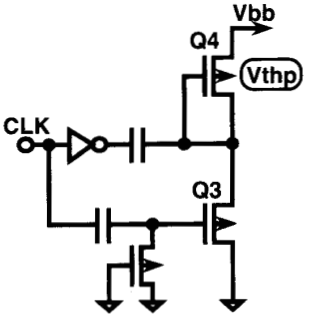
K is the body effect coefficient and assumed to be 0.59 $V^{1/2} \cdot \phi B$ is the potential difference between the Fermi level and the intrinsic Fermi level and has the value of 0.8 V approximately. Equation (2) leads to a result that a $V_{\rm bb}$ lower than -1.0 V is required in 1.5-V DRAM's. At high temperature, for example at 75°C, the subthreshold leakage becomes larger. In that case, the window of $V_{\rm th}$ becomes narrower than 0.28 V and the $V_{\rm bb}$ lower than -1 V would be necessary.

III. Circuit and Operation of HPC

Fig. 4 shows two conventional pumping circuits. In the circuit shown in Fig. 4(a), both pumping transistors, $Q1$ and $Q2$, are diode-connected NMOS's [3]. Here this system is called the NMOS system. A clock CLK is applied to the interconnection node $N1$, and negative charges flow from ground to $V_{\rm bb}$. Due to the diode connection, the final value of $V_{\rm bb}$ is 2 $V_{\rm thn} - V_{\rm cc}$, with a loss of $V_{\rm th}$ at $Q1$ and $Q2$ (2 $V_{\rm thn}$). The minority carrier injection also presents a problem in the NMOS system, because the n+ region of $Q1$ and $Q2$ is forward biased against the P-well when node $N1$ changes to a low level. In the circuit shown in Fig. 4(b), two PMOS's, $Q3$ and $Q4$, are used as pumping transistors. Here this system is



(a)



(b)

Fig. 4. Conventional pumping circuits. (a) NMOS system. (b) PMOS system.

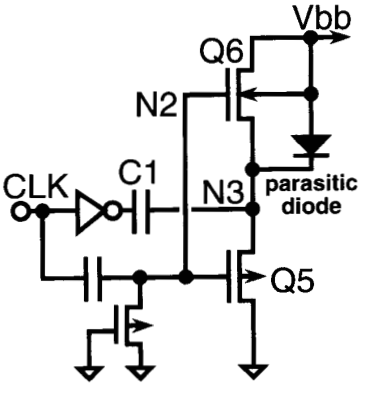


Fig. 5. Hybrid pumping circuit (HPC).

called the PMOS system. Since the gate voltage of $Q4$ only reaches $-V_{\rm cc}$, $V_{\rm bb}$ is not pumped lower than $|V_{\rm thp}| - V_{\rm cc}$ due to the $V_{\rm th}$ of the $Q4$ ($V_{\rm thp}$). Fig. 5 shows proposed HPC. $Q5$ transistor is a PMOS as in the PMOS system, and $Q6$ transistor is an NMOS with a parasitic junction diode.

The timing charge of HPC is shown in Fig. 6. When the clock CLK is at a low level, the voltage of node $N2$ reaches $|V_{\rm thp}| - V_{\rm cc}$, and $Q5$ clamps the voltage of node $N3$ to the ground level. When CLK changes to a high level, the voltage of $N2$ rises to $|V_{\rm thp}|$ and the voltage of $N3$, by capacitive coupling, becomes $-V_{\rm cc}$, causing $V_{\rm bb}$ to be equal to $-V_{\rm cc}$. It should be noted that when $N2$ is at a low level ($|V_{\rm thp}| - V_{\rm cc}$), $V_{\rm bb}$ is clamped at a level which is $V_{\rm thn}$ lower than the voltage

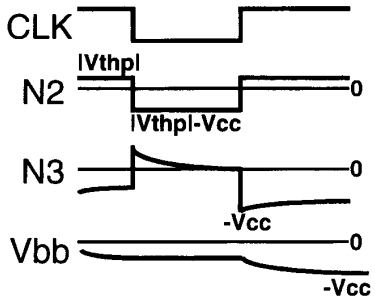


Fig. 6. Timing chart of HPC.

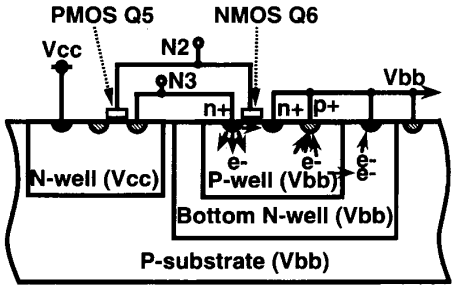


Fig. 7. Cross-sectional view of HPC.

of $N2$. Therefore, the exact form of V_{bb} will be

$$V_{bb} = \max\{-V_{cc}, |V_{thp}| - V_{cc} - V_{thn}\}. \quad (3)$$

By using HPC, no threshold voltage loss occurs in the generation of V_{bb}, which is able to reach the required negative voltage of $-V_{cc}$.

If we define the efficiency of a V_{bb} generator as $|V_{bb}|/V_{cc}$, the utmost efficiencies are 1–2 V_{thn}/V_{cc} for the NMOS system, $1 - |V_{thp}|/V_{cc}$ for the PMOS system, and 1 for HPC, respectively. HPC has the highest efficiency comparing to the other two methods.

IV. Triple-Well Structure

The NMOS transistor used in the V_{bb} pumping circuit has been the source of minority carrier injection. Injected carriers diffuse around the memory cell area and may destroy stored data. In HPC, a triple-well structure [5] in the pumping circuit has been introduced to prevent this injection. Fig. 7 shows the cross-sectional view of HPC. The NMOS transistor region is included in the bottom N-well. The bottom N-well, the P-well, and the P-substrate are connected to V_{bb}. Therefore, when node $N3$ sinks to $-V_{cc}$, electrons scattered from the n+ region to the P-well below are absorbed by either the P-well or the bottom N-well and do not diffuse out of the surrounding bottom N-well.

Fig. 8 presents another example of HPC. Fig. 8 differs from Fig. 7 in that the bottom N-well and the P-substrate are biased to ground level, and hence the bottom N-well is reverse-biased against the P-well. Therefore, a parasitic bipolar transistor is formed, consisting of the n+ region of $N3$ (emitter), the P-well

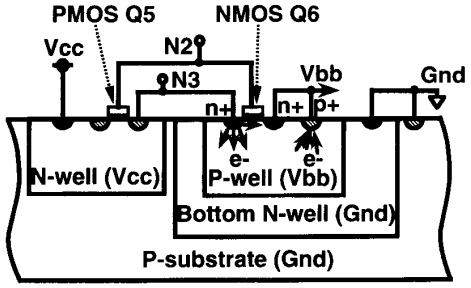


Fig. 8. Cross-sectional view of HPC with parasitic bipolar transistor.

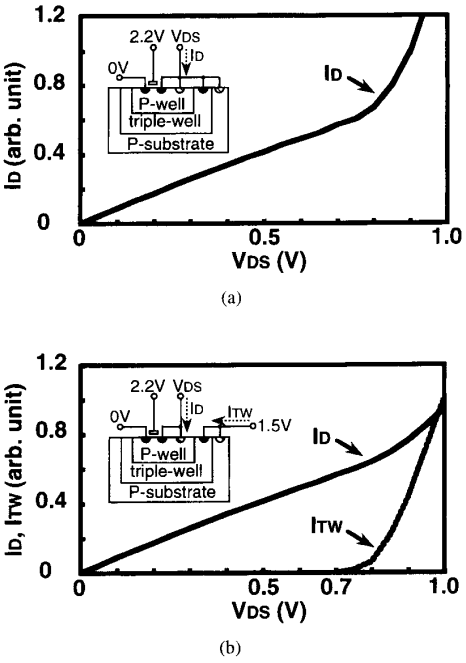
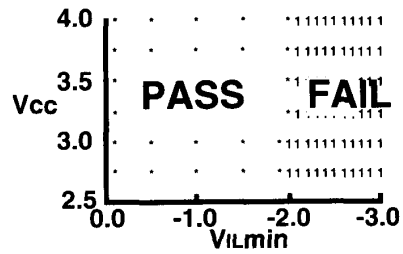


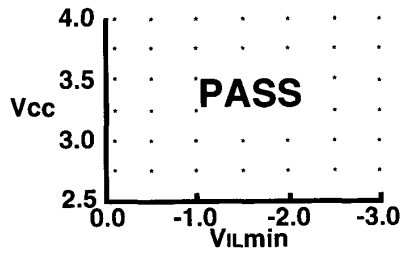
Fig. 9. DC characteristics of triple-well structure. (a) Without parasitic bipolar transistor. (b) With parasitic bipolar transistor.

(base), and the bottom N-well (collector). When $N3$ is lower than the P-well, scattered electrons from $N3$ may partially exit from the p+ region of V_{bb}, partially recombine with the holes, and partially penetrate through the P-well to the bottom N-well. If any electrons penetrate, they do not contribute to the pumping of V_{bb} and may deteriorate the efficiency of HPC. Whether the parasitic bipolar transistor turns on or not is verified by the dc measurement of the triple-well structure.

Fig. 9 shows the dc characteristics of the triple-well structure. In Fig. 9(a) the bottom N-well is shorted to the P-well which corresponds to Fig. 7, and in Fig. 9(b) the bottom N-well and the P-well are reverse biased, corresponding to Fig. 8. It can be seen in Fig. 9(b) that the parasitic bipolar transistor does not turn on as long as the voltage between the source and drain of the NMOS is less than 0.7 V. This is reasonable, taking the V_{BE} (base-emitter voltage) of a bipolar transistor into account. When $N3$ sinks, the source-drain voltage of $Q6$ is fairly smaller than V_{cc} because of the drain current of $Q6$.



(a)



(b)

Fig. 10. $V_{cc} - V_{I_{L\,min}}$ shmoo plot of test device. (a) Without triple-well. (b) With triple-well.

If we assume that capacitance $C1$ in Fig. 5 is 30 pF, the width/length of $Q6$ is 100 μm/0.5 μm, and the transition of clock CLK is set at 10 ns, then the source-drain voltage of $Q6$ is calculated to be 0.45 V. Therefore, the parasitic bipolar transistor does not turn on, and both Fig. 7 and Fig. 8 are applicable to HPC.

Absorption of the scattered electrons by the triple-well is assured through Fig. 10. Fig. 10(a) shows the $V_{cc} - V_{I_{L\,min}}$ shmoo plot of a test device without triple wells, and Fig. 10(b) shows that of a device with triple wells. Here $V_{I_{L\,min}}$ refers to the voltage of input signals into the device, and if $V_{I_{L\,min}}$ becomes lower than V_{bb}, minority carriers are injected into the P-well. In the device of Fig. 10(b), the P-wells of the memory cell array and input terminals are separate and included in the bottom N-well, and the structure in Fig. 8 is adopted. If $V_{I_{L\,min}}$ is lower than -2.0 V, Fig. 10(a) indicates FAIL and implies that injected minority carriers destroy cell data. In contrast, as shown in Fig. 10(b), the triple-well device manifests endurance against minority carriers up to $V_{I_{L\,min}} = -3.0$ V.

V. Simulation and Measurement

The results of the simulation and test device measurement are shown in Figs. 11–13. Fig. 11 indicates the simulated and measured V_{bb} levels without load current. In the PMOS system, both simulated and measured V_{bb} are approximately -0.6 V at V_{cc} = 1.5 V. On the other hand, the V_{bb} of HPC are almost equal to $-V_{cc}$ between V_{cc} = 1.5 V and 3.0 V and reach the required negative voltage of -1.44 V at V_{cc} = 1.5 V. Fig. 12 shows the measured pumping current. The intersection of the vertical axis indicates generator current when the V_{bb} is shorted to ground. The lowest V_{bb} that is attainable by each generator is shown by the intersection of the horizontal axis.

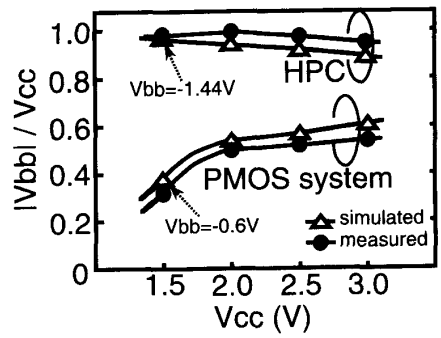


Fig. 11. V_{bb} level without load current.

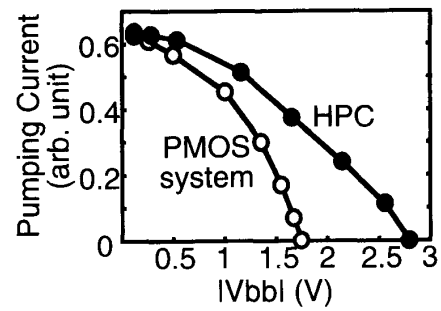


Fig. 12. Measured pumping current at V_{cc} = 3.0 V.

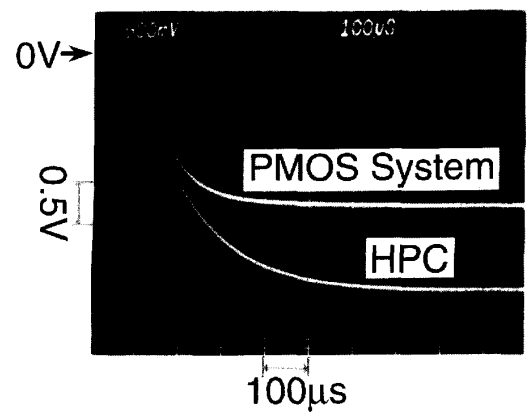


Fig. 13. Transient V_{bb} waveforms after power-on.

HPC has a stronger drivability and lower output-impedance compared with the PMOS system. Fig. 13 shows the transient V_{bb} waveforms of HPC and the PMOS system after power-on. The V_{bb} of HPC sinks faster and lower than that of the PMOS system. All of these results demonstrate that HPC has a higher efficiency than the PMOS system.

VI. Conclusion

In 1.5-V DRAM's, it is necessary for V_{bb} to be lower than -1 V. Conventional V_{bb} generators suffer a loss of voltage

due to the $V_{\rm th}$ of the pumping transistors. An efficient $V_{\rm bb}$ generator with the newly introduced hybrid pumping circuit (HPC) is proposed, which gives a $V_{\rm bb}$ level as low as $-V_{\rm cc}$. A triple-well structure is introduced in HPC, which prevents minority carrier injection. The efficiency and high drivability of HPC has been demonstrated by simulation and test device measurement. HPC shows promise and will be indispensable for 1.5-V DRAM's.

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