Low-Voltage, Low-Power BiCMOS Digital Circuits

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***Abstract*—A new BiCMOS buffer circuit, for low-voltage, low-power environment, will be presented. The circuit is based on the deep submicron technology and utilizes the parasitic bipolar transistors associated with the CMOS structure. The analysis, simulations and SPICE results confirm the functionality of the circuit and its speed and voltage swing superiority, compared with conventional BiCMOS circuits at low supply voltages.**

I. Nomenclature

A_e	Emitter area of BJT
β	Current gain of BJT
β_0	Current gain at low injection levels
C_0	Load capacitance
C_{ox}	Oxide capacitance
ϵ_s	Permittivity of silicon
I_C	Collector current
I_{DS}	Drain current
k	Short channel effects factor
I_K	Knee current of $\beta(I_C)$
L	Channel length
N_C	Collector doping concentration
μ_p	Hole mobility
V_{BE}	Base emitter voltage
V_{DD}	Supply voltage
V_{DS}	Drain to source voltage
V_{GS}	Gate to source voltage
V_o	Output voltage
V_{sat}	Saturation velocity for holes in PMOS
V_s	Saturation velocity for electrons in BJT
W	Channel width
W_C	Collector width

II. Introduction

SPEED degradation of BiCMOS circuits for reduced supply voltage has been reported [1]–[3]. The rapid deterioration in speed as the technology is scaled down from 1.2–0.8 μm to 0.5–0.25 μm [4] suggests the need for an innovative approach to design high speed BiCMOS circuits for future VLSI applications. Although BiCMOS is expected to scale better than CMOS under a proper scaling scheme [13], full swing (or near full swing) buffers are also essential for low supply voltages (< 3 V).

This paper describes a new BiCMOS circuit structure for low-voltage, low-power applications. The idea is based, in general, on utilizing the parasitic bipolar transistors, generic to the CMOS process, together with transmission gates to create additional charging and discharging paths, thereby enhancing the circuit speed. Moreover, the increase in the driving currents will increase the excess minority charge stored in the respective bipolar transistors and sustain their conduction even after the base current drops to zero. It has already been observed that, under low capacitance loading conditions, this phenomenon leads to "high" and "low" logic levels above $V_{DD} - 2V_{BE(on)}$ and less than $V_{BE(on)}$, respectively [14]. It will be shown that the new circuit extends the validity of this phenomenon, to include the high capacitive loads as well, and increases the output voltage to near full swing levels. The proposed addition is applicable to all BiCMOS structures and leads to new circuit configurations for the conventional BiCMOS, BiNMOS, and the complementary BiCMOS (CBiCMOS) [5], [6]. In general, CMOS-compatible bipolar transistors exhibit low performance characteristics. However, the recent interest in incorporating a BJT into a CMOS process has lead to high performance lateral bipolar action in a MOSFET structure [16], [17].

An analytical model to evaluate the delay time of the new circuit configuration will be derived and the results obtained will be discussed. Extensive circuit simulations are performed to verify the functionality of the new circuit, compare its performance with that of the corresponding conventional configuration, and evaluate the analytical model.

The performance of the new circuit is evaluated for scaled supply voltages ranging from 3.3 V to 2.2 V. The improvement in performance as related to the quality of the additional bipolar devices will also be highlighted.

Manuscript received April 7, 1993; revised January 7, 1994.

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IEEE Log Number 9401446.

III. Analysis

Reference is made to the new circuit configurations in Fig. 1, where the BiCMOS pull up section, BiNMOS, and the full BiCMOS buffer are shown in Fig. 1(a), Fig. 1(b), and Fig. 1(c) respectively. The modifications and additions to the conventional pull-up circuit are summarized as follows: (i) The substrate of the pmos MP (which forms the base of the parasitic pnp transistor Q_p) is connected to the source of the transmission gate TP. (ii) The drain of TP is connected to the load capacitance. (iii) The gate of TP is joined with the other gates making the input. For the BiNMOS and BiCMOS circuits in Figs. 1(b), 1(c), the modification amounts to an additional CMOS circuit.

To charge the output capacitance, the input is switched from high to low, turning both MP and TP, hence Q_p ON. The capacitance C_0 will be charged through not only MP (as is the case in conventional configurations) but also the lateral

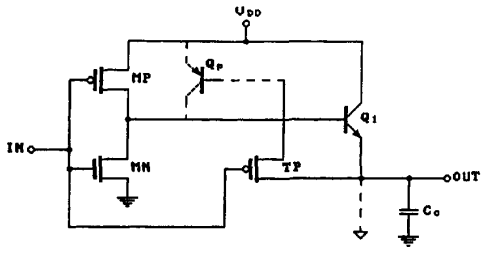


Fig. 1(a). BiCMOS pull up section.

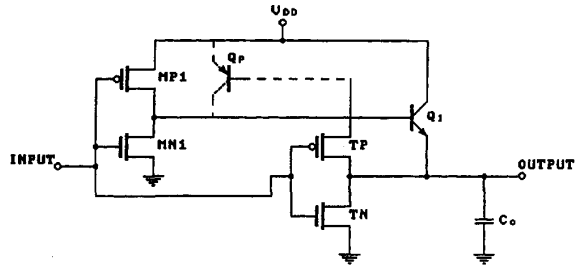


Fig. 1(b). BiNMOS buffer.

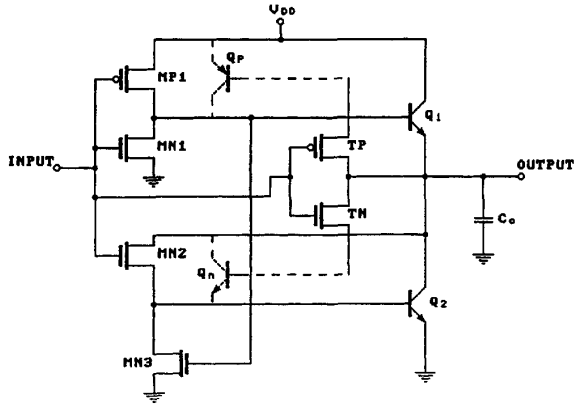


Fig. 1(c). BiCMOS buffer.

transistor Q_p, according to:

$$(I_{DS_1} + \beta_{pnp} I_{DS_2})\beta_{npn} \cong C_o \frac{dV_o}{dt} \tag{1}$$

where the indices 1, 2 refer to the pmos devices MP and TP respectively. While (1) governs the rise time of the output voltage (which constitutes the main circuit delay [7], [8]), other delay time components (charging the total capacitance associated with base of the npn transistor Q_1, as well as the base transit time) can be incorporated later into the model and calculated separately [8]. The conduction of both MP and TP (hence the C_0 charging process) goes through two device operating regions.

A. Region (1), $0 < t < T1$

During this region both pmos devices are saturated, and their drain currents I_{DS_1}, I_{DS_2} are given by the short channel model in [9]:

$$I_{DS_1} = k_1 v_{sat} C_{ox_1} W_1 (V_{GS_1} - V_{T_1}) \tag{1a}$$

$$I_{DS_2} = k_2 v_{sat} C_{ox_2} W_2 (V_{GS_2} - V_{T_2}) \tag{1b}$$

where k is the short channel current factor. (1) can then be solved to give:

$$V_0(t) = A_0 t \tag{2}$$

$$A_0 = \frac{[K_{S1}(V_{GS1} - V_{T1} + K_{S2}\beta_{pnp}]\beta_{npn}}{C_0} \tag{2a}$$

where,

$$K_s = k v_{sat} C_{ox} W. \tag{2b}$$

(2) shows that initially the output voltage rises linearly with time until $t = T_1$ at which TP (hence MP) moves out of saturation where $V_{DS_2} \leq (V_{GS_2} - V_{T_2})$.

That is:

$$V_o(T_1) = (V_{DD} - V_{EB}) - (V_{GS_2} - V_{T_2}). \tag{2c}$$

High level injection in Q_1 occurs if the load capacitance is high and/or the channel width of MP is large. If that is the case, then the base region of the bipolar device widens (Kirk effect) [10] causing β to roll off according to [11]:

$$\beta = \frac{\beta_0}{1 + I_C/I_K} \tag{3}$$

$$I_K = q v_s N_C A_e \left[1 + \left(\frac{2\epsilon_s V_{BC}}{q N_C W_C^2}\right)\right]. \tag{3a}$$

Hence, for $I_C \gg I_K, \beta_{npn} \sim \beta_o I_K / I_C$ and the constant A_o in (2) becomes A_{o_h}, where:

$$A_{o_h} = \sqrt{\frac{A_o I_K}{C_0}}. \tag{4}$$

Both (4) and the circuit simulations results show that the onset of high level injection decreases the rate at which the output voltage is rising with time.

B. Region (2), $t > T_1$

As the output voltage rises with time, the voltages V_{DS_1}, V_{DS_2} across MP and TP decrease, thereby driving the respective devices out of saturation and into the triode region where the current I_{DS} is given by:

$$I_{DS} = K\left[(V_{GS} - V_T)V_{DS} - 0.5V_{DS}^2\right] \tag{5}$$

where:

$$K = \mu_p C_{ox} W/L. \tag{5a}$$

(5), if used with (1), will lead to a differential equation in $V_o(t)$, the solution of which gives:

$$V_o(t) = (V_{DD} - V_{BE}) - \frac{2(V_{GS_2} - V_{T_2})}{1 + \exp[(t - T_1)/\tau]} \tag{6}$$

where:

$$\tau = C_0/\{\beta_{npn}[K_1(V_{GS_1} - V_{T_1}) + K_2\beta_{pnp}(V_{GS_2} - V_{T_2})]\}. \tag{6a}$$

In deriving (6) β_{npn} has been assumed to be constant. However, it can be shown that for high level injection conditions (5) and (3) lead to the following differential equation in $V_o(t)$:

$$\frac{dV_o(t)}{dt} = a_1\sqrt{a_2(V_f - V_o) - a_3(V_f - V_o)^2} \qquad (7)$$

where:

$$V_f = V_{\text{DD}} - V_{\text{BE}}$$
$$a_1 = \sqrt{I_K\beta_0}/C_0$$
$$a_2 = K_1(V_{\text{GS}_1} - V_{T_1}) + K_2\beta_{\text{pnp}}(V_{\text{GS}_2} - V_{T_2})$$
$$a_3 = 0.5(K_1 + K_2\beta_{\text{pnp}}).$$

The solution of (7) is given by:

$$V_o(t) = V_f - A_1[1 + \sin\{A_2 + A_3(t - T_1)\}] \qquad (8)$$

where:

$$A_1 = a_2/2a_3$$
$$A_2 = \arcsin\left[\left(\frac{V_f - V_o(T_1)}{A_1}\right) - 1\right]$$
$$A_3 = -a_1\sqrt{a_3}.$$

IV. Circuit Simulations and Discussion

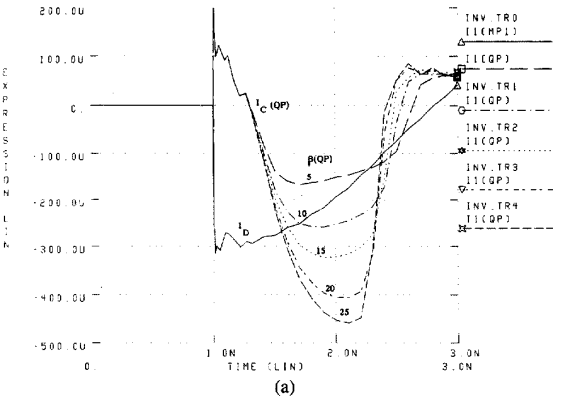
Extensive HSPICE circuit simulations are performed in this section to evaluate the performance of the new circuit as compared to the conventional BiCMOS buffer. More specifically, emphasis wil be given to: the base current components (their relative magnitudes and waveform patterns), the base voltage of the output bipolar transistor, the circuit delay time, and the output voltage swing. The relation between the circuit performance and the current gain of Q_p in the pull up section (and the BiNMOS configuration) is also considered. The simulations are carried out for supply voltages ranging from 3.3 V to 2.2 V.

Since the new circuit uses more devices, its area is expected to be, in general, larger than the conventional circuit. To make up for this, and unless stated otherwise, the channel widths $W_{(\text{conventional})}$ is assumed to be $1.5 \times W_{(\text{new})}$ in the simulations.

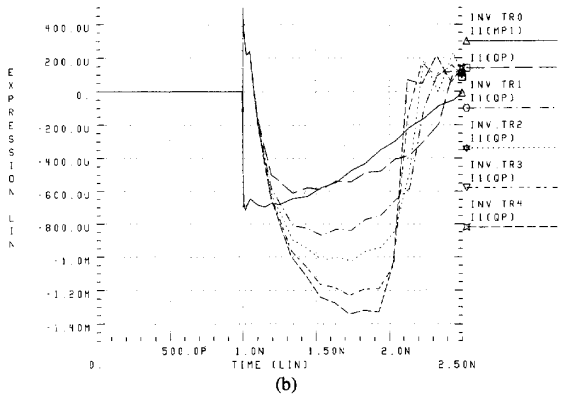
The key device and technology parameters used in the simulations are $V_{\text{to}} = \pm 0.5$, $T_{\text{ox}} = 19$ nm, $N_{\text{sub}} = 6 \times 10^{16}$, $C_{\text{jsw}} = 450 \times 10^{-12}$, $C_j = 500 \times 10^{-16}$, $M_{\text{jsw}} = 0.33$, β_f(vertical npn) = 100, $T_f = 12 \times 10^{-12}$, $I_K = 2 \times 10^{-3}$, $R_c = 100$, $R_e = 10$, $R_b = 400$, $C_{je} = 12$ fF, $C_{jc} = 10$ fF, $C_{js} = 25$ fF. The emitter area is taken to be $4\ \mu \times 0.8\ \mu$. The input to the circuit is a step voltage switched from high to low (or low to high in the pull down section) at $t = 1$ ns.

A. The Base Current Components

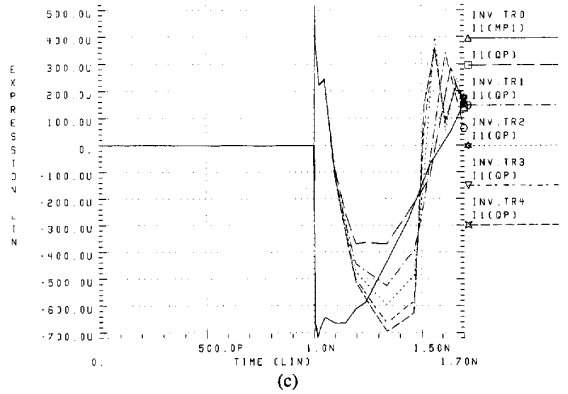
The BiNMOS circuit of Fig. 1(b) has been simulated, using HSPICE, for different values of the supply voltage, load capacitance, and β_{pnp} of Q_p. The base current components, I_{DS} (MP1) and $I_C(Q_p)$, are shown in Fig. 2(a), (b), (c) where the contribution of Q_p to the charging process is clear



(a)



(b)



(c)

Fig. 2. Base current components of Q_1 ($I_C(Q_p)$ are shown for different values of β_{pnp}). (a) $C_0 = 5$ pF, $V_{\text{DD}} = 2.2$ V (b) $C_0 = 5$ pF, $V_{\text{DD}} = 3.3$ V, (c) $C_0 = 1$ pF, $V_{DD} = 3.3$ V.

for all the values of V_{DD}, C_0, and β_{pnp}. Moreover, and as depicted in the same figure, Q_p contributes higher currents for higher supply voltages, higher load capacitances, and higher β_{pnp}. Even if the value of β_{pnp} drops to 5, the ratio $I_C(Q_p)/I_{\text{DS}}$(MP1) is ≥ 0.5. It is worth noting here that, unlike the pattern of $I_{\text{DS}}(t)$, Q_p pumps charges almost uniformly during the charging period thereby contributing significantly to the minority charge stored in Q_1, which in turn leads to higher output voltage swings (as will be shown later).

B. The Base Voltage and the Output Swing

The base voltage waveforms and the associated output voltage rise responses are derived from the same simulations of the circuit of Fig. 1(b). The results, compared to those obtained using the conventional BiNMOS circuit, are shown in Figs. 3(a), 3(b), and 3(c). While comparing Fig. 3(a) and 3(b) shows the effect of the load capacitance, the comparison between Figs. 3(a) and 3(c) gives the effect of scaling the supply voltage on V_B and V_o. The following observations are evident from Fig. (3): (i) The base voltage peaks before settling down to its final value. (ii) V_B shows higher peaks for higher capacitances and higher supply voltages. (iii) The new circuit generates higher base voltage peaks as well as higher output voltage swings, especially at higher supply voltages (V_{DD} = 3.3 V).

It is widely known that under typical loading conditions, the voltage swing of the conventional BiCMOS driver suffers from a voltage loss of 2 $V_{BE(on)}$ [14]. However, it has also been observed that under low capacitance loading conditions, the "high" and "low" logic levels are above $V_{DD} - V_{BE(on)}$ and less than $V_{BE(on)}$ respectively. The results in Fig. 3 confirm this phenomenon and show that the new proposed circuit extends its validity to give a near full voltage swing even under high capacitance loading conditions. This is attributed to the fact that by confining a high excess minority charge in the base of the output bipolar transistors, the transistors can be kept conducting for a long enough time to saturate them. To illustrate this point further, Figs. 4(a) and (b) shows the relation between the obtained voltage swing and β_{pnp} of Q_p for two values of the supply voltage, 3.3 V and 2.2 V, and for different load capacitances. As β_{pnp} increases from 5 to 15 $\sim$ 20, the excess minority charge stored in Q_1 increases as well, thereby enhancing the voltage swing. Higher values of β_{pnp} render insignificant change in that swing. It is also clear from the same figure that the voltage swing improves in general for higher load capacitances and supply voltages. For V_{DD} = 3.3 V and 2.2 V, voltage swings of 3.1 $\sim$ 3.15 V and 1.8 $\sim$ 1.85 V are shown to be attainable. If, however, it is absolutely required to add an additional 100 $\sim$ 200 mV to the voltage swing, then the same technique proposed in this paper can still be implemented in the full swing configuration of [14], [15] to improve the circuit speed. It is worth mentioning here that the near full swing has been obtained by adding a few devices to the conventional circuit, far less than that used by Embabi [14] to achieve full swing operation. Figs. 5(a), (b) and (c) show how the voltage swing varies with the supply voltage for different load capacitances.

C. The Circuit Delay Time

The delay time of the new circuit of Fig. 1(b), compared to its conventional version, is shown in Fig. 6 for C_0 = 1 pF, 3 pF, and 5 pF respectively. The results show that the new circuit is faster than its conventional version and that the speed improvement factor increases for higher load capacitances and supply voltages. This can be explained as follows: when the input switches from "High" to "Low," a component of the

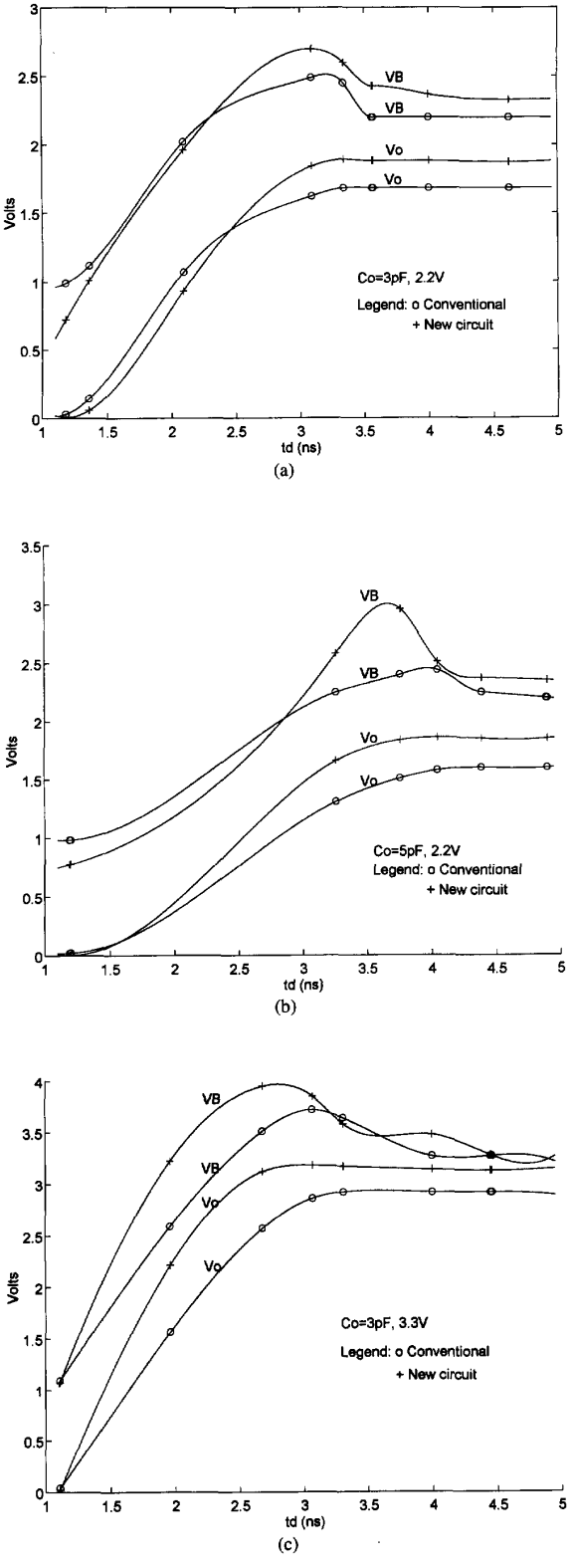


Fig. 3. Base voltage of Q_1 and output rise response for conventional and new circuit. (a) C_0 = 3pF, V_{DD} = 2.2 V, (b) C_0 = 5 pF, V_{DD} = 2.2 V, (c) C_0 = 3 pF, V_{DD} = 3.3 V β_{pnp} = 15.

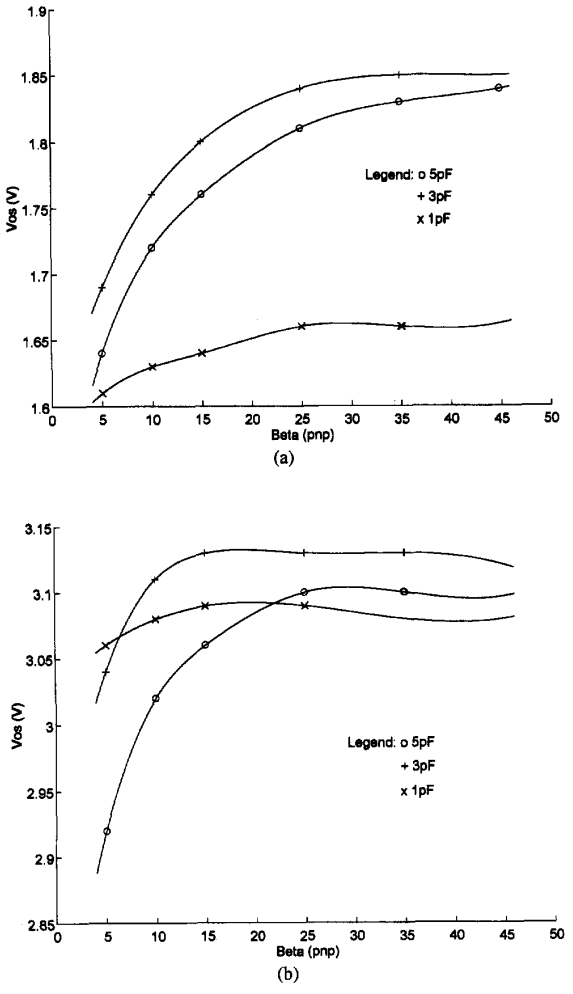
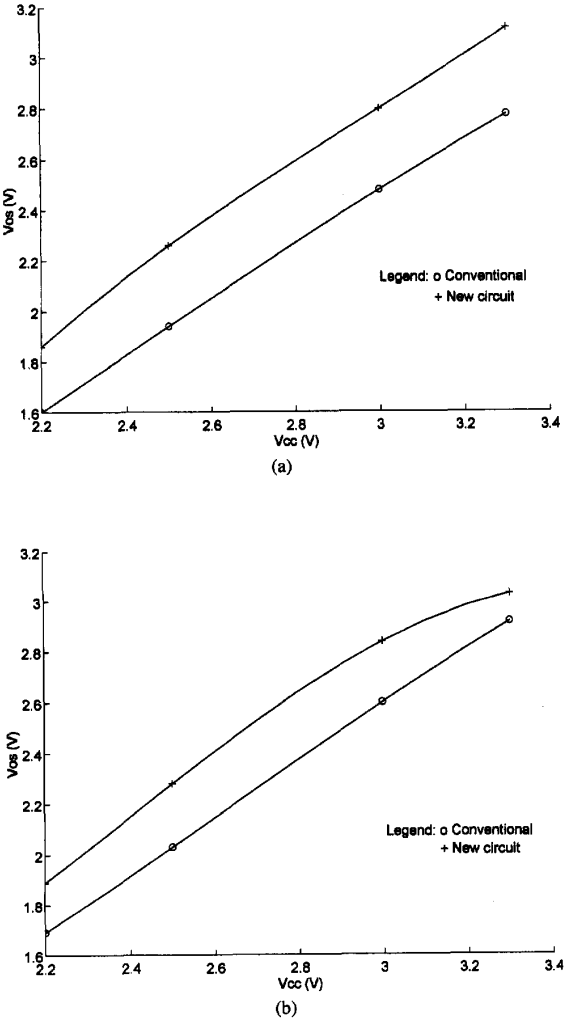


Fig. 4. The relation between the output voltage swing and β_{pnp} of Q_p. (a) $V_{DD} = 2.2$ V, (b) $V_{DD} = 3.3$ V.

current I_D(MP) flows into the collector of Q_p, to discharge whatever is left of its base charge from the previous cycle, giving rise to the negative collector current spikes in Fig. 2. This process will continue for a short time beyond which Q_p starts to contribute positively to the circuit performance. It can be shown, however, that during the charging of C_0, lower load capacitances and/or lower supply voltages drive Q_p deeper in the saturation mode thereby causing the area under $I_C(Q_p)$, from the time of switching to the time at which $I_C(Q_p)$ turns from negative to positive, to increase as well. Referring to Fig. 2, for $V_{DD} = 2.2$ V and $C_0 = 5$ pF, $I_C(Q_p)$ is negative for a duration of 300 ps. The corresponding period for 3.3 V, 5 pF and 3.3 V, 1 pF is 100 ps.

D. The Case of a Buffer Chain (the Cascading Effect)

Circuit simulations have been carried out to study the cascading effect on the circuit performance. The comparison between the new and conventional circuit, shown in Fig. 10, confirm that the new circuit offers improved voltage swings,



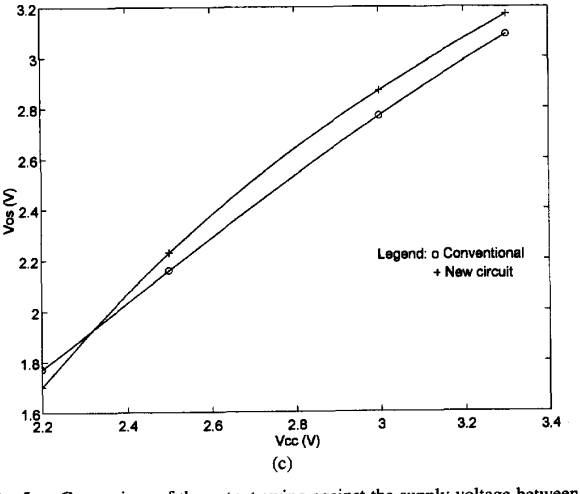


Fig. 5. Comparison of the output swing against the supply voltage between the new and conventional circuits. (a) $C_0 = 5$ pF, (b) $C_0 = 3$ pF, (c) $C_0 = 1$ pF. $\beta_{pnp} = 15$.

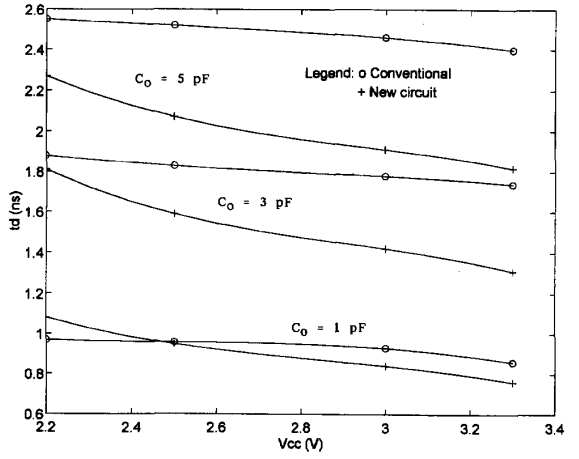


Fig. 6. The delay time of the new circuit of Fig. 1(b), compared to its conventional version for $C_0 = 5$ pF, 3 pF, and 1 pF. $\beta_{pnp} = 15$.

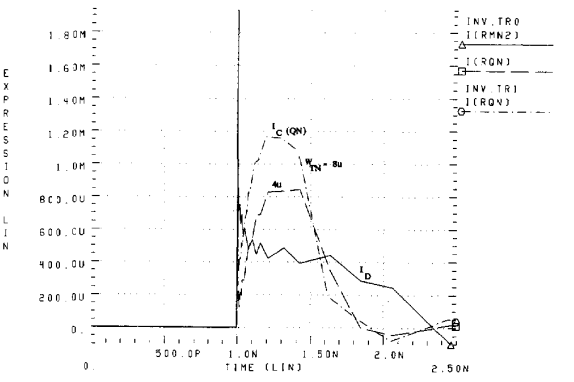


Fig. 7. The base current components of Q_2. (I_C of Q_n is shown for two values of W_{TN}). $\beta(Q_n) = 25$.

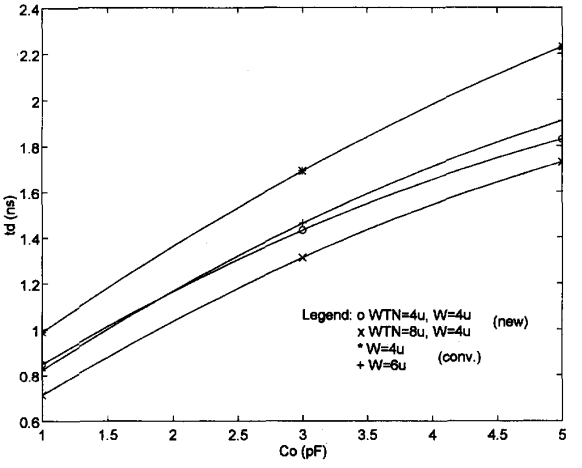


Fig. 8. The delay time of the pull down section of Fig. 1(c) for the new and conventional version. $\beta(Q_n) = 25$.

the amount of which increases for higher load capacitances. The simulation results also show that while the new circuit sustains its functionality for lower supply voltages without sacrificing its speed advantage (except for a single stage operation where $C_o = 1$ pF and V_{DD} is less or equal to 2.2 V), the conventional circuit cannot drive additional stages for supply voltages less or equal to 2.5 V (even if the load capacitance is low).

E. Performance of the New Improved Pull Down Section

The circuit simulations have confirmed that the BiCMOS pull down section of Fig. 1(c) is, in general, faster than that of the BiNMOS circuit of Fig. 1(b). Moreover, the presence of the bipolar transistor Q_n together with the MOSFET TN have improved the circuit speed. The channel width W_{TN} (of TN) has been found to be of particular importance in triggering Q_n to conduct. This is because as W_{TN} increases the base current of Q_n increases which, in turn, increases the current injected into the base of Q_2 leading to faster discharging of C_o. Fig. 7 shows the current components making the base current of Q_2 and the relative contribution made by I_{DS} of MN_2 and I_C of Q_n. The role played by channel width of TN and the delay time comparison between the new and conventional circuits are shown in Fig. 8. It is clear that the new circuit has a speed advantage especially for larger values of W_{TN} and higher load capacitances. Two cases have been considered in Fig. 8: (i) all the MOSFET devices in the two circuits have the same channel width, $W = 4\ \mu$. In this case, A_{new} is slightly higher than $A_{conventional}$. (ii) $W_{(new)} = 4\ \mu$ while $W_{(conventional)} = 6\ \mu$, to make up for the additional devices in the new circuit.

F. Analytical and Simulation Results

The analytical model presented in Section II has been used to calculate the rise time of the pull up section of Fig. 1(b). The results are compared to the SPICE simulations for $V_{DD} = 2.2$ V and different load capacitances. The comparison, in Fig. 9, shows a good agreement especially at higher load capacitances. This is attributed to the fact that the intrinsic delay of the circuit (not included in the analytical model) becomes relatively small at high load capacitances.

G. The Power Dissipation

Fig. 11 shows the power dissipation in the pull up section of the new and conventional circuit for $C_o = 3$ pF, $V_{DD} = 3.3$ V, and $f = 100$ MHz. The comparison shows a comparable average power dissipation in the two circuits and highlights the fact that the improved performance rendered by the new circuit has been achieved at no extra power.

V. Conclusion

A new low-voltage, low-power BiCMOS buffer circuit has been described, analyzed, and simulated. The circuit is based on utilizing the presence of the pnp and npn transistors in the CMOS structure to speed up the conventional circuit and improve its capacitance driving capability at low voltages. Both the analytical model and the circuit simulations confirm the functionality of the circuit and show its speed advantage

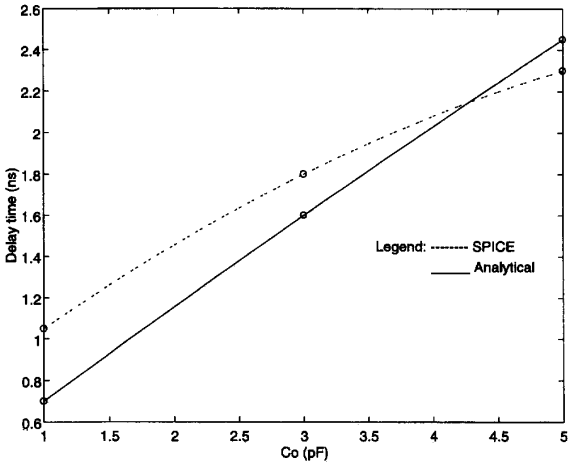


Fig. 9. Comparison between the rise time (analytical) and the delay time (SPICE) of the new circuit for $V_{DD} = 2.2$ V, $\beta(Q_p) = 15$, $\beta(Q_n) = 25$.

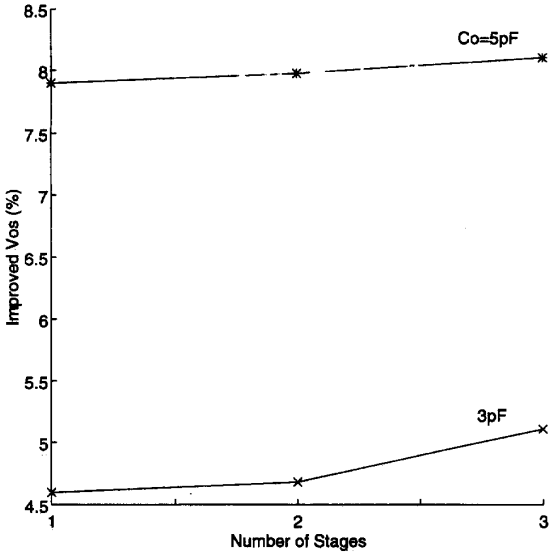


Fig. 10. Improved output voltage swing (in comparison with the conventional circuit) versus the number of stages for $V_{DD} = 3.3$ V.

over conventional BiCMOS circuits. With the addition of just a few devices to the conventional circuit, the new circuit has shown near full swing performance especially for relatively higher supply voltages (3.3 V) and load capacitances. Since the lateral transistors, employed in the new BiCMOS configuration, exhibit higher current gains for lower base (channel) width, the performance of the new circuit is expected to improve as the technology is scaled to deep submicron dimensions.

ACKNOWLEDGMENT

The author wishes to thank B. K. Tay and D. Pu for their technical support. Special thanks should be also given to the unknown reviewers of this paper for their constructive comments which lead to furthering the scope of the work and enhancing the clarity of the manuscript.

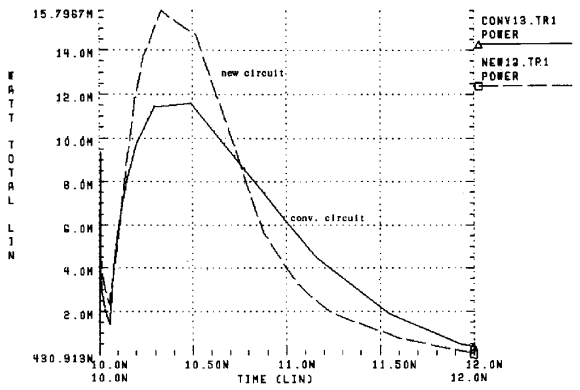


Fig. 11. Power dissipation in the new and conventional circuits (pull up), for $C_0 = 3$ pF, $V_{DD} = 3.3$ V, and $f = 100$ MHz.

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