Highly Testable Design of BiCMOS Logic Circuits

Mohamed Y. Osman, *Member, IEEE*, and Mohamed I. Elmasry, *Fellow, IEEE*

***Abstract*—Most of the work reported in the literature to date on the testability of BiCMOS circuits has concentrated on fault characterization and the need for a suitable testing method that can address the peculiarities of BiCMOS circuits. The problem of adequately testing large BiCMOS logic networks remains open and complex. In this paper, we introduce a new design for testability technique for BiCMOS logic gates that results in highly testable BiCMOS logic circuits. The proposed design incorporates two features: a test charge/discharge path and built-in current sensing (BICS). The test charge/discharge path is activated only during testing and facilitates the testing of stuck-open faults using single test vectors. BICS facilitates testing of faults that cause excessive IDDQ. HSPICE simulation results show that the proposed design can detect stuck-open faults at a test speed of 10 MHz. Faults causing excessive IDDQ are detected by BICS with a detection time of 1 ns and a settling time of 2 ns. Impact of the proposed design on normal operation is minimal. The increase in propagation delay in normal operation is less than 3%. This compares very favorably with CMOS BICS reported in the literature [22], [23] where the propagation delay increase was 20%, 14.4% respectively. The increase in the area is less than 15%.**

***Index Terms*— Testing of BiCMOS logic circuits, design for testability, built-in current sensing.**

I. Introduction

BiCMOS technology combines the advantages of speed and high-drive capabilities of bipolar technology as well as the low-power and high-density of CMOS technology. The main disadvantages of BiCMOS technology, however, are its greater process complexity and its complex failure modes [1]–[7].

The area of testing bipolar and CMOS logic circuits has received considerable attention in the past several years. Numerous testing algorithms, fault simulation methods, and automatic test pattern generation (ATPG) software for generating test sets for bipolar and/or CMOS logic circuits have been developed assuming suitable fault models. For example, see [15]–[20] for test algorithms and ATPG systems based on the single stuck-at fault model, [9], [10] for stuck open faults, and [21] for delay faults. Most of these algorithms and ATPG systems usually work with a gate level description of the circuit rather than a switch level description. In addition, several design for testability (DFT) techniques [8] have been developed to reduce the complexity and cost of testing.

Manuscript received June 21, 1993; received February 25, 1994. This work was supported by KFUPM.

M. Y. Osman was with VLSI Research Group, Dept. of Electrical and Computer Engineering, University of Waterloo, Waterloo, Ontario N2L 3G1, where this work was done. He is now with Computer Engineering Dept., King Fahd University of Petroleum and Minerals, Dhahran 31261, Saudi Arabia.

M. I. Elmasry is with VLSI Research Group, Dept. of Electrical and Computer Engineering, University of Waterloo, Waterloo, Ontario N2L 3G1.

IEEE Log Number 9402127.

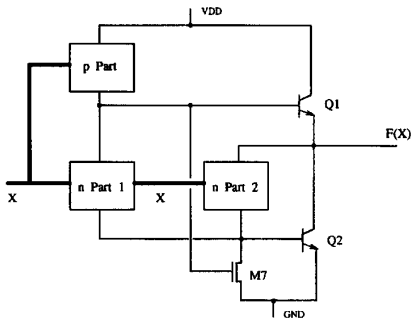

Fig. 1. General structure of a complex BiCMOS logic gate.

In contrast, most of the work reported in the literature to date on the testability of BiCMOS circuits has concentrated on fault characterization and the need for a suitable testing method that can address the peculiarities of BiCMOS circuits. The problem of adequately testing large BiCMOS logic networks remains open and complex.

In this paper, we propose a new design for testability technique for BiCMOS logic gates that results in highly testable BiCMOS logic circuits. The complexity of testing BiCMOS logic circuits implemented using the proposed design method will be comparable to that of testing CMOS logic circuits.

The rest of this paper is organized as follows. First, we review the general structure of BiCMOS logic gates, and their failure modes. Next, Section 2 introduces the proposed highly testable design of BiCMOS logic circuits. Performance assessment and simulation results of the proposed design are provided in Section 3. Conclusions are provided in Section 4.

A. Structure of BiCMOS Logic Gates

The general structure of a BiCMOS logic gate [1] is shown in Fig. 1. It consists of a CMOS logic stage and a bipolar output stage. The CMOS stage performs the logic function and provides proper bias to the output stage which consists of two bipolar transistors: a pull-up (Q1), and a pull-down (Q2) transistor. For normal (fault-free) operation, the CMOS stage ensures that Q1 and Q2 do not both turn on simultaneously.

BiCMOS logic gates can be either primitive gates, e.g., *NAND, NOR, INVERTER*, or complex gates, e.g., *AND-OR-INVERT gate* (*AOI*), *OR-AND-INVERTED gate* (*OAI*) which implement complex logic functions.

B. Failure Modes in BiCMOS Logic Circuits

Physical defects (e.g., *shorts* and *opens*) in BiCMOS logic gates manifest themselves as one or more of the following

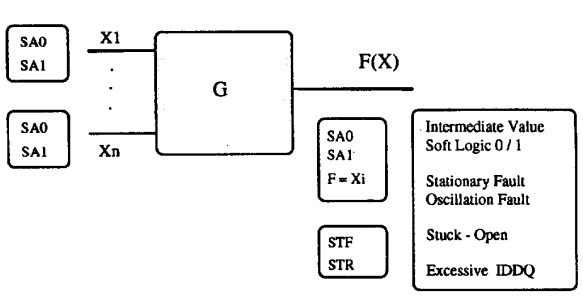

Fig. 2. Effects of shorts and opens on a BiCMOS logic Gate.

categories of logical and/or performance degradation faults [3]–[6], (see Fig. 2):

1. Output is stuck-at 1 (SA1), or is stuck-at 0 (SA0).
2. Input is stuck-at 1 (SA1), or is stuck-at 0 (SA0).
3. Output is stuck-open (*S-Open*), (i.e., the output is floating and presents a high impedance).
4. Output follows one of the inputs.
5. Output has a soft logic 1 or a soft logic 0.
6. Output is logically indeterminate.
7. Abnormal increase in quiescent power supply current (IDDQ).
8. Output is slow to rise (STR) or is slow to fall (STF).

In addition, it has been recently reported [7] that shorts can cause the following non-conventional faults in BiCMOS logic circuits:

1. *Stationary* fault, where during a transition, the output of the circuit initially switches correctly, but settles to an incorrect value.
2. *Oscillation* fault, where the output oscillates between the correct and incorrect value.

II. Testable Design of BiCMOS Logic Circuits

To facilitate testing of BiCMOS logic circuits we propose augmenting the general structure of Fig. 1 by adding:

- A charge/discharge test path for stuck-open faults which is activated only during testing.
- A built-in current sensor (BICS) to detect excessive IDDQ current and generate an error signal.

The augmented design is shown in Fig. 3, and is further detailed in the following subsections.

A. Testability of Stuck-Open Faults

Let Xi be an input to an n-input BiCMOS logic gate that realizes the function $F(X)$ where $X = \{X1, X2, \cdots Xn\}$ and let $F(X)$ be dependent on all its variables. Let Xi be connected to the gate terminal of the p-MOS pi in the p-part and the n-MOS(s) $ni(1), ni(2)$ in n-part 1, 2 respectively. That is, Xi controls $pi, ni(1), ni(2)$. If Xi is high (low), i.e., set to logic 1 (0), then pi is OFF (ON) and $ni(1), ni(2)$ are ON (OFF).

Since $F(X)$ depends on Xi, then there exists at least one input pattern $t = X1X2\cdots Xn$ such that t sensitizes F to Xi, i.e., makes F toggles as Xi toggles. Let $t(i,0)$, $t(i,1)$ designate the input patterns obtained from t by setting Xi to 0, 1 respectively,

$$t(i,0) = X1X2\cdots Xi-1\ 0\ Xi+1\cdots Xn$$
$$t(i,1) = X1X2\cdots Xi-1\ 1\ Xi+1\cdots Xn.$$

Since t sensitizes F to Xi then $F(t(i,0)) = \overline{F(t(i,1))}$, e.g., $F(t(i,0)) = 1$ and $F(t(i,1)) = 0$. The patterns $t(i,0), t(i,1)$ must satisfy the following two conditions.

Condition 1: $t(i,0)$ *sensitizes pi*, (the p-MOS controlled by Xi), i.e., $t(i,0)$ turns ON conduction path(s) between VDD and the base of Q1 such that all such path(s) contain pi and no other conduction path(s) in the p-part are turned ON. Furthermore, all conduction path(s) in n-part 2 between the output and GND are turned OFF and all conduction path(s) in n-part 1 between the base of Q1 and GND are OFF. (This ensures that when $t(i,0)$ is applied, Q1 is turned ON, Q2 is turned OFF, and the output is pulled up only if pi is conducting).

Condition 2: $t(i,1)$ *sensitizes ni*(2), (the n-MOS in n-part 2 that is controlled by Xi), i.e., $t(i,1)$ turns ON conduction path(s) between the output and the base of Q2 such that all such path(s) contain $ni(2)$ and no other conduction path(s) in the n-part 2 are turned ON. Furthermore, all conduction path(s) in the p-part between VDD and the base of Q1 are turned OFF. (This ensures that when $t(i,1)$ is applied, Q1 is turned OFF, Q2 is turned ON, and the output is pulled down only if $ni(2)$ is conducting).

The above conditions ensure that, when the input pattern t is applied, the gate output is sensitized to Xi and will toggle if Xi toggles. It should be clear that $t(i,0)$ detects the fault Xi SA1 and $t(i,1)$ detects the fault Xi SA0.

Now consider a stuck-open fault in the pi sensitized by $t(i,0)$. If $t(i,0)$ is applied, then by condition (1), all conduction path(s) through n-part 1, 2 are OFF, and all conduction path(s) through the p-part are also OFF since the only one(s) that could have been ON in the good circuit contain pi which is now OFF due to the fault. Therefore, both Q1 and Q2 are OFF and the output floats and assumes a value that depends on its value prior to applying $t(i,0)$. Hence, $t(i,0)$ can detect the fault pi stuck-open ONLY if it is preceded by the proper initialization pattern to initialize the output to the opposite value, i.e., 0 in this case. As a result, to detect a stuck-open fault, two test patterns are required: the first to initialize the output and the second to drive the output to high impedance in the presence of the fault.

Since $t(i,0)$ also detects the fault Xi SA1, we will use the notation that the fault Xi SA1 is *potentially equivalent* to the fault pi stuck-open to mean that a test for Xi SA1 will also be a test for pi stuck-open provided that the proper initialization pattern is applied first. (This is similar to [9] for CMOS circuits). Likewise, Xi SA0 is potentially equivalent to $ni(2)$ stuck-open, F SA0 is potentially equivalent to Q2 stuck-open, and F SA1 is potentially equivalent to Q1 stuck-open.

Two-pattern tests have been widely used for testing stuck-open faults in CMOS logic circuits [9], [10]. However, they can be invalidated due to circuit delays, hazards, and timing

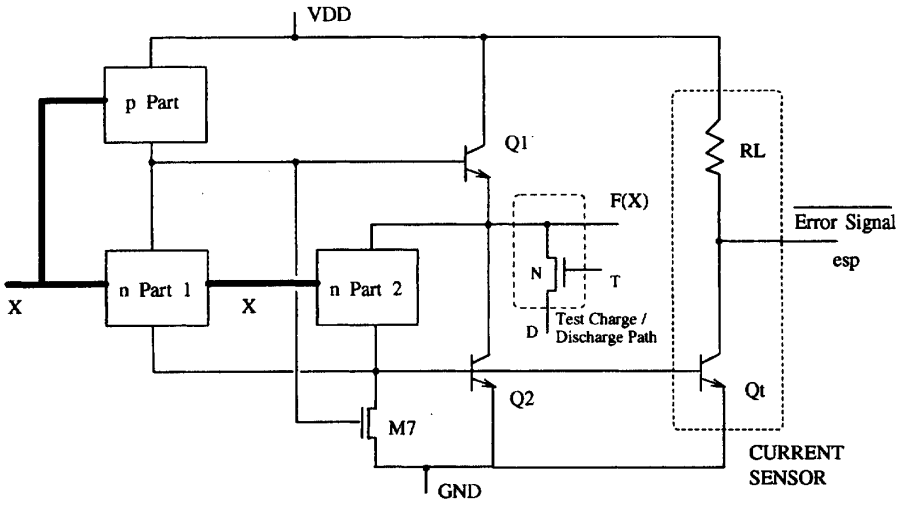

Fig. 3. Structure of a highly testable complex BiCMOS logic gate.

skews [11]–[14]. To facilitate testing of stuck-open faults in CMOS logic gates, modifications to their design have been proposed in the literature [11]–[14]. In particular, a method is developed in [14] to remove the initialization requirement and allow stuck-open faults in CMOS logic circuits to be detected by single test patterns. The basic idea is to provide, during testing, an additional path for charging or discharging the output of the gate whenever it is floating. Such an additional path is only activated during testing and does not affect normal circuit operation. This can be easily adapted for BiCMOS logic gates by augmenting each gate by an additional n-MOS transistor, N, as shown in Fig. 3.

In normal operation, T is set to logic 0 so that the added transistor N is OFF and does not affect the normal operation of the circuit. Furthermore, N is designed such that its ON *resistance*, (R_{on}), is much higher than that of n-part 2, Q1, Q2. In addition, its ON *resistance* must also be much smaller than the OFF *resistance*, (R_{off}), of n-part 2, Q1, Q2. Specifically, the following relations must be satisfied:

$$R_{\text{on}} \text{ of } N >> R_{\text{on}} \text{ of } n \text{ part } 2, R_{\text{on}} \text{ of Q1}, R_{\text{on}} \text{ of Q2}$$
$$R_{\text{on}} \text{ of } N << R_{\text{off}} \text{ of } n \text{ part } 2, R_{\text{off}} \text{ of Q1}, R_{\text{off}} \text{ of Q2}.$$

The augmented BiCMOS gate of Fig. 3 removes the need for the initialization vector and allow testing of stuck-open faults in BiCMOS logic circuits by using single test patterns as explained below.

Consider the fault pi stuck-open, where pi is any p-MOS in the p-part. Let pi be controlled by Xi, and let $t(i,0)$ be an input pattern that *sensitizes pi* in the fault-free circuit. The single test vector $t^* = (t(i,0), T = 1, D = 0)$ will detect the fault pi stuck-open as shown below.

Since $T = 1$, N conducts and provides a pull down path for the output. In the fault-free circuit, $t(i,0)$ turns Q1 ON and Q2 OFF (due to condition(1)). The output is therefore being pulled up through Q1 and pulled down through N. But since the ON resistance of N is much higher than that of Q1 (by design), then the output is pulled up and attains logic 1.

In the faulty circuit, $t(i,0)$ turns both Q1 and Q2 OFF (due to condition (1) and the fault). However, the output is pulled down through N and attains logic 0. Hence, t^* produces an output of 1 in the fault-free circuit and an output of 0 if pi is stuck-open. Therefore, t^* is a test for the fault pi stuck-open.

Similarly, a stuck-open in $ni(2)$ (p-MOS in n-part 2) can be detected by the single test pattern $t^* = (t(i,1), T = 1, D = 1)$, where $t(i,1)$ sensitizes $ni(2)$.

Opens and shorts that can cause the output of a BiCMOS logic gate to be stuck-open includes [3]:

- Opens at the source (s), drain (d), or gate (g) terminals of the MOS transistors in the p-part and n-part 2.
- Opens at the base or emitter terminals of Q1 and Q2.
- Gate to source short in M7.

For each open or short that can cause the output of the BiCMOS logic gate to be stuck-open, Table I provides a single test vector that can detect the fault in the augmented gate.

The results of the above discussions are formalized in the following lemma(s).

Lemma 1: Let pi ($ni(2)$) be a p-MOS (n-MOS) in the p-part (n-part 2) of the augmented gate of Figure 2 and let pi ($in(2)$) be controlled by Xi. Let t be a test for the fault Xi SA1 ($SA0$). Then, a single test vector t for the fault pi ($ni(2)$) stuck-open is given by: $t^* = (t, T, D)$ where $T = 1$, $D = 0(1)$ as shown in Table I.*

Lemma 2: Let F be the output of a BiCMOS logic gate. Let t be a test for the fault F SA0 (SA1). Then, in the augmented gate of Figure 3, a single test vector t for the fault Q1(Q2) stuck-open is given by: $T^* = (t, T, D)$ where $T = 1$, $D = 0(1)$ as shown in Table I.*

Lemma 3: Let F be the output of a BiCMOS logic gate. Let t be a test for the fault F SA0. Then, in the augmented gate of Figure 3, a single test vector t for the output stuck-open fault*

TABLE I
TESTING FOR STUCK-OPEN FAULTS

Fault	Apply			Response	
	T	D	Test Vector t	Good	Faulty
Stuck-open in p-part (opens at s, d, or g of a p-MOS)	1	0	element of the ON set of F, and sensitizes the p-MOS in question	1	0
Stuck-open in n-part 2 (opens at s, d, or g of an n-MOS)	1	1	element of the OFF set of F, and sensitizes the n-MOS in question	0	1
Q1 S-Open (open base or emitter)	1	0	element of the ON set of F	1	0
Q2 S-Open (open base or emitter)	1	1	element of the OFF set of F	0	1
Short in M7 (gate to source)	1	0	element of the ON set of F	1	0

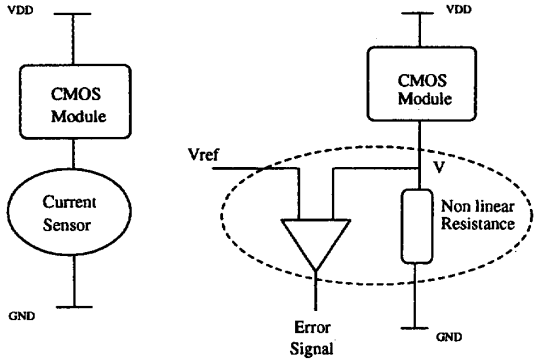

Fig. 4. CMOS built-in current sensing (BICS).

caused by a gate-to-source short in M7 is given by: $t^* = (t, T, D)$ *where* $T = 1$, $D = 0$ *as shown in Table I.*

Lemma 4: In the augmented gate of Fig. 3, a complete stuck-at test set in which every vector is augmented with T, D as defined in Table I, will detect all the following fault categories of Section 1, 2*:* (1), (2), (3), (4).

It should be noted that the size of the added nMOS N for the charge/discharge test path for stuck-open faults must be carefully chosen. As the size of N increases, the test speed improves as it will provide a faster charging/discharging path for the output node in the presence of stuck-open faults. However, a larger size of N will also result in a degradation of V_{out} (*high*), V_{out} (*low*) in test mode. This is because in test mode for stuck-open fault, $T = 1$ and the output of a good gate will be simultaneously pulled up (down) by Q1 (Q2) and pulled (up) by N.

B. Built-in Current Sensing (BICS) for IDDQ Testing

Built-in current sensing (BICS) has been suggested as an effective means for testing faults that cause excessive IDDQ in CMOS circuits [22]–[26]. The general structure of a CMOS BICS is shown in Fig. 4 [26]. However, the inclusion of BICS between a CMOS module and its ground path results in excessive increase in propagation delays (14% to 20%) as reported in [22], [23].

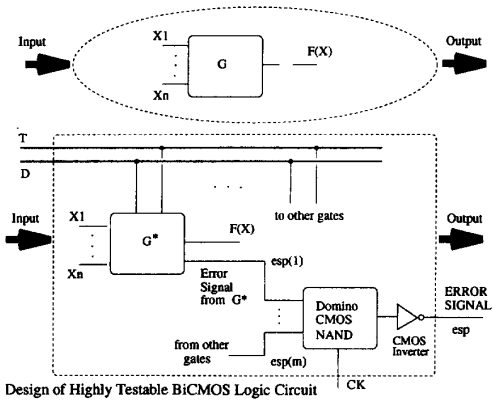

Fig. 5. Highly testable BiCMOS logic circuit design.

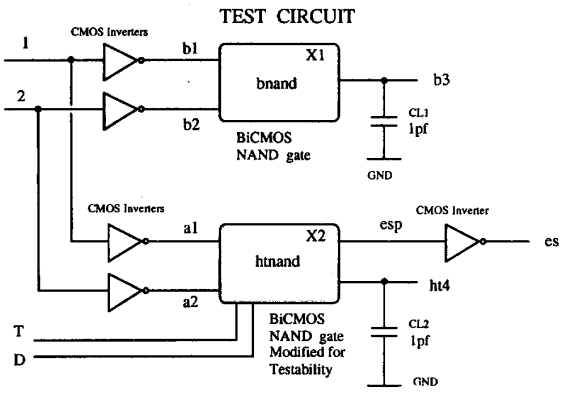

Fig. 6. Test circuit used to assess the performance and testability of the proposed design.

BICS performance can be categorized by the following factors:

1. Impact on normal operation, i.e., amount of added propagation delay.
2. Detection time, i.e., how fast can tests be applied.
3. Sensitivity, i.e., the minimum required IDDQ to trigger the error signal.
4. Area overhead.

We propose the BICS structure shown in Fig. 3 for BiCMOS circuits. Qt is a current mirror whose base and emitter nodes are connected to the base and emitter nodes of the pull-down transistor Q2. In case of a fault that causes an abnormal current to pass between VDD and GND and due to the current mirror effect, Qt will carry a current proportional to that which passes through Q2. If that current is above certain threshold, it will cause sufficient voltage drop across RL and the error signal *esp* will be low (i.e., logic 0) indicating the presence of a fault. On the other hand, for fault-free circuit operation, the steady state current that passes in Q2 (and the proportion of it that passes in Qt) is very small and the error signal *esp* will be high (i.e., logic 1) indicating fault-free operation.

In reference to Fig. 3, it should be noted that the size of Qt (relative to Q2) directly impacts two performance factors of

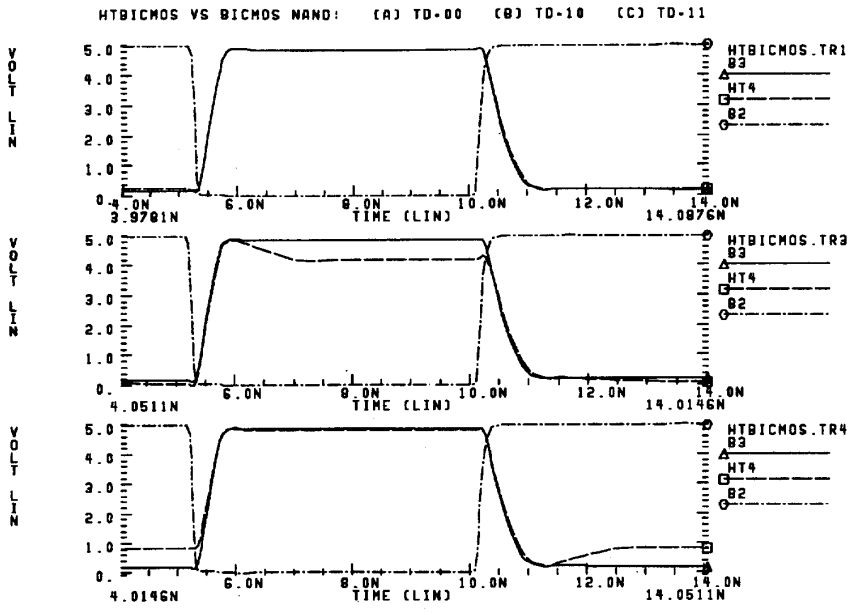

Fig. 7. Highly testable BiCMOS NAND (*htnand*) vs BiCMOS NAND Gate (*bnand*): (a)TD = 00, (b) TD = 01, (c) TD = 11.

BiCMOS BICS. As the size of Qt increases, the sensitivity of BICS increases since the threshold IDDQ required to trigger the error signal decreases. However, a larger size of Qt will result in an increase of the fall time of the gate output in normal operation, i.e., the penalty will be more propagation delay. This is because the proportion of the current that flows in Qt could have been otherwise used (if passed through Q2) to discharge the output node during an output transition from high to low. Likewise, for a given size of Qt, the size of RL directly impacts two performance factors of BICS. As the size of RL increases, the sensitivity increases, however, the settling time of the error signal will also increase. Detailed performance assessment of the proposed highly testable structure of Fig. 3 as obtained by HSPICE simulation is provided in Section 3.

As noted in [26], [27], a complete stuck-at test set plus monitoring IDDQ detects all stuck-on faults in an irredundant CMOS combinational circuit, and is a complete leakage current test set. And since the following fault categories of Section 1.2: (5)–(7) are associated with excessive IDDQ current [3], then we have the following lemma.

Lemma 5: In the augmented gate of Fig. 3, a complete stuck-at test set plus monitoring IDDQ will detect all the following fault categories of Section 1.2: (1), (2), (4)–(7).

Furthermore, a source-to-drain short in the added nMOS transistor N will cause excessive IDDQ current to flow in Q2 and can be detected provided that D is set to logic 1 and F(X) is set to logic 0. *Similarly a gate-to-drain short in N can be detected by monitoring IDDQ as stated in the following lemma.*

Lemma 6: In the augmented gate of Fig. 3, a source-to-drain short in the added transistor N can be detected by the test vector $t^* = (t, T, D)$ *plus monitoring IDDQ, where* t *is an element of the OFF set of* $F, T = 0, D = 1$. *Similarly, a gate-to-drain short in the added transistor N can be detected by the test vector* $t^* = (t, T, D)$ *plus monitoring IDDQ, where* t *is an element of the OFF set of* $F, T = 1, D = 0$.

Now to implement a highly testable BiCMOS logic circuit consisting of m BiCMOS logic gates, each BiCMOS logic gate, G, is replaced with its highly testable version, G*, that is detailed in Fig. 3. The error signals $esp(i), (i = 1, \ldots, m)$ of the m gates can be combined using a NAND gate to provide a single error signal *esp* for the whole circuit. Due to the large number of inputs of such a NAND gate, it is best implemented as a domino logic CMOS NAND gate. The overall structure of a highly testable BiCMOS logic circuit is shown in Fig. 5.

III. Performance Assessment

To assess the performance and testability of the proposed BiCMOS logic gate design, a BiCMOS NAND gate with BICS and test charge/discharge path as shown in Fig. 3 was designed using 0.8 μm technology. All pMOS transistors have (W/L) = (30 μm/0.8 μm), all nMOS transistors in n-part 2 have (W/L) = (18 μm/0.8 μm), and all nMOS transistors in n-part 1 as well as M7 have (W/L) = (2 μm/0.8 μm). The added nMOS N has a (W/L) = (2 μm/0.8 μm). The pull-up and pull-down bipolar transistors Q1, Q2 are of size 4× whereas the current mirror Qt has a size 1×, and RL = 4 kΩ. From a preliminary layout, the estimated area penalty of the added testability features is less than 15%.

Several faults were injected in the gate including an open pMOS, a stuck-on nMOS (drain-to-source short), and a gate-to-source short. The simulated circuit contained a standard unmodified BiCMOS NAND gate (*bnand*) and a highly testable BiCMOS NAND gate (*htand*). CMOS input inverters were used to provide realistic driving inputs, and a load capacitance of 1 pF was connected to the gate output to provide a realistic

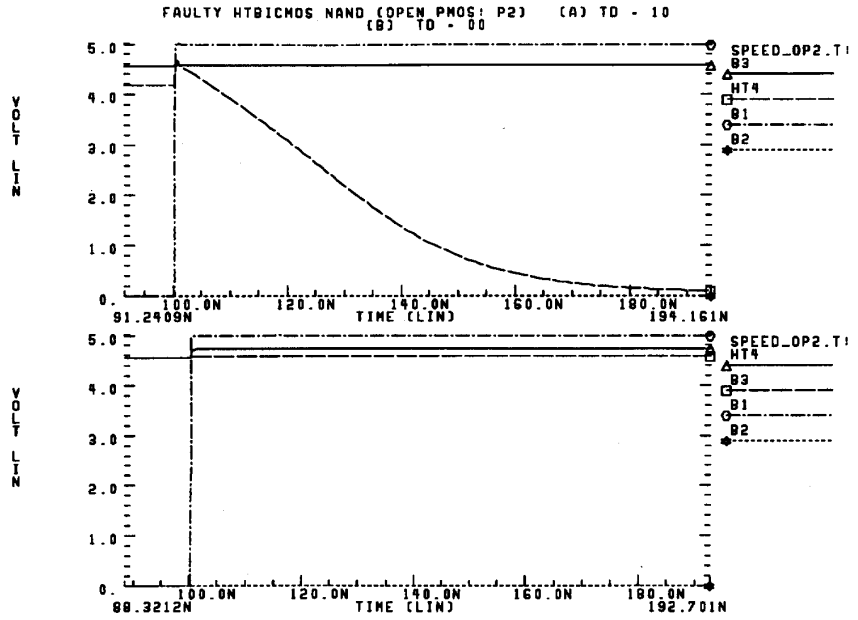

Fig. 8. Faulty *htnand* gate: open pMOS: (a) TD = 10, (b) TD = 00.

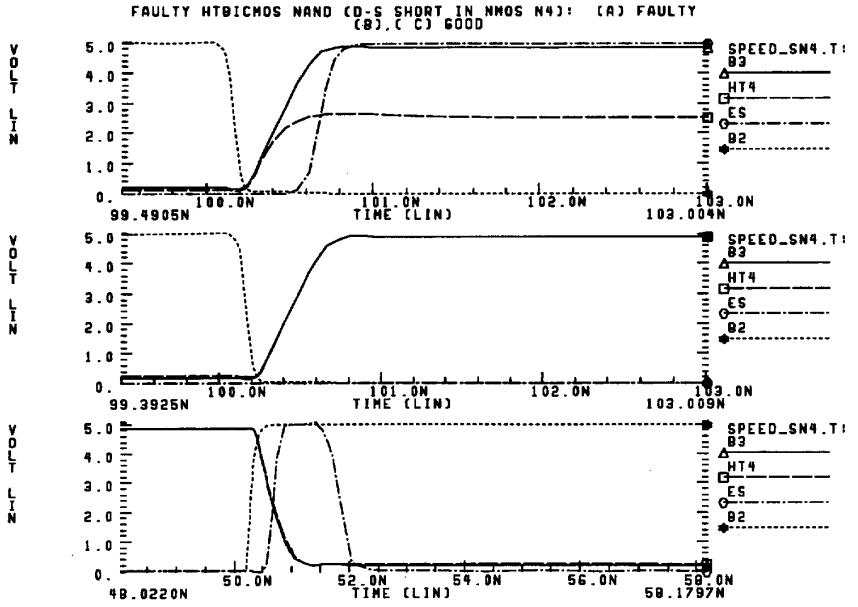

Fig. 9. Faulty *htnand* gate: shorted nMOS: (a) faulty gate, (b) good gate, (c) settling time for *es* (good gate).

load as shown in Fig. 6. HSPICE simulation results are summarized below.

1. For TD = 00, or TD = 01, (i.e., in normal operation), the output waveforms of *htnand* and *bnand* are virtually identical, see Fig. 7(a), with the exception of a slight increase in the propagation delay of *htnand* as follows: increase in rise time = 0%, increase in fall time = 5.2%. Therefore, the average increase in propagation delay is 2.6%, i.e., less than 3%.
2. For TD = 10, or TD = 11, (i.e., in test mode), the output wave forms are shown in Fig. 7(b) and (c), where the degradation in $V_{\text{out}}(high)$, $V_{\text{out}}(low)$ of the good circuit is apparent but is still acceptable.
3. Stuck-open fault(s) are easily detectable with single test vector(s) and $T = 1$ as shown in Fig. 8(a). Detection time is well below 80 ns allowing a test speed of 10 MHz with a comfortable margin. Note that if $T = 0$, i.e., if the test charge/discharge path is deactivated, then

TABLE II
IMPACT OF THE SIZE OF Qt ON BICS SENSITIVITY AND PROPAGATION DELAY AS OBTAINED BY HSPICE SIMULATION (RL=1 kΩ)

Size of Qt (Current Mirror)	1X	2X	4X
Size of Q2 (Pull-down Trans.)	4X	4X	4X
Min. IDDQ* (μA)	900	350	150
Increase in Fall Time	5.2%	11.09%	22.8%

TABLE III
IMPACT OF THE SIZE OF RL ON BICS SENSITIVITY AND SETTLING TIME OF THE ERROR SIGNAL AS OBTAINED BY HSPICE SIMULATION (Qt=1×, Qw=4×)

Size of RL	1 K	2 K	3 K	4 K	5 K
Min. IDDQ* (μA)	900	500	330	175	160
Settling Time (ns)	1	1.5	1.8	2	2.3

this fault is not detectable by a single test vector, as shown in Fig. 8(b), due to charge retention as the output node.

4. Faults that cause excessive IDDQ, (e.g., stuck-on faults, drain-to-source shorts, gate-to-source shorts) are easily detectable by BICS as indicated by $es = 1$. It should be noted that in the presence of such a fault, the output assumes an intermediate value (as shown in Fig. 9(a)) and the fault may not be detected by functional testing, but is easily detectable by BICS. Detection time is within 1 ns as shown in Fig. 9(a). However, when the output of the good gate makes a high-to-low transition, high current passes through Q2 and causes the error signal *es* to be set for a short duration, (see Fig. 9(c)). Therefore, *es* should not be sampled before it settles down. This settling time is about 2 ns.

To assess BICS sensitivity, a gate-to-source short of variable size was injected and the circuit was simulated for different sizes of Qt, RL. Tables II and III summarize the impact of the size of Qt, RL on BICS sensitivity, propagation delay of *htnand*, and the settling time of the error signal. Note that, in Tables II and III, the value listed for IDDQ* is the minimum abnormal current flowing in n-part 2 (rather than in Q2) and that is necessary to trigger the error signal. This is chosen to provide a common base for comparison with CMOS BICS.

Tables II and III clearly demonstrate the contention among the various BICS performance objectives, namely, impact on propagation delay, sensitivity, and settling time. As a design strategy, one can proceed by selecting the size of Qt such that the propagation delay degradation is within the acceptable limits. RL is then selected to meet the sensitivity requirement, and the settling time determines the permissible test speed.

The proposed BICS (with Qt = 1×, Q2 = 4×, RL = 4 kΩ) has the following performance characteristics: detection time is less than 2 ns, and the increase in propagation delay in normal operation is less than 3%. This compares very favorably with the CMOS BICS structures reported in [22], [23] where the propagation delay increase in [22] is 20%, and in [23] is 14.4%.

IV. CONCLUSION

In this paper, we have introduced a new design for testability technique for BiCMOS logic gates that results in highly testable BiCMOS logic circuits. The proposed design incorporates two features: a test charge/discharge path and built-in current sensing (BICS). The test charge/discharge path is activated only during testing and facilitates the testing of stuck-open faults using single test vectors. BICS facilitates testing of faults that cause excessive IDDQ. HSPICE simulation results show that the proposed design can detect stuck-open faults at a test speed of 10 MHz. Faults causing excessive IDDQ are detected by BICS with a detection time of 1 ns and a settling time of 2 ns. The impact of the proposed design on normal operation is minimal. The increase in propagation delay in normal operation is less than 3%. This compares very favorably with CMOS BICS reported in the literature [22, 23] where the propagation delay increase was 20%, 14.4% respectively. The area penalty is less than 15%.

REFERENCES

[1] A. R. Alvarez, Ed., *BiCMOS Technology and Application.* Kluwer Academic, 1989.

[2] S. H. Embabi, A. Bellaouar and M. I. Elmasry, *Digital BiCMOS Integrated Circuit Design.* Kluwer Academic, 1993.

[3] A. E. Salema and M. I. Elmasry, "Fault characterization, testing considerations, and design for testability of BiCMOS logic circuits," *IEEE J. Solid-State Circuits*, vol. 27, no. 6, pp. 944–947, June 1992.

[4] B. E. Stewart, D. Al-Khalili and C. Rozon, "Defect modeling and testability analysis of BiCMOS circuits," *Canadian J. Elect. & Comp. Eng.*, vol. 16, no. 4, pp. 148–153, 1991.

[5] M. E. Levitt, K. Roy and J. A. Abraham, "BiCMOS fault models: is stuck-at adequate?," *Proc. IEEE Int. Conf. on Computer Design*, pp. 294–297, 1990.

[6] K. Roy, M. E. Levitt and J. A. Abraham, "Test considerations for BiCMOS logic families," *Proc. IEEE Custom Integrated Circuit Con.*, pp. 17.2.1–17.2.4, 1991.

[7] S. C. Ma and E. J. McCluskey, "Non-conventional faults in BiCMOS digital circuits," *Proc. IEEE Int. Test Conf.*, pp. 882–891, 1992.

[8] M. Abramocivi, M. A. Breuer and A. D. Friedman, *Digital Systems Testing and Testable Design.* Computer Science, 1990.

[9] H. K. Lee and D. S. Ha, "SOPRANO: an efficient automatic test pattern generator for stuck-open faults in CMOS combinational circuits," *Proc. 27th ACM/IEEE Design Automation Conf.*, pp. 660–666, June 1990.

[10] H. Cox and J. Rajski, "Stuck-open and transition fault testing in CMOS complex gates," *Proc. IEEE Int. Test Conf.*, pp. 688–694, Sept. 1988.

[11] S. M. Reddy and M. K. Reddy, "Testable realizations for FET stuck-open faults in CMOS combinational logic circuits," *IEEE Trans. Comput.*, vol. 35, no. 8, pp. 742–754, Aug. 1986.

[12] D. L. Liu and E. J. McCluskey, "CMOS scan-path IC design for stuck-open fault testability," *IEEE J. Solid-State Circuits*, vol. 22, no. 5, pp. 880–885, Oct. 1987.

[13] R. Rajsuman, A. P. Jayasumana and Y. K. Malaiya, "CMOS open-fault detection in the presence of glitches and timing skews," *IEEE J. Solid-State Circuits*, vol. 24, no. 4, pp. 1055–1061, Aug. 1989.

[14] A. P. Jayasumana, Y. K. Malaya and R. Rajsuman, "Design of CMOS circuits for stuck-open fault testability," *IEEE J. Solid-State Circuits*, vol. 26, no. 1, pp. 58–61, Jan. 1991.

[15] J. P. Roth, W. G. Bouricius and P. R. Scheneider, "Programmed algorithm to compute tests to detect and distinguish between failures in logic circuits," *IEEE Trans. Comput.*, vol. 16, no. 10, pp. 567–580, Oct. 1967.

[16] P. Goel, "An implicit enumeration algorithm to generate tests for combinational logic circuits," *IEEE Trans. Comput.*, vol. 30, no. 3, pp. 215–222, March 1983.

[17] H. Fujiwara and T. K. Shimono, "On the acceleration of test generation algorithms," *IEEE Trans. Comput.*, vol. 32, no. 12, pp. 1137–1144, Dec. 1983.

[18] T. Kirkland and M. R. Mercer, "A topological search algorithm for ATPG," *Proc. 24th ACM/IEEE Design Automation Conf.*, pp. 502–508, 1987.

[19] M. H. Schulz, E. Trischler and T. M. Sarfert, "SOCRATES: a highly efficient automatic test pattern generation system," *IEEE Trans. Computer-Aided Design*, vol. 7, no. 1, pp. 126–137, Jan. 1988.

[20] T. Larrabee, "Test pattern generation using boolean satisfiability," *IEEE Trans. Computer-Aided Design*, vol. 11, no. 1, pp. 4–15, Jan. 1992.

[21] K. Fuchs, F. Fink and M. H. Schulz, "DYNAMITE: an efficient automatic test pattern generation system for path delay faults," *IEEE Trans. Computer-Aided Design*, vol. 10, no. 10, pp. 1323–1335, Oct. 1991.
[22] P. Nigh and W. Maly, "A self-testing ALU using built-in current sensing," *IEEE Custom Integrated Circuits Conf.*, pp. 22.1.1–22.1.4, 1989.
[23] T. Shen, J. Daly and J. Lo, "A 2-ns detecting time, 2 μm CMOS built-in current sensing circuit," *IEEE J. Solid-State Circuits*, vol. 28, no. 1, pp. 72–77, Jan. 1993.
[24] P. Maxwell and R. Aitken, "The effectiveness of IDDQ, functional and scan tests: how many fault coverage we need?," *IEEE Int. Test Conf.*, pp. 168–177, Oct. 1992.
[25] R. Perry, "IDDQ testing in CMOS digital ASIC's—putting it all together," *IEEE Int. Test Conf.*, pp. 151–157, Oct. 1992.
[26] Q. Tong, "Built-in current self-testing scheme (BICST) for CMOS logic circuits," *IEEE VLSI Test Symp.*, April 1992, pp. 304–308.
[27] Y. K. Malaiya and S. Y. H. Su, "A new fault model and testing technique for CMOS devices," *IEEE Int. Test Conf.*, pp. 25–34, 1982.

Mohamed Y. Osman (S'70-M'73-M'89) received the B.Sc. degree in Electrical Engineering and the B.Sc. degree in Mathematics, both from Cairo University, Cairo, Egypt, in 1966 and 1968, respectively. He received the Ph.D. degree in Electrical Engineering from Johns Hopkins University, Baltimore, MD in 1972.

From 1972 to 1976, he was a member of Technical Staff at GTE Laboratories, Waltham Research Center, Waltham, MA. From 1976 to 1978, he was with the faculty of the Electrical Engineering Department, King Fahd University of Petroleum & Minerals, Dhahran, Saudi Arabia. From 1978 to 1982, he was a member of Technical Staff at AT&T Bell Laboratories, Holmdel, NJ. From 1982 to 1985, he was an MTS Supervisor in the Product Certification Department at AT&T Information Systems, Lincroft, NJ. Since 1985, he has been Professor of Computer Engineering at King Fahd University of Petroleum & Minerals, where he founded the Computer Engineering Department and has been its Chairman from 1986 to 1992. During the academic year 1992-1993, while on sabbatical from KFUPM, he was a Visiting Professor at the VLSI Research Group, Department of Electrical & Computer Engineering, University of Waterloo, Waterloo, Ontario, Canada. His current research interests include digital logic design and testing, memory testing, automatic test pattern generation, and design for testability.

Mohamed I. Elmasry (S'69-M'73-SM'79-F'88) was born in Cairo, Egypt on December 24, 1943. He received the B.Sc. degree from Cairo University, Cairo, Egypt and the M.A.Sc. and Ph.D. degrees from the University of Ottawa, Ottawa, Ontario, Canada, all in Electrical Engineering in 1965, 1970, and 1974, respectively.

He has worked in the area of digital integrated circuits and system design for the last 27 years. He worked for Cairo University from 1965 to 1968, and for Bell-Northern Research, Ottawa, Canada from 1972 to 1974. He has been with the Department of Electrical and Computer Engineering, University of Waterloo, Waterloo, Ontario, Canada since 1974, where he is a Professor and founding Director of the VLSI Research Group. He has a cross appointment with the Department of Computer Science where he is a Professor. He holds the NSERC/BNR Research Chair in VLSI design at the University of Waterloo, Waterloo, Ontario, Canada since 1986. He has served as a consultant to research laboratories in Canada and the United States, including AT&T Bell Laboratories, GE, CDC, Ford Microelectronics, Linear Technology, Xerox, and BNR, in the area of LSI/VLSI digital circuit/subsystem design. During sabbaticals from the University of Waterloo, he was at the Micro Components Organization, Burroughs Corporation (Unisys), San Diego, CA, Kuwait University, Kuwait, and Swiss Federal Institute of Technology, Lausanne, Switzerland. He has authored and co-authored over 200 papers on integrated circuit design and design automation. He has several patents to his credit. He is editor of the IEEE Press books: *Digital MOS Integrated Circuits* in 1981, *Digital VLSI Systems* in 1985, *Digital MOS Integrated Circuits II* in 1991, and *Analysis and Design of BiCMOS Integrated Circuits* in 1993. He is also author of the book *Digital Bipolar Integrated Circuits*, Wiley, 1983, and a co-author of the book *Digital BiCMOS Integrated Circuits*, Kluwer, 1992.

Dr. Elmasry has served in many professional organizations in different positions including the Chairmanship of the Technical Advisory Committee of the Canadian Microelectronics Corporation. He is a founding member of the Canadian Conference on VLSI, the International Conference on Microelectronics, and the founding president of Pico Electronics Inc. He is a member of the Association of Professional Engineers of Ontario and is a Fellow of the IEEE for his contributions to "digital integrated circuits."