A Wideband Low-Noise Variable-Gain BiCMOS Transimpedance Amplifier

Robert G. Meyer, *Fellow, IEEE*, and William D. Mack, *Member, IEEE*

***Abstract*—A new monolithic variable gain transimpedance amplifier is described. The circuit is realized in BiCMOS technology and has measured gain of 98 kΩ, bandwidth of 128 MHz, input noise current spectral density of 1.17 pA/$\sqrt{\text{Hz}}$ and input signal-current handling capability of 3 mA.**

I. Introduction

FIBER-optic communication systems require the use of sensitive current-input preamplifiers to condition the electrical signals received in the form of current pulses from p-i-n diode or avalanche photodiode detectors. A commonly used topology is the transimpedance feedback amplifer whose (relatively) low input impedance and flat gain characteristic is well suited to this application [1]–[4]. Important specifications for such amplifiers include input current noise, input-current overload level, bandwidth, gain flatness, power dissipation, power-supply rejection and cost of fabrication.

In the design of fixed-gain transimpedance amplifiers for these applications, there is a direct tradeoff between input current noise and the input current overload level via the value of the shunt feedback resistor used in the signal path. For this reason, in applications requiring both large overload levels and low noise (very wide dynamic range), various means have been employed to vary the gain of the amplifier in response to the input signal level. [7], [10], [13], [14]. This gain variation allows very low noise and high gain to be achieved for small input signals, while the circuit can also handle large input signals with acceptably small duty-cycle distortion.

In this paper a new monolithic variable-gain transimpedance amplifier is described which achieves very low input current noise (1.17 pA/$\sqrt{\text{Hz}}$) in the highest-gain state and very high overload level (greater than 3 mA input signal) in the lowest-gain state. The circuit is realized in BiCMOS technology and is intended for use in applications up to 160 MBit/s.

II. Circuit Topology

The basic topology of the first two stages in the high-gain condition is shown in Fig. 1. A Darlington input stage composed of Q_1 and Q_4 drives resistive load $R_1 = 10$ kΩ through level-shifting diode Q_2. Emitter follower Q_3 drives the signal to the second-stage differential pair $Q_{24} - Q_{25}$ through level-shifting diode Q_8. Shunt feedback to the input from Q_3 emitter is transmitted via resistor $R_{F1} = 28$ kΩ and compensation capacitor $C_2 = 32$ fF [15]. An identical dummy stage is used to generate a matching bias voltage V_{REF1} at Q_{25} base to allow single-ended to balanced conversion. On-chip filtering essentially eliminates noise in V_{REF1}. From nodes A and B, emitter followers drive differential outputs V_{01} and V_{02} as shown in Fig. 2. Resistors R_{85} and R_{86} produce good matches to 50 Ω at each output. The provision of a differential output is important for rejecting common-mode signals in the connection to the post-amplifier where differential operation is also highly desirable.

The Darlington input is used for two reasons. First, this allows use of a large bias current and thus high gain in

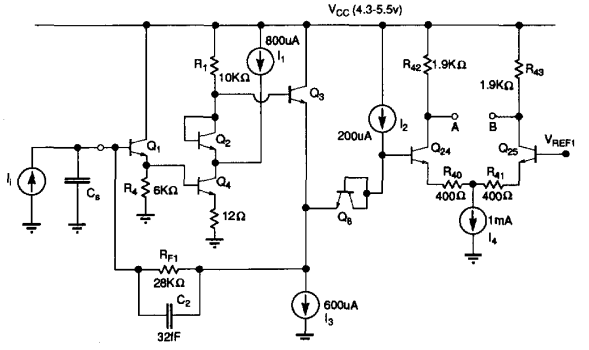

Fig. 1. Basic topology of the transimpedance amplifier in the high-gain condition.

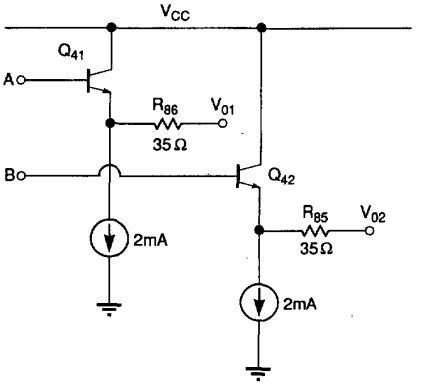

Fig. 2. Differential output stage.

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R. G. Meyer is with the Department of Electrical Engineering and Computer Sciences and the Electronics Research Laboratory, University of California, Berkeley, CA 94720.

W. D. Mack is with Philips Semiconductors, Sunnyvale, CA 94086.

$Q_4(I_{C4} = 1$ mA) while still giving a low input noise current contribution from $Q_1(I_{C1} = 140\ \mu$A). An NMOS FET is an alternative possibility for use as the main gain stage, but adds more input capacitance and consumes more bias current for the same gain. The 12 Ω resistor in Q_4 emitter is a variable element realized by a MOSFET to be described later. A second reason for the use of the Darlington stage is to raise the bias voltage at the input to allow adequate voltage swing on a gain control device connected between the base of Q_1 and the collector of Q_4. This is described later.

The bandwidth of the input stage (which dominates the whole amplifier) is set essentially by the zero contributed by R_{F1} and C_2. Thus,

$$f_{-3\,\mathrm{dB}} \cong \frac{1}{2\pi R_{F1} C_2} = 160\mathrm{MHz}. \tag{1}$$

Gain peaking in the amplifier is controlled by the secondary pole whose magnitude is determined by the RC product at the high-impedance node at the base of Q_3. The incremental resistance at this node is set by $R_1 = 10$ kΩ and the output resistance of current source I_1 (realized as a PMOS device) which is also about 10 kΩ. The voltage gain from the base of Q_1 to the emitter of Q_3 is thus,

$$A_V \cong \frac{5\mathrm{k}\Omega}{\frac{1}{g_{m4}+12}} \cong 125. \tag{2}$$

The input resistance and capacitance seen at the base of Q_1 can thus be determined by Miller-effect calculations as:

$$R_i \cong \frac{R_{F1}}{1 + A_V} = 240\Omega \tag{3}$$

$$C_i = (1 + A_V)C_2 = 4\ \mathrm{pF}. \tag{4}$$

This Miller capacitance dominates over the source capacitance of 0.1–1 pF (dependent on the photo detector used) and thus the circuit response is relatively independent of the value of C_S. This allows use of the amplifier in a wide variety of applications.

The mid-band equivalent input current noise of the amplifier is:

$$\bar{i_i^2} \cong 2qI_{B1}\Delta f + 4kT\frac{1}{R_F}\Delta f \tag{5}$$

$$\therefore \frac{\bar{i_i^2}}{\sqrt{\Delta f}} = 2 \times 1.6 \times 10^{-19} \times 1.2 \times 10^{-6} + 1.66 \times 10^{-20}\frac{1}{28,000}$$

$$= 0.98 \times 10^{-24}\ \mathrm{A^2/Hz}$$

$$\therefore \frac{i_i}{\sqrt{\Delta f}} \cong 1\ \mathrm{pA}/\sqrt{\mathrm{Hz}}.$$

The input overload current of the amplifier in the high-gain state is determined by the linear range of the second stage. This is approximately 600 mV at the base of Q_{24} giving an input-referred overload current of

$$I_i = \frac{600\ \mathrm{mV}}{28\ \mathrm{k}\Omega} \cong 20\ \mu\mathrm{A}. \tag{6}$$

The desired input overload current for this amplifier was 3 mA or higher. Thus some form of gain variation must be introduced to allow the circuit to absorb such large input drive currents while maintaining linear operation. Other performance characteristics which must be maintained under gain variation include bandwidth (which can go higher), absence of gain peaking and a nominal zero output differential offset. Modifications to the basic topology of Fig. 1 to achieve these goals are shown in Fig. 3. Variable resistors realized with NMOS devices are shown as R_A, R_B, R_C, R_D and R_E. These are turned on in a continuously controlled sequence in order to reduce the circuit gain and increase the overload point while maintaining other performance characteristics. Although the circuit exhibits symmetrical limiting for positive and negative input currents in the high-gain condition, low-distortion operation at very high input levels is only maintained for positive input currents as the gain is reduced. This limitation can be accommodated by appropriate connection of the circuit to the phototransducer. Alternatively, the bias current in Q_1 (basically set by I_1) could be increased to allow larger signal currents to be pulled from the input. This however has noise implications and the circuit frequency response would be affected by the larger capacitance associated with the physically larger current source.

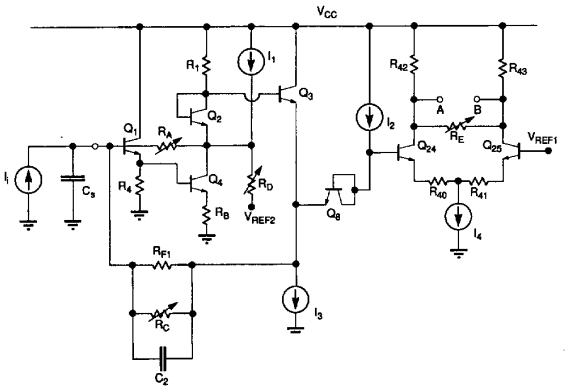

Fig. 3. Amplifier topology with variable-resistor MOSFET's included.

Resistor R_C shunting the feedback path is turned on first and has a minimum value of 15 kΩ. In parallel with $R_{F1} = 28$ kΩ this gives an effective shunt FB resistor of about 10 kΩ which reduces the transimpedance of the overall circuit by a factor of 3. However this also increases the feedback loop gain by a factor of 3 which would normally cause about a factor of 3 increase in circuit bandwidth and unacceptable gain peaking. This is eliminated by simultaneously turning on resistor R_D (realized as a 5/1 NMOS FET) which shunts the main high-impedance node in the forward path, thus reducing the loop gain and broadbanding the secondary pole. Appropriate control of these resistance variations results in a gain-frequency characteristic which shows essentially no peaking with gain reduction. Voltage V_{REF2} is generated on chip using the dummy transimpedance amplifier which also generates V_{REF1}. This prevents R_D from disturbing the dc bias in the amplifier. A matching set of variable resistors ensures that the dummy amplifier accurately tracks the main amplifier.

If all the gain reduction were accommodated by reducing R_C, current source I_3 would have to be large (more than

4 mA) to handle the large positive input signal currents. In addition, the very low minimum value required of R_C (about 200 Ω to give 0.6 V swing at Q_3 emitter with 3 mA input signal) would give severe problems in ensuring stability in the feedback amplifier. It is thus convenient to introduce variable resistor R_A as local shunt feedback around the Darlington. This has the advantage of maintaining well-specified circuit performance due to the resulting tightly-coupled feedback around the Darlington, while having much less severe stability problems than a similar resistor around the overall feedback loop. It was found useful to include variable resistor R_B (going from 10 Ω to 80 Ω as R_A goes from ∞ to 200 Ω) in order to eliminate moderate gain-frequency peaking caused by intermediate values of R_A. Resistor R_B is realized by a 400/1 NMOS device in shunt with an 80 Ω resistor. Note that large applied input signal currents are shunted to ground via Q_4 and R_B.

The minimum value of R_A of 200 Ω gives a maximum signal at Q_{24} base of 600 mV for 3 mA input signal at I_i. In order to allow the output voltage of the amplifier to be regulated to an even lower value (to reduce overload at the postamplifier input) variable resistor R_E (realized by a 100/1 PMOS device) is included between the collectors of Q_{24} and Q_{25} and is activated after R_A reaches its minimum value.

When resistor R_A is turned on to a value of 10 kΩ it will have lowered the amplifier transresistance by a factor of 2. (R_{F1} = 28 kΩ and R_C = 15 kΩ giving 10 kΩ effective already present in the circuit). From this value, we require R_A to drop further by a factor of 50 to about 200 Ω. This raises the issue of the linearity of R_A which is realized by an NMOS device with varying gate bias. Linearity of the overall amplifier characteristic is important to preserve the incoming signal duty cycle, and thus gross nonlinearity introduced by R_A must be avoided. The potential problem can be appreciated by examining the characteristics of a MOSFET used as a variable resistor. The $I_D - V_{DS}$ characteristics of a MOSFET are shown in Fig. 4 with the triode region boundary given by $V_{DS} = (V_{GS} - V_t)$. In the triode region the device characteristics can be represented as:

$$I_D = \mu C_{0X} \frac{W}{L}\left[(V_{GS} - V_t)V_{DS} - \frac{1}{2}V_{DS}^2\right], \qquad (7)$$

and the incremental resistance for $V_{DS} = 0$ is:

$$r_{ds} = \frac{dV_{DS}}{dI_D} = \frac{1}{\mu C_{0X} W/L(V_{GS} - V_t)}. \qquad (8)$$

Thus, in order to change r_{ds} over a given range, $(V_{GS} - V_t)$ must change by the same ratio. But the range of voltage swing allowable across the drain-source of a MOSFET in the triode region before gross nonlinearity occurs is directly related to $(V_{GS} - V_t)$. In fact $r_{ds} = \infty$ when $(V_{DS} = (V_{GS} - V_t)$ and the value of r_{ds} at $V_{DS} = \frac{1}{2}(V_{GS} - V_t)$ is already twice its value for $V_{DS} = 0$. This can be seen by differentiating (7) for arbitrary V_{DS} to give in general

$$r_{ds} = \frac{dV_{DS}}{dI_D} = \frac{1}{\mu C_{0X} W/L(V_{GS} - V_t - V_{DS})}. \qquad (9)$$

Since $(V_{GS} - V_t)$ is limited to a maximum value of about 2 V for V_{CC} = 4.3 V minimum (due to headroom considerations),

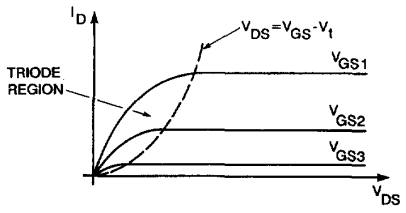

Fig. 4. MOSFET $I_D - V_{DS}$ characteristics.

a resistance variation in r_d of 10:1 means that at the maximum resistance value the voltage swing on V_{DS} must be limited to significantly less than 200 mV. For this reason, variable resistor R_A in Fig. 3 is realized by two parallel MOSFET's of different sizes which are turned on sequentially. The first MOSFET M_{19} (see Fig. 6) with $W = 7$ μm and $L = 1$ μm is turned on and reaches a minimum value of 1.5 kΩ for $(V_{GS} - V_t) \cong 2$ V. As M_{19} approaches its minimum resistance value a second parallel MOSFET M_6 (not shown) with $W = 50$ μm and $L = 1$ μm is activated across M_{19} and this device has a minimum r_{ds} = 200 Ω for $(V_{GS} - V_t) = 2$ V. This condition (M_6 fully on) allows very linear circuit operation with input signal currents up to and beyond $I_i = 3$ mA. All variable-resistance MOSFET's are turned on only with other significant shunt resistive elements present. In this way the large nonlinearity of a MOSFET resistor with small $(V_{GS} - V_t)$ is swamped by a much smaller linear resistance. As $(V_{GS} - V_t)$ is then increased further to reduce the total resistance, the MOSFET resistor becomes much more linear because of the larger value of $(V_{GS} - V_t)$.

These variable resistors (including R_E) in the gain path allow the overall circuit transresistance R_T from I_i to V_{AB} to be varied from $R_T \cong 100$ kΩ to $R_T \cong 40$ Ω. This allows the circuit to regulate the differential output voltage to a constant value as low as 120 mV for input currents varying from 0 to 3 mA.

III. Gain Regulation

The gain-setting resistor in the high-gain condition (R_{F1}) is a crucial element. Its tolerance directly affects the tolerance of the overall amplifier gain with important implications for worst-case system design. In addition, capacitive parasitics associated with R_{F1} contribute to the amplifier input shunt capacitance, which affects high-frequency noise performance. Finally, excess phase shift generated by R_{F1} contributes to stability problems in the amplifier. These issues are in conflict, since use of a large area resistor layout to better define the value of R_{F1} increases its parasitic capacitance. It is thus attractive to use a small area MOSFET in the triode region to realize R_{F1}, and then to overcome the tolerance problem by tying the gate of that MOSFET to that of a tracking MOSFET in a separate bias feedback loop which forces the tracking MOSFET to match a precision resistor. This is implemented as shown in Fig. 5 where MOSFET M_8 with $W/L = 3/3$ realizes R_{F1} = 28 kΩ nominal. The voltage across M_{13} (composed of eight matching MOSFET's each with $W/L = 3/3$ and surrounding M_8 in the layout) is forced to equal the voltage

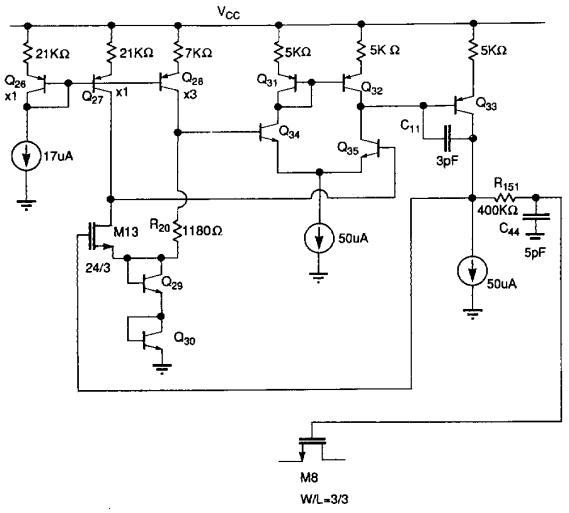

Fig. 5. Feedback amplifier setting the on-resistance of M_8 as a multiple of precision resistor R_{20}.

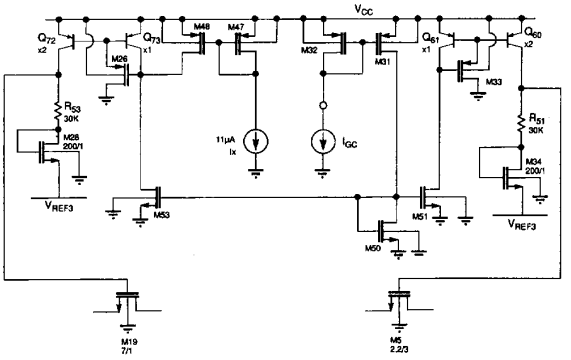

Fig. 6. Gain-control circuitry with precision gate-bias offsets for different variable-resistance MOSFET's.

across the large area precision resistor R_{20} (whose value is 1180 Ω) by the dc feedback loop through Q_{34}, Q_{35} and Q_{33} back to the gate of M_{13}. Since precision currents in Q_{27} and Q_{28} are ratioed by 3:1, the r_{ds} of M_8 will be nominally $3 \times 8 \times 1180 = 28.3$ kΩ. Resistor R_{151} and capacitor C_{44} represent a noise filter to prevent bias noise from reaching the gate of M_8, which is a very sensitive node in the circuit. Diodes Q_{29} and Q_{30} set the bias voltage on M_{13} channel close to that of M_8 (set by Q_1 and Q_4 in Fig. 1) and thus equalize body effect in these MOSFET's. Since resistor R_{20} is not in the high-frequency signal path, a large area layout can be used for precision without impacting rf performance.

IV. MOSFET Variable-Resistor Control

Variable resistors $R_A - R_E$ must be turned on in a controlled sequence in order to maintain the desired overall gain-frequency response and also to ensure a monotonic variation of amplifier gain versus gain-control input. Resistor R_C is realized by MOSFET M_5 whose gate is controlled by the gain-control current I_{GC} as shown in Fig. 6. Current I_{GC} is mirrored to M_{51} and Q_{60} and is then fed to M_{34} and R_{51} to create the gate bias for M_5. Voltage V_{REF3} is derived from the dummy input stage and tracks the dc voltage at Q_3 emitter which is the channel voltage bias for M_5. The control current in Q_{60} then raises the gate voltage of M_5 by one threshold voltage (from M_{34}) plus $I_{C60} \times R_{51}$.

Resistor R_A is comprised of two MOSFET's in parallel of which one (M_{19}) is shown in Fig. 6. The input control current I_{GC} is mirrored to M_{53} and Q_{72} and develops gate bias for M_{19} across R_{53} and M_{28}. A precision current $I_X = 11$ μA generated on-chip is mirrored to M_{48} and holds Q_{72} off until $I_{D51} = I_{C61} = 11$ μA also. At this point $I_{C60} = 22$ μA and $V_{G5} = (V_{REF3} + V_{t34} + 22 \times 10^{-6} \times 30\ \text{k}\Omega)$ and thus $(V_{GS} - V_t)_5 = 0.66$ V. Device M_5 is thus in conduction by a known amount when M_{19} begins to turn on. A similar offset scheme is used to turn on M_6 in parallel with M_{19} when $(V_{GS} - V_t)_{19} = 0.66$ V also. This scheme ensures both monotonicity and also that the nonlinearity of a MOSFET when turning on [low$(V_{GS} - V_t)$] is swamped by a shunting conducting MOSFET.

V. Parasitic Element Tolerance

This circuit exhibits a very large gain-bandwidth product and care must be taken to ensure stability in the presence of lead and package inductance and capacitive loading. Signal currents from the output stages produce voltages on the supply rail impedance that couple back to sensitive nodes at or near the input of the circuit via various parasitic capacitive paths. (For example, collector-base capacitance of Q_1). External capacitive loading at the emitters of Q_{42} and Q_{41} exacerbates this problem. Power-supply bond-wire and package inductance of several nanohenries is always present and much larger values are often created by the difficulties of external supply bypassing. It was found from SPICE simulations that both packaged and chip versions could be made to oscillate at frequencies in the hundreds of megahertz to gigahertz range with a number of combinations of supply-lead inductance (as low as several nanohenries but larger values made the problem predictably worse) and output-stage capacitive loading. Output buffer resistors R_{85} and R_{86} shown in Fig. 2 helped to reduce this tendency but the active supply bypass [16] shown in Fig. 7 was found necessary to eliminate all possibilities of oscillation. This circuit introduces an active broadband ac impedance of about 10 Ω (almost purely resistive over a wide bandwidth) between internal chip V_{CC} and internal ground, while only consuming about 3 mA of bias current. The active bypass returns signal currents from the V_{CC} rail to ground internally to the chip and the resulting ac voltages on supply and ground leads are limited to relatively small values. Supply-line resonances are essentially eliminated. With this bypass included, simulations showed the circuit to be completely stable (minimal ringing on transients) for any supply-line inductance up to 100 nH, output capacitive loading to 20 pF and ground inductances up to 10 nH.

VI. Computer Simulations

Extensive SPICE simulations confirmed theoretical predictions and showed total supply current of 22 mA from 5 V,

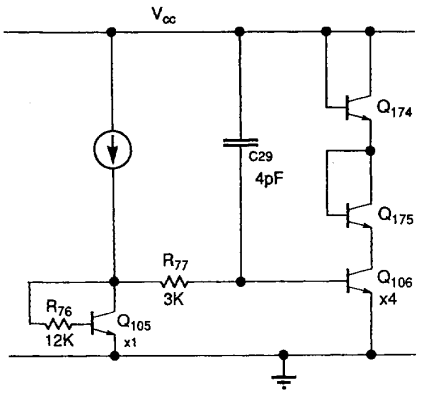

Fig. 7. Active supply bypass.

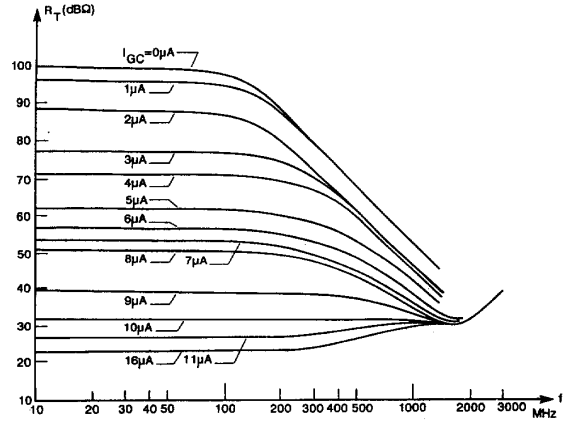

Fig. 8. Measured transimpedance versus frequency as a function of I_{GC}.

overall maximum transresistance (differential output) of 100 kΩ with $I_{GC} = 0$ and minimum overall transresistance of 40 Ω with I_{GC}. The −3 dB bandwidth was 190 MHz with $C_S = 0.1$ pF, 160 MHz at $C_S = 1$ pF and 60 MHz at $C_S = 10$ pF. The gain-frequency characteristic showed no peaking at maximum gain and less than 1 dB peaking for any gain setting. Power-supply-rejection-ratio was −60 dB at 10 kHz and −20 dB at 1 MHz. Equivalent input noise current was 1.05 pA/$\sqrt{\text{Hz}}$ up to about 20 MHz where it began rising (dependent on source capacitance). For $C_S = 0.4$ pF the total integrated equivalent input noise current was 15 nA from 0–120 MHz and 18 nA from 0–150 MHz. With $R_L = 1$ kΩ the overall transfer characteristic from I_i to $(V_{01} - V_{02})$ was linear within a few percent at all gain settings up to a maximum input signal swing of 0–4 mA at minimum gain.

VII. Measurements

The circuit was fabricated in Philips Semiconductors QUBiC BiCMOS process with peak npn f_T of 13 GHz, minimum $C_{\mu 0}$ of 6 fF and CMOS L_{eff} of 0.8 μm. For initial test purposes the IC was mounted in an 8-pin ceramic DIP. Power-supply current was very close to the nominal value of 22 mA. Overall low-frequency transresistance to the differential output was 98 kΩ at maximum gain. The measured gain-frequency characteristics versus gain-control current are shown in Fig. 8. The measured bandwidth of 128 MHz at maximum gain is close to that expected in this package and socket. The characteristics show essentially no peaking, although for very low gain values (actually large attenuation) board and package feedthrough in the gigahertz range is apparent.

Measured transimpedance versus gain control current I_{GC} is compared with the SPICE generated curve in Fig. 9. The two curves match well but are offset in slope by the variation of some on-chip resistors from their nominal values. The breakpoints where successive FET's are turned on are evident as is the monotonicity of the curve. In a closed-loop system, I_{GC} is generated by detecting the output voltage amplitude and feeding back a proportional control current I_{GC}.

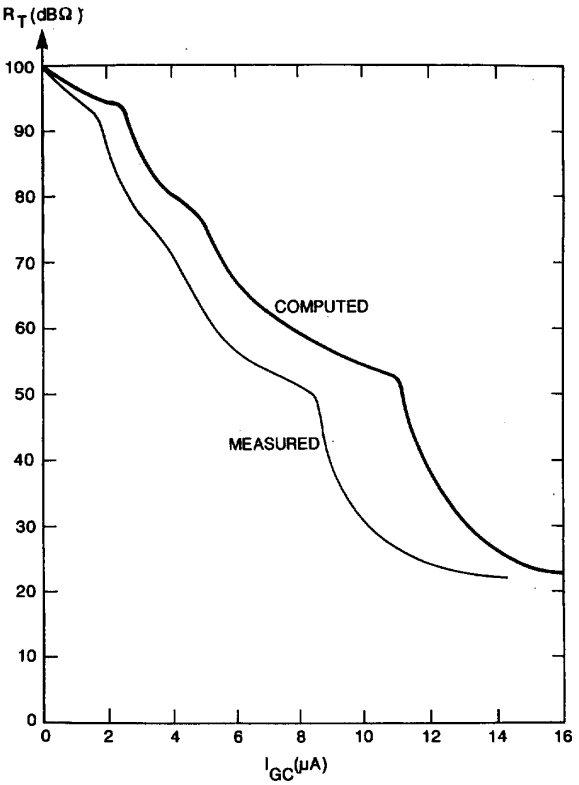

Fig. 9. Measured and computed transimpedance versus I_{GC}.

Amplifier tests with pulsed input currents showed no detectable duty-cycle distortion for output voltage swings up to several hundred millivolts over the gain control range, up to 3 mA pulses at minimum gain. Midband input noise current spectral density was 1.17 pA/$\sqrt{\text{Hz}}$. The measured dc transfer characteristics from I_i to V_0 (single-ended) are shown for maximum gain (50 KΩ single-ended transimpedance) in Fig. 10 and for reduced gain (160 Ω single-ended transimpedance) in Fig. 11.

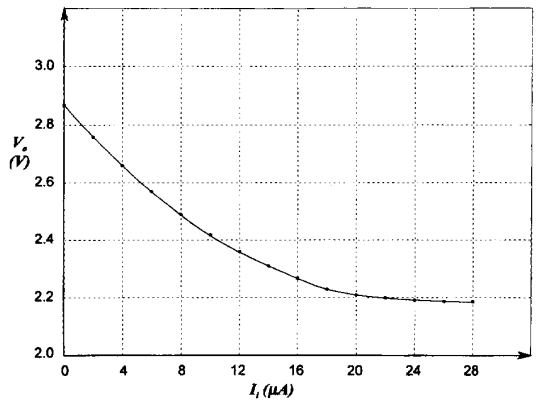

Fig. 10. Measured dc transfer characteristic at maximum gain.

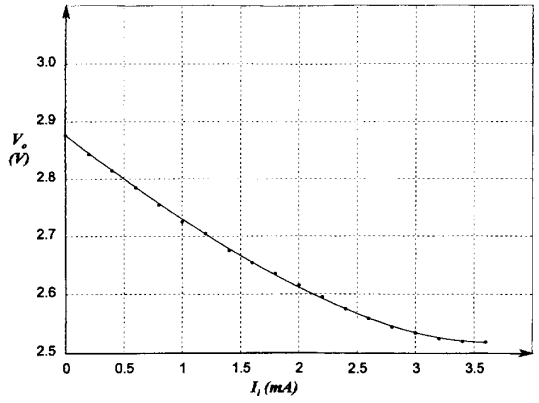

Fig. 11. Measured dc transfer 160 Ω characteristic at single-ended transimpedance.

VIII. Conclusion

A new monolithic variable-gain transimpedance amplifier has been developed using multiple sequentially switched MOSFETs as gain-control devices. Fabricated in a BiCMOS process the circuit achieves 1.17 pA/$\sqrt{\text{Hz}}$ input noise current density, 3 mA input signal-current handling capability, maximum transimpedance of 98 kΩ and bandwidth of 128 MHz. The circuit is tolerant of parasitic inductance and capacitance in all leads.

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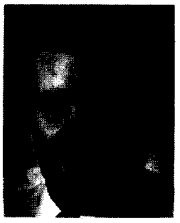
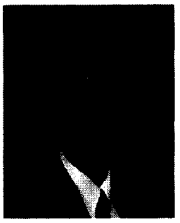


Robert G. Meyer (S'64-M'68-SM'74-F'81) was born in Melbourne, Australia, on June 21, 1942. He received the B.E., M.Eng.Sci., and Ph.D. degrees in electrical engineering from the University of Melbourne in 1963, 1965, and 1968, respectively.

In 1968, he was employed as an Assistant Lecturer in Electrical Engineering at the University of Melbourne. Since September 1968, he has been employed in the Department of Electrical Engineering and Computer Sciences, University of California, Berkeley, where he is now a Professor. His current research interests are in high-frequency analog integrated circuit design and device fabrication. He has acted as a consultant on electronic circuit design for numerous companies in the electronics industry. He is co-author of the book, *Analysis and Design of Analog Integrated Circuits* (New York: Wiley, 1993), and editor of the book, *Integrated Circuit Operational Amplifiers* (New York: IEEE Press, 1978).

Dr. Meyer was President of the IEEE Solid-State Circuits Council and was an Associate Editor of the IEEE JOURNAL OF SOLID-STATE CIRCUITS and of the IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS.



William D. Mack (S'76-M'79) was born in San Francisco, CA on December 12, 1955. He received the B.S. and M.S. degrees in electrical engineering from the University of California, Berkeley, CA, in 1977 and 1979, respectively.

He held teaching assistant/associate positions at the University of California, Berkeley, during 1978 and 1979. Summer engineering positions were held at the Space Science Laboratory, University of California, Berkeley, Ampex Corporation, Redwood City, CA, and Tektronix IC Design Group, Beaverton, OR. In 1979 he joined the Signetics Analog Circuit Research Group, Sunnyvale, CA, where he was engaged in the design of high-speed and high-accuracy bipolar integrated circuits. Presently he is the BiCMOS Methodology Manager for the Application-Specific Business Group of Philips Semiconductors. His current area of interest is advanced circuits and CAD for RF communications.

Mr. Mack is a member of Eta Kappa Nu.