A BiCMOS Low-Power Current Mode Gate

S. H. K. Embabi, D. E. Brueske and K. Rachamreddy

Abstract— **A controllable BiCMOS low-power current mode logic (LPCML) gate is proposed. The LPCML can be controlled to operate in a high-power mode when its inputs and outputs are in transition. When the gate is idle, it is in a low-power mode and the circuit maintains its output levels with very little tail current. A circuit implementation of the LPCML is also reported with a discussion on its design considerations. A circuit implementation of the LPCML with conventional CML indicates that its delay is greater than that of CML by about 60%. The power consumption of LPCML is proportional to the time it spends in the high-power mode, and, hence, may be significantly lower than that of CML.**

I. Introduction

While CMOS remains to be the technology most suitable for VLSI, it sometimes fails to satisfy the speed requirements. This is especially true for systems with critical paths that have large delays. Heimish *et al.* [1] have proposed the use of current mode logic (CML) to replace a CMOS carry lookahead chain, in order to reduce the propagation delay of the adder. The CML blocks can be used within a CMOS dominated system selectively to improve the overall system throughput at the expense of some additional power dissipation. However, the number of CML gates to be integrated will be limited by their DC power consumption which is a result of the DC tail current. In this paper, we introduce a controllable low-power CML (LPCML) gate which achieves speeds comparable to those of conventional CML with less power consumption.

The basic concept of the low-power CML is introduced in Section II. In Section III, an implementation of the LPCML is proposed. An analytical delay model is presented in Section IV. The important design consideration of the LPCML are discussed in Section V.

II. Basic Concept of the Low Power Controllable CML

One of the advantages of CMOS is its low DC power dissipation. The conventional CML gate (Fig. 1), on the other hand, consumes more standby power than CMOS. The DC current source (tail current) used in a CML gate is typically around 500 μA. Such a high current is required during the input and output transitions to guarantee fast switching. However, when the gate is idle (i.e., input is not changing), the tail current can be reduced significantly provided that the output levels are maintained.

The proposed gate can operate in a high-power mode (HPM) when the high current is needed during switching, and then go into a low-power mode (LPM) when the input is not changing and there is no need for the high current.

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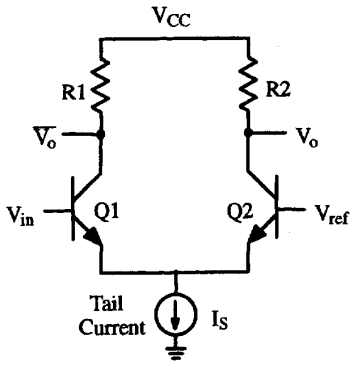


Fig. 1. Conventional CML gate.

Maintaining constant logic levels during mode changes is important to prevent erroneous data from propagating through the logic unit. This can be achieved by ensuring that the IR drop across the load remains constant. Therefore, a variable load that changes in proportion to the tail current is required. The tail current switches between two levels by means of a variable current source. The variable load can vary to exhibit low impedance for the HPM when the tail current is large. For the LPM the tail current is switched to its low level while the variable load is tuned to have large impedance. Fig. 2 shows the conceptual schematic of the (LPCML gate) with the variable current source and variable loads, which are controlled by an external signal Φ.

III. Implementation of the Low-Power CML

A possible implementation of the LPCML concept is shown in Fig. 3. The input and output voltages switch between V_{CC} and $V_{CC} - V_S$ where V_{CC} is the supply voltage and V_S is the voltage swing (e.g., $V_S = 500$ mV). When the control signal is high ($= V_{CC}$) the circuit is in the low-power mode, and when its low (GND) the circuit is in the high-power mode.

The operation of the variable current source can be described as follows. If Φ is high (i.e., LPM), then M_6 is off and current only flows through M_5. M_5, which has a small aspect ratio, in series with R_5 form a large impedance. Hence, the collector current of Q_2 is very small (e.g., 10 μA). This is mirrored to Q_4 to yield the desired small tail current, thus reducing the power dissipation. The sizing of M_5 and the resistance of R_5 are adjusted so that the drain-source voltage of M_5 is equal to V_S as will be explained in Section V. When Φ goes low (i.e., HPM) M_6 turns on. Because the aspect ratio of M_6 is greater than that of M_5 the collector current of Q_3, in the HPM, increases by about two orders of magnitude compared

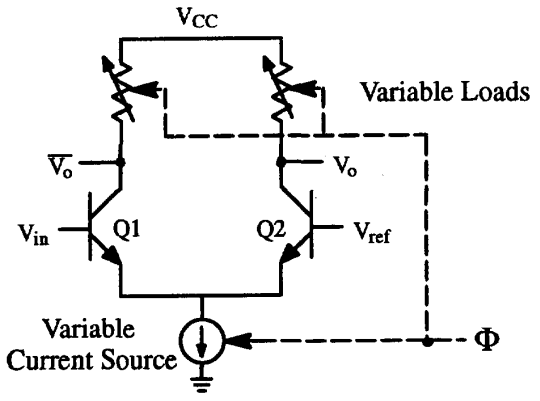


Fig. 2. Low-power CML gate with variable loads and variable current source.

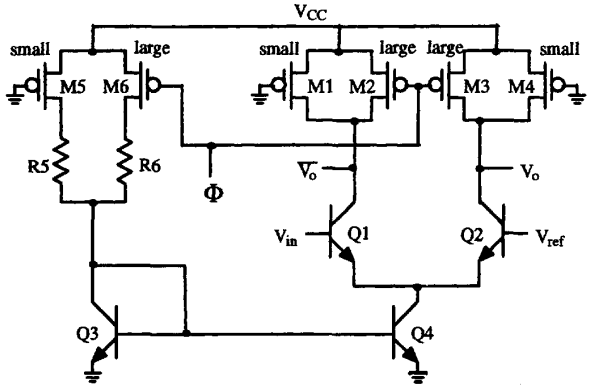


Fig. 3. Schematic of the LPCML gate using PMOS transistors for implementing the programmable loads and the current source.

to its value in the LPM. This high current is mirrored to Q_4. Again the drain-source voltage of M_6 is set to V_S by adjusting its W/L and the resistance R_6. Note that one variable current source (M_6, M_5, R_5, R_6 and Q_3) can be used for more than one LPCML gate.

The transistors M_1 to M_4 are constructed to form the variable loads. If Φ is high (i.e., LPM), transistors M_2 and M_3 are off, while M_1 and M_4 operate in the ohmic region. The resistance of M_1 and M_4, which have small W/L, is large enough so that the small current passing through any of them produces the desired V_S drop. When Φ goes low (i.e., HPM), all of the PMOS transistors M_1 to M_4 operate in the ohmic region. Since the tail current changes from low to high, the impedance of the load must be reduced to maintain the V_S drop across the parallel combination. This can be achieved by making the aspect ratio of M_2 and M_3 greater than that of M_1 and M_4. By designing the circuit in this manner a change from HPM to LPM will not alter the output voltage levels.

IV. Analytical Model for the Delay of the LPCML

The transient analysis of a conventional CML gate in [3] can be used for the LPCML to derive the following expression for its propagation delay:

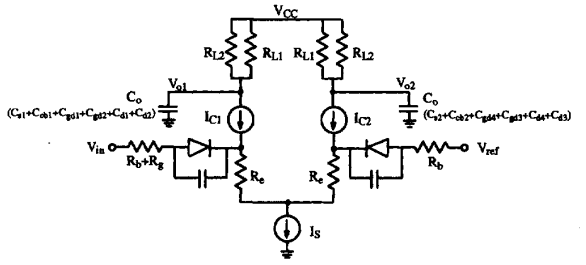


Fig. 4. Transient equivalent circuit of the LPCML. C_s is the substrate-collector junction capacitance, C_{cb} is the collector-base junction capacitance. C_{gd} is the gate-drain capacitance and C_d is the drain junction capacitance.

$$t_d = K_b\tau_b + K_c\tau_c \tag{1}$$

where, τ_b is a measure for the rate by which the tail current switches from one branch to the other, and is given by:

$$\tau_b = \frac{I_S\tau_f\beta R_t}{5V_t(1+\beta) + 2I_SR_e(1+\beta) + I_S(R_g + 2R_b)} \tag{2}$$

and τ_c is the output time constant and can be written as:

$$\tau_c = \frac{V_S}{I_S}C_o \tag{3}$$

where, C_o is the total output capacitance as shown in Fig. 4. K_b and K_c are given by:

$$K_b = \frac{1}{2}\ell n_D$$

$$K_c = \frac{1}{2}\ell n\left(\frac{(V_o(t_1) + V_S - V_{CC})(V_{CC} - V_o(t_2))}{0.5V_S^2}\right)$$

where,

$$V_o(t_1) = V_{CC} - DI_SR_L \times \left(1 + \frac{\tau_c}{\tau_b - \tau_c}e^{-t_1/\tau_c} - \frac{\tau_b}{\tau_b - \tau_c}e^{-t_1/\tau_b}\right)$$

$$V_o(t_2) = V_{CC} - V_Se^{-t_2/\tau_c} - D'I_SR_L \times \left[1 + \frac{(1-D)\tau_b}{\tau_c - \tau_b}e^{-t_2/\tau_b} + \frac{\tau_c - D\tau_b}{\tau_b - \tau_c}e^{-t_2/\tau_c}\right].$$

The parameters t_1, t_2, D, D', R_e, R_t, R_g, τ_f and β are all defined in Table I.

(1) yields fairly accurate delay estimates. This is demonstrated by the comparison between the delay times of HSPICE to those obtained from (1) as shown in Fig. 5(b).

V. Design Considerations for the LPCML

This section deals with some of the design issues such as the selection of the tail current and the definition of the voltage swing. A discussion on the transient behavior of the LPCML during mode switching and the power consumption is also included.

TABLE I
DEFINITIONS FOR (1).

$t_1 = \tau_b \ell n(\frac{D}{D-1})$
$t_2 = \tau_b \ell n(1-D)$
$D = \frac{A+2.5B}{5B+C}$
$D' = \frac{A'+2.5B}{5B+c}$
$A = \frac{1}{R_t}(R_e + \frac{R_b}{1+\beta} + \frac{V_S}{2I_S})$
$A' = \frac{1}{R_t}(R_e + \frac{R_b}{1+\beta} + \frac{V_S}{2I_S})$
$B = \frac{V_t}{R_t I_S}$
$C = \frac{1}{\beta} + 2\frac{R_e}{R_t}$
$R_t = R_g + 2R_b + 2R_e$
$V_t = kT/q$
R_b is the base resistance of Q_1 and Q_2 (Fig. 4).
R_e is the emitter resistance of Q_1 and Q_2 (Fig. 4).
R_g is the input source resistance (Fig. 4).
τ_f is the forward base transit time of Q_1 and Q_2.

A. Tail Current for Minimum Delay

(1) indicates that the delay is a function of τ_b and τ_c. τ_b is proportional to I_S as can be seen from (2). This is also illustrated in Fig. 5(a). The time constant τ_c, on the other hand, is proportional to $1/I_S$, which is also depicted in Fig. 5(a). At low values of I_S, the delay of the LPCML will drop as I_S increases because the $K_c\tau_c$ term dominates. As I_S increases $K_b\tau_b$ becomes comparable to $K_c\tau_c$, hence, the delay saturates. Further increase in the tail current results in a slow increase in the delay as shown in Fig. 5(b). It is interesting to note that the delay starts to saturate when $I_S = 400$ μA, which is approximately where $\tau_b \cong \tau_c$ (see Fig. 5(a)). Hence, the condition $\tau_b = \tau_c$ could be used as a design equation to find the optimum tail current[1]. This has been concluded in a previous study on conventional CML by Stork [4].

B. Setting of the Voltage Swing

Assuming that the HPM tail current is determined based on the $\tau_b = \tau_c$ condition, the tail current in the LPM, i_s, can be also determined as a fraction of I_S (e.g., $i_s = \frac{I_S}{50}$). The desired voltage swing can be achieved by selecting the appropriate values for R_5, R_6 and the aspects ratios of M_1 to M_6. In the LPM M_6, M_2 and M_3 are off. The drain voltage of M_5 is to be equal to V_S, hence

$$R_5 = \frac{V_{CC} - V_S - V_{BE}}{i_s} \tag{4}$$

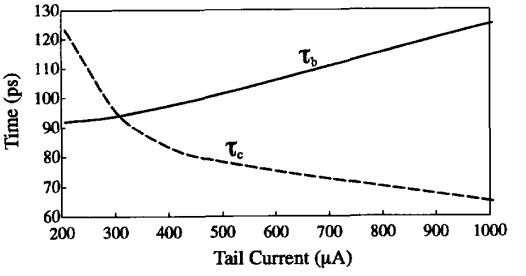
and

$$W_5 = \frac{L_{min}}{K_p} \frac{i_s}{(V_{CC} - V_T)V_S - \frac{V_S^2}{2}} \tag{5}$$

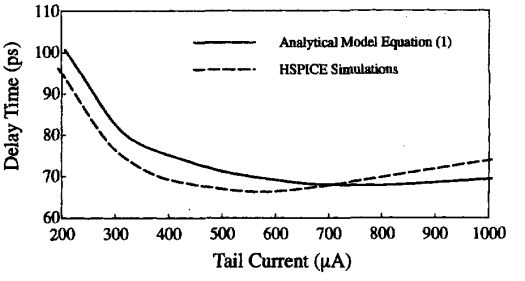
where, V_{BE} is the base-emitter voltage of Q_3, L_{min} is the minimum channel length and $K_p = \mu_p C_{ox}$.

The transistor on the conducting branch, whether it is M_1 or M_4, has the same gate-source voltage, the same size and the same current (i_s) as M_5. Therefore, its drain-source voltage should be equal to that of M_5. Thus, the output swing is set to V_S. Similarly, for the HPM the drain-source voltage of M_6 is adjusted to be equal to V_S when its on and its current is equal to I_S. R_6 and W_6 can be determined in the same manner as R_5 and W_5 respectively (i_s would be replaced by I_S in (4) and (5)). Since M_6, M_3 and M_2 are equally sized, the drop across M_3 or M_2 will be equal to that of M_6 ($= V_S$).

[1]Note that I_S here refers to the tail current in the HPM.



(a)



(b)

Fig. 5. τ_c and τ_b versus I_S, (b) The propagation delay of the LPCML version I_S. The analytical expression of the delay is in good agreement with HSPICE.

C. Transient Behavior During Mode Switching

Ideally the design would allow the output voltages to remain exactly the same as the power mode changes. However, there are transient deviations from the nominal voltage levels as can be seen in Fig. 6. When the control signal goes from low to high, the high output voltage level (out1) exceeds V_{CC} due to the capacitive coupling by the gate to drain parasitic capacitances of M_2 and M_3. The output voltage then slowly decreases and settles at V_{CC}. This transient behavior has no major effect on the driven gates.[2] The voltage level increases, but the logic level still remains the same. The low level output voltage (out2) decreases below its nominal value during the mode change because the variable load switches to its high impedance state slightly before the current switching takes place. The high impedance of the load increases the IR drop resulting in the output voltage shift. This transient glitch will not propagate to subsequent gates.

The output transient behavior caused by a low to high power mode change impacts the outputs in a more critical manner. The capacitive coupling between the gate and the drain of M_2

[2]Although the bipolar transistor of the emitter follower, may saturate, yet, the saturation is soft because the base-collector voltage is well below the V_{BE} (0.8 V) level. In addition, the effect of saturation will be insignificant because the emitter follower operates in the LPM. Hence, the collector current of the BJT of the emitter follower will be very small so that the charge acccumulated in its base will be small.

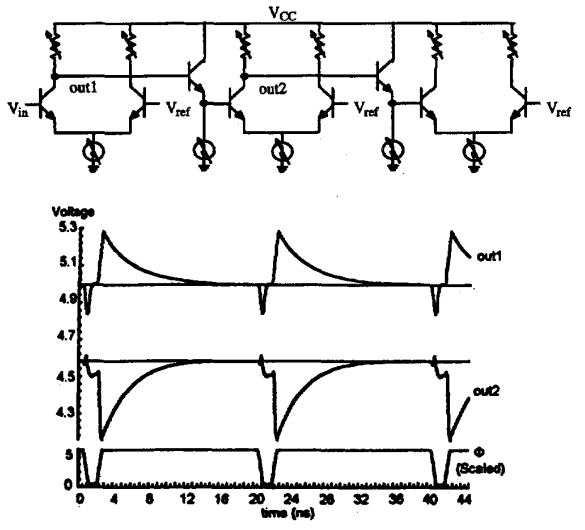


Fig. 6. The waveforms of the output voltage during power mode switching.

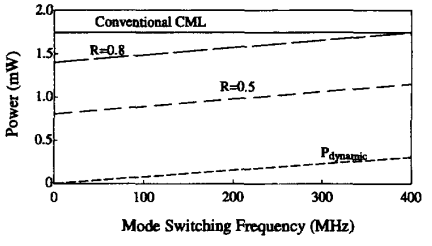


Fig. 7. Comparison between the total power consumed by a LPCML with that of conventional CML. As the LPCML spends more time in HPM, its power approaches that of CML. The effect of dynamic power is only significant at very high frequencies of power mode switching.

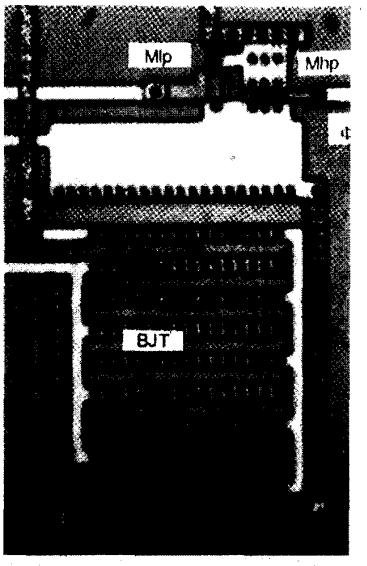


Fig. 8. Photomicrograph of a LPCML gates.

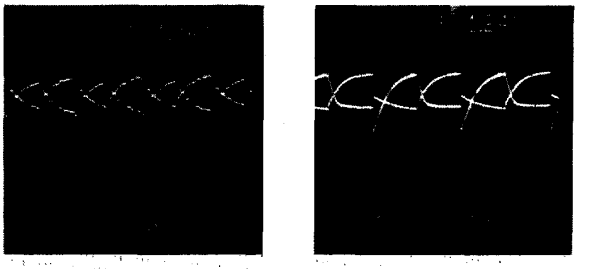


Fig. 9. The measured waveforms of the output voltage for (a) HPM and (b) LPM.

or M_3 reduces the high voltage level (out1) momentarily. The output voltage may approach the gate threshold voltage. Note, however, that the transient drop of out1 has little impact on the following gate output (i.e., out2) as shown in Fig. 6. Thus, false data does not propagate due to transients caused from both high to low and low to high mode changes.

D. Power Consumption of the LPCML Gate

The total power dissipated by the LPCML gate when it operates in the high-power mode is given by:

$$P_{\text{total}} = P_{\text{dc}} + P_{\text{dynamic}}, \tag{6}$$

where, P_{dc} is the DC power dissipation due to the tail current in high power mode, and P_{dynamic} is the dynamic power dissipation due to the switching of load and current source MOS transistors. The average power depends on the ratio of the time when the gate operates in the HPM to that of the LPM. If this ratio is R, then the average power can be written as

$$P_{\text{avg}} = RP_{\text{dc}} + P_{\text{dynamic}}. \tag{7}$$

Consider two cases as shown in Fig. 7. In the first case, the LPCML spends 50% of the time in the HPM (i.e., $R = 0.5$) and in the second case, it spends 80% of the time in HPM ($R = 0.8$). From Fig. 7, it can be concluded that if the load and the current source are switched too frequently (e.g., $R = 0.8$), the total average power dissipation approaches that of the conventional CML if the power mode is switching at 400 MHz and has no more advantage over conventional CML. However, if it operates 50% of the time in the HPM, the LPCML outperforms the conventional CML in terms of power consumption even if the power mode changes at a high rate.

The delay of a conventional CML has been compared to that of a LPCML. The simulation was performed for a chain of three gates of each type (Fig. 6). Using HSPICE, the minimum 50% propagation delay of the LPCML turned out to be greater than that of the CML by 60%. This difference in delay is mainly due to the extra parasitic capacitances of the PMOS loads. It is expected that this difference will decrease as the device features are scaled down.

VI. Experimental

The concept of the low-power current mode switch has been tested on silicon using the Orbit Analog 2 μm CMOS process available through MOSIS. This process offers a vertical NPN transistor, which has no buried layer and hence has a large

collector resistance. The photomicrograph of the input bipolar transistor and the PMOS transistors of the variable load are shown in Fig. 8. The aspect ratio of the PMOS transistors are 14/2 for Mhp and 4/9 for Mlp (Mhp corresponds to M_2 or M_3 while Mlp corresponds to M_1 or M_4). The area of the bipolar had to be large to achieve reasonable collector resistance. The measured waveforms of the output signals V_{o1} and V_{o2} are shown in Fig. 9. In the HPM the gate was switching at 3 MHz as demonstrated Fig. 9(a) and at 0.11 MHz in the LPM (Fig. 9(b)). The output signals in the LPM and the HPM had the same voltage swing which is about 1.24 V as illustrated in Fig. 9. The measured tail current in the HPM was 4.1 mA and 102 μA for the LPM.

VII. Conclusion

This paper presents a new concept to reduce the power consumption of CML. The new gate consumes power mainly when it is switching to guarantee high speed. The paper presents a possible implementation of the proposed concept. Simulations show that its delay is greater than that of conventional CML by 60%. However, its power consumption is a function of the gate activity and maybe significantly less than that of CML. A silicon prototype of the LPCML was also reported.

References

[1] W. Heimsch, *et al.*, "Merged CMOS/bipolar current switch logic (MCSL)," *IEEE J. Solid-State Circuits*, vol. 24, pp. 1307–1311, Oct. 1989.

[2] S. H. K. Embabi, *et al.*, *Digital BiCMOS Integrated Circuit Design*. Kluwer Academic, 1993.

[3] M. Y. Ghannam, R. P. Mertens and R. J. Van Overstreten, "An analytical model for the determination of the transient response of CML and ECL gates," *IEEE Trans. Electron Devices*, vol. 37, pp. 191–201, Jan. 1990.

[4] J. M. C. Stork, "Bipolar transistor scaling for minimum switching delay and energy dissipation," *IEDM Tech. Dig.*, 1988.