CMOS Four-Quadrant Multiplier Using Bias Feedback Techniques

Shen-Iuan Liu and Yuh-Shyan Hwang

Abstract—**A new wide-range CMOS four-quadrant multiplier using the bias feedback techniques [1]–[4] was presented. Simulation results show that for a power supply of ± 5 V, the linear range is over ±4 V and the linearity error is less than 1% over a ±3 V input range. Experimental results show that the linear range is over ±1 V. The results will be useful in analog signal processing applications.**

I. Introduction

RECENTLY, many efforts have been focused on the realizations of multiplier circuits based on the square-law characteristics of MOS transistors [2]–[8]. However, most CMOS multiplier circuits have a dynamic input range (for a linear output swing) which did not exceed 50% of the power supply [7]. A modified CMOS version of the Gilbert multiplier cell and a composite transistor based multiplier with ±4 V input range has been reported [7], [8]. Both the multiplier circuits using the active attenuators [7], [8] to obtain a wider input range. In the video and communication applications, both linearity and high frequency performances should be optimized simultaneously. In this paper, we proposed a new CMOS four-quadrant multiplier based on the bias feedback techniques [1]. It has a very simple configuration and a wide input range (±4 V) and the linearity error is less than 1% for input up to ±3 V. Moreover, its high frequency performance was also good.

II. Circuit Description

The proposed CMOS multiplier, shown in Fig. 1, was based on the bias feedback techniques [1]. The drain currents I_D of an NMOS transistor in the saturation and triode regions can be given as

$$I_D = K(V_{GS} - V_{Tn})^2 \tag{1}$$

and

$$I_D = 2K\left[(V_{GS} - V_{Tn})V_{DS} - \frac{V_{DS}^2}{2}\right] \tag{2}$$

where K is the transconductance parameter, V_{Tn} is the threshold voltage of the transistor and V_{DS} and V_{GS} is the drain-to-source voltage and the gate-to-source voltage, respectively. When V_X and V_Y are small, the transistors M_1–M_4 are operated in the triode region and M_5–M_8 operated in the saturation region with their sources connected to the substrate.

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Substituting (1) and (2) into Fig. 1, a routine circuit analysis yields:

$$I_1 = K(V_X - \overline{V}_B - \overline{V}_1)^2 \tag{3}$$

where,

$$\overline{V}_B = V_B + V_{Tn}, \overline{V}_1 = V_1 - V_B \tag{4}$$

and, [see (5), bottom of following page].

In general, the voltage V_B should be connected to the negative power supply. If $|V_X|, |V_Y| \ll V_B + V_{Tn}$, (3) can be approximated as:

$$I_1 = K\left\{\left(\frac{V_X - V_Y}{2}\right)^2 - \frac{\sqrt{2}(V_X - V_Y)}{2}\overline{V}_B \times \left[1 - \frac{V_Y}{\overline{V}_B} + \frac{V_X V_Y}{2\overline{V}_B^2} + \frac{V_Y^2 - V_X^2}{4\overline{V}_B^2}\right] + \frac{\overline{V}_B^2}{2}\left[1 - \frac{V_Y}{\overline{V}_B} + \frac{V_X V_Y}{2\overline{V}_B^2} + \frac{V_Y^2 - V_X^2}{4\overline{V}_B^2}\right]^2\right\} \tag{6}$$

The remaining currents I_2, I_3, and I_4 of Fig. 1 can be obtained similarly. Thus, the output current can be expressed by

$$I_0 = I_1 + I_3 - I_2 - I_4 = (2\sqrt{2})KV_XY_Y + K\frac{V_Y^2 - V_X^2}{2\overline{V}_B^2}V_XV_Y \tag{7a}$$

$$\cong (2\sqrt{2})KV_XV_Y. \tag{7b}$$

If $|V_X|, |V_Y| \ll V_B + V_{Tn}$, a four-quadrant multiplier can be obtained. Once this multiplier was used to be a squaring circuit, its linearity will be better. To widen the linear operation range of the proposed multiplier circuit, the magnitude of V_B should be increased. To guarantee linear operation for this circuit, the following conditions should be satisfied.

$$|V_X|, |V_Y| \le V_{1,2} + V_{Tn}. \tag{8}$$

The input range is given according to (8).

III. Error Analysis

Our previous analysis of the proposed circuits was based on the assumption that all the devices are ideal. However, practically the various second-order effects, such as mobility reduction, transistor mismatch, and channel length modulation will degrade the circuit performance. The channel length modulation effect can be improved by using the long channel length devices. In this section, we will only discuss the influence of mobility reduction and transistor mismatch.

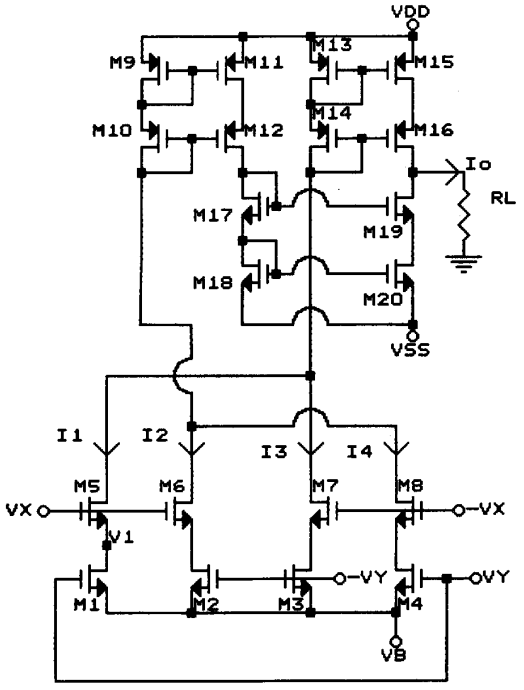

Fig. 1. The proposed four-quadrant multiplier circuit based on the bias feedback techniques.

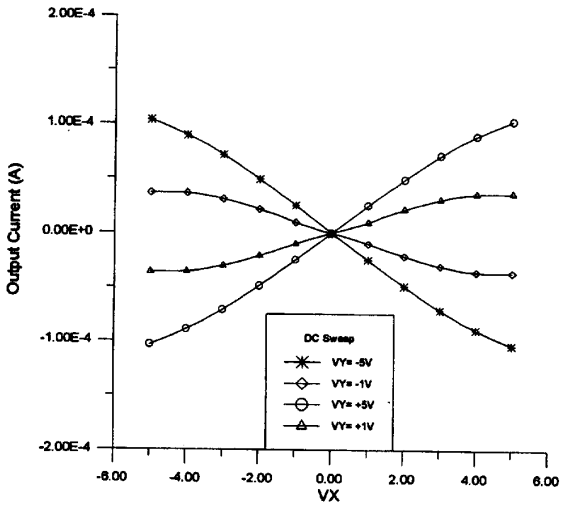

Fig. 2. The transfer characteristic curves of the proposed multiplier with $V_Y = \pm 5$ V, ± 1 V and $RL = 10$ kΩ. V_X changes from -5 V to 5 V.

TABLE I
THE ASPECT RATIOS OF THE MULTIPLIER IN FIG. 1

Transistor	$M_1 - M_8$	$M_9 - M_{16}$	$M_{17} - M_{20}$
$\frac{W}{L}$	$\frac{5\mu m}{20\mu m}$	$\frac{50\mu m}{10\mu m}$	$\frac{20\mu m}{10\mu m}$

A. Mobility Reduction

The simplified *I–V* characteristics of an NMOS can be modeled as [9]:

$$I_D = \frac{K(V_{GS} - V_{Tn})^2}{1 + \theta(V_{GS} - V_{Tn})} \tag{9}$$

where, θ is the mobility degradation parameter which has a value of about $0.1 \sim 0.001\ V^{-1}$. Substituting (9) into (3)–(7b), we can obtain the output current deviation (from that given by (7b)) as:

$$\Delta I_0 = -\frac{3\sqrt{2}}{2} K\theta \overline{V}_B \left(1 + \frac{V_Y^2 - V_X^2}{4\overline{V}_B^2}\right) V_X V_Y \tag{10}$$

where, the higher-order terms of θ were neglected. Both (7a) and (10) indicate the third-order harmonics will be dominant in the total harmonic distortion. Experimental results will be given to demonstrate this in the following section.

B. Transistor Mismatch

For the proposed multiplier in Fig. 1, let us assume that the transconductance parameters of the matched transistors M_1, M_3, M_5, and M_7 and those of the matched transistors M_2, M_4, M_6, and M_8 are $K + \frac{\Delta k}{2}$ and $K - \frac{\Delta K}{2}$, respectively. The output current deviation (from that given by (7b)) can be obtained as

$$\Delta I_0 \approx \Delta K \left[(1 + \sqrt{2})V_Y^2 - \frac{V_X^2}{4}\right]. \tag{11}$$

Hence, such mismatch will contribute to the second-order harmonics.

IV. SIMULATION AND EXPERIMENTAL RESULTS

The following simulation results are obtained using SPICE together with 3 μm p-well process parameters and MOSFET's with $V_{Tn} = 0.8$ V, $V_{Tp} = -0.85$ V, $K_n = 43.07$ μA/V^2, and $K_p = 20.79$ μA/V$_2$. The aspect ratios of all transistors are listed in Table I. The power supply is ± 5 V and $V_B = -5$ V. Fig. 2 shows the transfer curves of the multiplier circuit. This circuit has a linear range over ± 4 V and the nonlinearity error is less than 1% over ± 3 V input range. The total harmonic distortion of the output current was also evaluated and it is found to be less than 2.5% for $|V_X| < 5$

$$\overline{V}_1 = \frac{V_X + V_Y - 2\overline{V}_B + \sqrt{(V_Y - \overline{V}_B)^2 + 2(V_Y - \overline{V}_B)(V_X - \overline{V}_B) - (V_X - \overline{V}_B)^2}}{2} \tag{5}$$

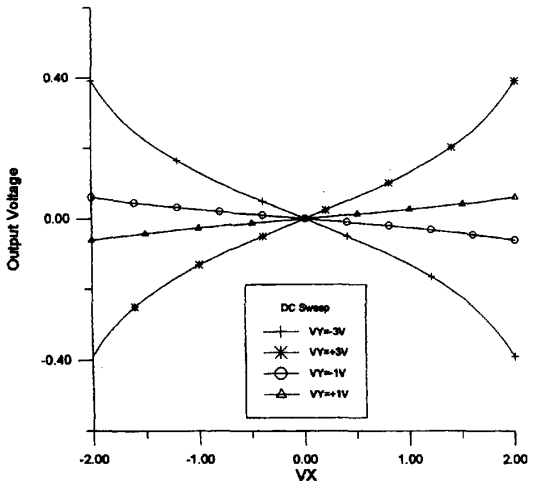

Fig. 3. The measured DC transfer functions of the proposed multiplier circuit with V_X changing from -3 V to $+3$ V and V_Y being equal to -3 V, -1 V, $+3$ V, and $+1$ V.

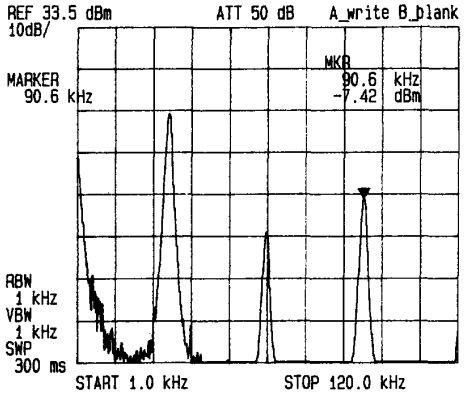

Fig. 4. A typical spectrum of the output voltage of the proposed multiplier. The vertical scale is 10 dBm/div.

V (peak-to-peak) and $|V_Y| < 5$ V. The simulated -3 dB bandwidth was about 20 MHz.

To demonstrate the feasibility of the proposed multiplier, we have breadboarded the multiplier circuit in Fig. 1 where two 50 kΩ resistors were used to replace the cascaded current mirrors. We use the NMOS transistors with their substrate connected to the negative power supply in a commercial CMOS transistor array (CA3600E). The phase inversion was achieved by an operational amplifier (LF356) and two 10 kΩ resistors. The power supply is ± 5 V and V_B is equal to -5 V. The measured DC transfer functions are shown in Fig. 3 with V_X being a triangular signal of 1 kHz changing from -3 V to $+3$ V and V_Y being equal to -3 V, -1 V, $+3$ V, and $+1$ V, respectively. To measure the harmonic distortion, a I–V sine wave of 30 kHz is applied to V_X while V_Y is 1 V. The measured spectrum of

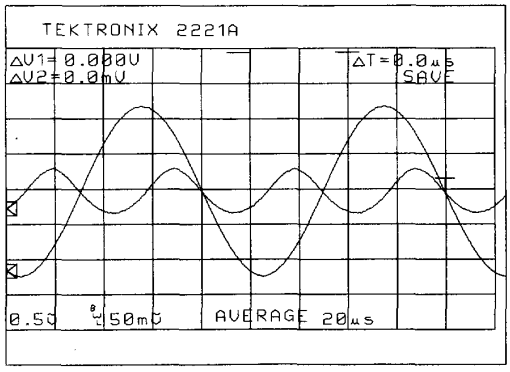

Fig. 5. The output waveform of the squaring circuit with a 2.42 V_{p-p} sinusoidal input signal of 10 kHz. The horizontal scale is 20 μs/div and the vertical scales are 0.5 V/div and 50 mV/div.

the output voltage of the multiplier is shown in Fig. 4. In Fig. 4, the third order harmonic distortion was dominant in the total harmonic distortion. As an example, a squaring circuit was also implemented based on this multiplier circuit. A 10 kHz sinusoidal signal with an amplitude 2.42 V (peak-to-peak) was applied to the input and its output waveform was shown in Fig. 5. Its -3 dB bandwidth was also measured to be about 820 kHz.

V. Conclusion

A CMOS four-quadrant multiplier using bias feedback techniques was proposed. Its performances have been demonstrated by SPICE and experiments. Second-order effects have been analyzed to evaluate the practical circuit performance. The circuit will be useful in many analog signal processing applications.

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