Programmable Switched-Current Wave Analog Filters

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***Abstract*— This paper presents a methodology to realize Programmable Switched-Current filters. A universal wave filter structure is built based on a low-pass (LP) to band-pass (BP) frequency transformation in the z-domain that allows obtaining different filtering functions from a single low-pass reference filter without altering the global circuit topology. Two different parameters, modified by changing the gain of current mirrors, independently control the filter bandwidth and center frequency. A 2.88-mm^2 IC prototype has been fabricated in a 1.6-μm CMOS digital technology that is capable of implementing three LP's (and their three complementary HP's) and nine BP's (and their nine complementary BR) Chebyschev filters. The realization of the 24 filtering functions requires less than 15% of additional area than that required to implement only one BP function. The chip operates from a 5-V supply, dissipates 0.83 mW/pole, and met the expected performance levels for all filter functions.**

I. Introduction

LOW-sensitive switched-current (SI) filters are based on the emulation of doubly-terminated LC ladder networks because of these circuits' low sensitivity to their element variations. Two different approaches have been explored to implement these SI filters. One applies the synthesis procedures broadly used for switched-capacitor (SC) filters [1], [2], the other, which has proven to be particularly interesting for SI techniques [3], [4], is based on the wave digital filter (WDF) concept developed by Fettweis [5]. Wave digital filters emulate the behavior of passive lossless reference filters by transforming passive L and C elements into one-port digital elements defined by an incident signal, a reflected signal, and a port resistance determined by the value of the corresponding analog element and the sampling frequency. The interconnection of one-port elements with different port resistances requires a multiport element called an *adaptor*.

In addition to their excellent passband sensitivity properties, WDF's have two inherent advantages. They are based on the bilinear transformation between continuous and discrete frequency domains, and they have a high degree of homogeneity involving very regular and simple structures formed by the interconnection of easy-to-design components (linear multiport and unit delay) instead of requiring high quality integrators.

In spite of both their wide acceptance in digital applications and their theoretical superiority, wave filters have been found impractical in analog when either continuous-time or switched-capacitors are used. However, since the basic operations required to implement Wave Analog Filters (WAF) are addition, subtraction, multiplication by a constant, and delaying, a current mode technique involving only accurate current amplifiers and simple memory cells appears highly suitable. We have already proved that the wave filter concept is worth considering as a practical manner to implement SI analog filters in low-voltage standard CMOS technologies [3], [4].

This paper intends to explore further this technique, providing a method to synthesize programmable SI filters which is demonstrated with a working IC prototype. We will show how different filtering functions can be obtained from a single low-pass reference filter relying on a universal wave filter structure. Section II describes the general procedure to build programmable structures, based on an LP to BP frequency transformation in the z-domain, which gives rise to a universal wave filter structure. Two different parameters of the transformation independently control the bandwidth and center frequency of the filter. The basic building blocks used in the programmable switched-current WAF are shown in Section III, together with some synthesis issues, which by exploiting the freedom in the choice of filter parameter values, leads to implementations that are less dependent on element tolerances and nonidealities. Section IV presents an IC prototype that implements a programmable 6-th order bilinear Chebyschev filter and its experimental results. Finally, Section V gives some conclusions.

II. Ppogrammable Filter Structure

A) Wave Filter Synthesis

A general procedure to realize a wave filter basically consists of two steps. First, a reference passive filter is constructed to meet the required frequency specifications. Then, a wave model is derived which emulates the reference filter. This wave model establishes the relationships between wave signals through modular building blocks (delays and adaptors). The wave model is described in the z-domain and the reference filter in the ψ-domain, in such a manner that the correspondence between domains is governed by the bilinear transformation,

$$\Psi = \frac{2}{T} \times \frac{1 - z^{-1}}{1 + z^{-1}} \tag{1}$$

where T is the sampling period.

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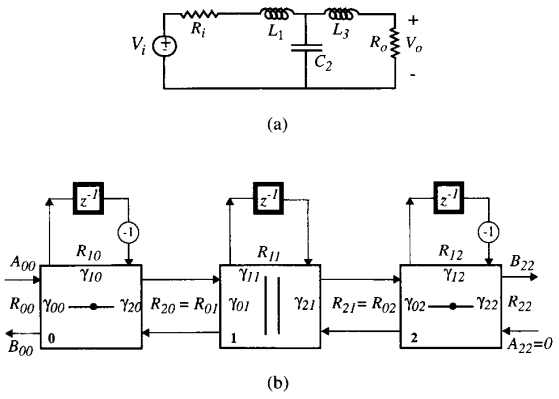


Fig. 1. (a) Third order reference ladder filter. (b) Wave model.

Wave filter structures that are easily modified to achieve programmability are those derived considering the passive elements in the reference filter as two-terminal elements [5] instead of two-port elements [6]. We will rely on these structures; thus, each passive component is represented by its incident (A_k) and reflected (B_k) wave variables, and is characterized by an equivalent port resistance whose value depends on the passive component value and the sampling frequency. Interconnections of components with different port resistances are realized by the corresponding adaptors, which are characterized by a set of reflection coefficients, γ_{ij} (see [5] or [7] for a detailed explanation). The general synthesis procedure is illustrated in Fig. 1 for a third order LP filter; the wave filter in Fig. 1(b), where adaptors 0 and 2 are series adaptors while adaptor 1 is parallel, is derived from the reference filter in Fig. 1(a). The following relations are met for an $f_s = 1/T$ sampling frequency:

$$R_{00} = R_i, R_{10} = \frac{2L_1}{T}, R_{11} = \frac{T}{2C_2},$$
$$R_{12} = \frac{2L_3}{T}, R_{22} = R_0 \tag{2}$$

$$\sum_{i=0}^{2} \gamma_{ij} = 2, \qquad j = 0, 1, 2 \tag{3}$$

where γ_{ij} are the adaptor reflection coefficients, which are defined as functions of the adaptor port resistances as we will see in Section III.

In general, for an N-th order filter only $N + 2$ values of the adaptor port resistances are fixed by the $N + 2$ passive element values and the chosen sampling frequency; the other $N - 1$ values (R_{2j} always equal to $R_{0(j+1)}$) can be chosen so that the most convenient values of γ_{ij} result. This is an important property of wave filters which eases achieving optimum adaptor realizations. It is worth mentioning that in analog implementations, none of the γ_{ij} values are limited by realizability conditions as in digital realizations.

Another interesting property of wave filters is that two complementary functions are simultaneously obtained; for instance, in the circuit shown in Fig. 1, the transfer function B_{22}/A_{00} is a low-pass function while B_{00}/A_{00} is its complementary high-pass function.

B) Programmable Band-Pass Architectures

Band-pass (BP) wave filters with any desired frequency specification can be obtained from a low-pass prototype (LPP) by applying a frequency transformation directly in the z-domain, without altering the overall filter structure. This involves substituting z^{-1} in the original LPP by extra elements implementing the LP to BP transformation [8]. In [7] we have shown that this property can be exploited to introduce programmability.

The following $z^{-1} \rightarrow g(z^{-1})$ transformation can be applied to develop a BP function from an LP function

$$g(z^{-1}) = -\frac{z^{-2} - \beta(1+\alpha)z^{-1} + \alpha}{\alpha z^{-2} - \beta(1+\alpha)z^{-1} + 1}, |\alpha| < 1, |\beta| \leq 1 \tag{4}$$

where parameters α and β characterize the normalized frequency warping associated with the mapping $z^{-1} \rightarrow g(z^{-1})$. Considering as a reference an LP filter whose bandwidth equals one fourth of the sampling frequency, parameters α and β are given by:

$$\alpha = \frac{1 - \tan\left(\frac{BW_0}{2}\right)}{1 + \tan\left(\frac{BW_0}{2}\right)} \tag{5}$$

$$\beta = \cos(\Omega_0) \tag{6}$$

where BW_0 and Ω_0 represent the normalized bandwidth and center frequency, respectively.

The effect of applying the mapping $z^{-1} \rightarrow g(z^{-1})$ in a wave filter structure is equivalent to making two modifications in the wave model [7], [9]. One of the modifications affects the value of the adaptor port resistances which are determined by the analog elements (i.e., R_{1j} in Fig. 1(b)); the new values are obtained as:

$$R'_{1j} = \frac{1 - m\alpha}{1 + m\alpha} \times R_{1j} \tag{7}$$

when $m = 1$ when a capacitor is simulated and $m = -1$ for an inductor. The second modification is equivalent to making the following transformation in the LP filter model

$$z^{-1} \rightarrow -z^{-1}\frac{z^{-1} - \beta}{1 - \beta z^{-1}}. \tag{8}$$

The latter can be realized by using a two-port adaptor with β as its reflection coefficient. Fig. 2 presents the resulting modified wave filter after applying $g(z^{-1})$ to the filter in Fig. 1(b). Note that each element z^{-1} has been replaced by a 2-port parallel adaptor connected to an extra z^{-1} element, and that the port resistances R_{1j} have been substituted by R'_{1j}, which must be $R'_{1j} = R_{1j}(1 + \alpha)/(1 - \alpha)$ for $j = 0, 2$ and $R'_{1j} = R_{1j}(1 - \alpha)/(1 + \alpha)$ for $j = 1$.

The wave model in Fig. 2 represents a universal wave filter structure where for $|\beta| < 1$ the function B_{22}/A_{00} is a BP filtering function and B_{00}/A_{00} is its complementary BR function, and for $\beta = 1$ they are an LP and an HP filter function, respectively. From (7) and (8) and considering (5)

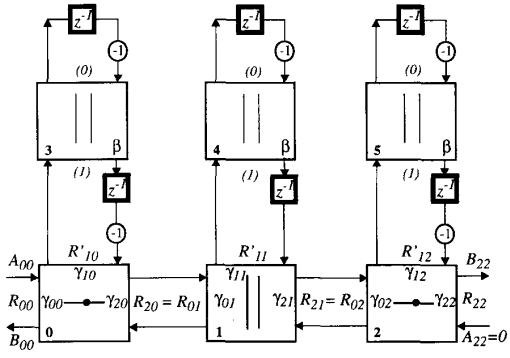


Fig. 2. Universal wave structure obtained after applying the $z^{-1} \rightarrow g(z^{-1})$ transformation to the LP wave filter in Fig. 1(b).

and (6), it can be concluded that frequency specifications of the BP functions can be modified as follows:

1) The bandwidth, which is determined by the parameter α, is controlled by modifying the port resistances R'_{1j}, and hence changing the value of the γ_{ij} parameters in the 3-port adaptors.
2) The center frequency is controlled by modifying the reflection coefficients β of the 2-port adaptors (all of them having the same value).

Summarizing, we can independently and simultaneously modify the bandwidth and the center frequency by varying adaptor coefficients. Practical implementations of this universal structure must provide the way to vary these coefficients. The particular value of β equal to 1 (to implement an LP filter) can be done directly bypassing the 2-port adaptors (e.g., providing the appropriate switches) since $\beta = 1$ implies that $A_1 = B_1$ in these adaptors.

III. Basic Building Blocks

Incident and reflected wave signals are represented by currents in switched-current wave analog filters. Thus, the filter consists of an arrangement of current-mode adaptors and current delay cells establishing direct correspondence between wave flow signal models and SI circuits. The involved elements must be interconnected in such a way that the incident wave in a port of an element is the reflected wave of the adjacent element. Hence, for SI elements and their interconnection we need a sign criterion for currents; we will assume that currents modeling incident (reflected) waves are considered positive when they enter (leave) the corresponding port.

This section presents practical implementations for the required building blocks as well as some design issues for efficient realization.

A) Parallel and Series Adaptors

Adaptors are multiport linear circuits implementing algebraic relationships between incident (A_j) and reflected (B_j) wave variables. For general n-port adaptors, these relations are:

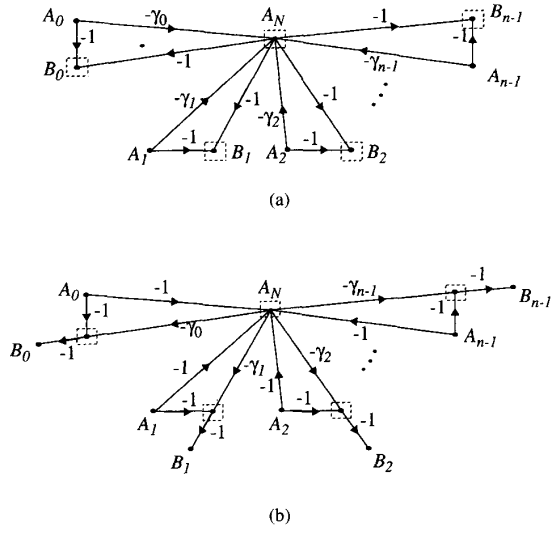


Fig. 3. SFG for an n-port (a) parallel adaptor, (b) series adaptor.

1) Parallel Adaptors:

$$B_j = \sum_{i=0}^{n-1} \gamma_i A_i - A_j, \qquad j = 0, 1, \ldots, n-1 \tag{9}$$

$$\gamma_i = 2G_i \left(\sum_{k=0}^{n-1} G_k \right)^{-1}. \tag{10}$$

2) Series Adaptors:

$$B_j = A_j - \gamma_j \sum_{i=0}^{n-1} A_i, \qquad j = 0, 1, \ldots, n-1 \tag{11}$$

$$\gamma_j = 2R_j \left(\sum_{k=0}^{n-1} R_k \right)^{-1} \tag{12}$$

where γ_k represents the reflection coefficient in port k.

Considering wave variables as current signals, these adaptors are easy to realize as an interconnection of current mirrors. Fig. 3 shows the general signal flow graphs (SFG's) for the two types of n-port adaptors. The transmission of each branch represents the gain of a current mirror. Nodes inside a dashed square are summation nodes and hence they are no more than a wired connection of current-mirror outputs. Fig. 4 gives a simplified schematic of the circuit we propose to implement the SFG of a 3-port parallel adaptor. In practical implementations, the cascode configuration shown in Fig. 5 has been used for each current mirror to improve its performance. Nonideality effects can be significantly reduced by using these or other cascode configurations, appropriate dimensioning and biasing, as well as careful layouts [10], [11].

Note from Fig. 3 that we need two coefficients, γ_0 and γ_1, for a 2-port adaptor. However, these adaptors were represented with only the β coefficient in the last section. This is the result

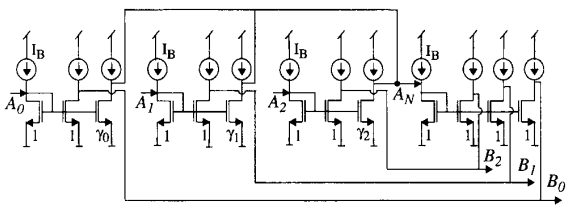


Fig. 4. Simplified schematic for a three-port parallel adaptor.

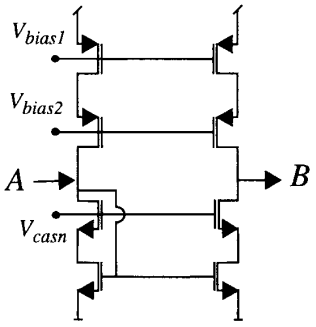


Fig. 5. Cascode current mirror.

of manipulating its equations, which leads to:

$$B_0 = A_1 + \beta(A_1 - A_0) \tag{13}$$

$$B_1 = A_0 + \beta(A_1 - A_0) \tag{14}$$

where the new parameter β is defined as $\beta = 1 - \gamma_0 = \gamma_1 - 1$.

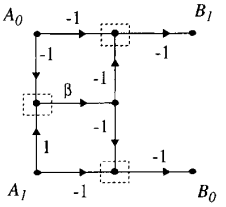
The SFG and the corresponding simplified schematic for this new 2-port adaptor are shown in Fig. 6. Note that the output inverting stages are not included in Fig. 6(b); they are not necessary when using the universal structure in Fig. 2, because of the existence of current inverters at one or both adaptors.

The advantage of using this implementation is evident from the programmability point of view, since only one parameter needs to be varied from one specification to another. Of course, simpler implementations of (13) and (14) can be derived, for instance that given in [7], but trade-off with easy programmability must be considered.

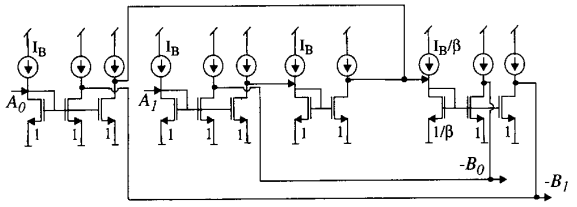
B) Delay Cells

The output current of the z^{-1} element (reflected signal, B) must be its input current (incident signal, A) delayed a whole sampling period; that is, $B(n) = A(n-1)$. In addition, since both currents are processed in continuous time by the connected adaptor, the output must be available during the same phase that the input is sampled; hence, input and output must be isolated from one another.

The cascade of two switched-current memory cells, each built as a current mirror with a switch separating its input



(a)



(b)

Fig. 6. (a) SFG for a two port parallel adaptor using only one coefficient. (b) Current mode realization.

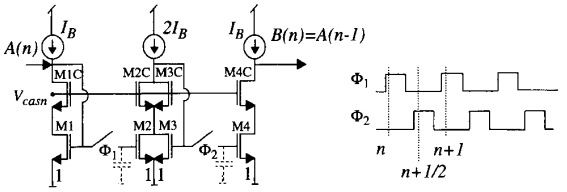


Fig. 7. Delay cell.

and output transistors, serves this purpose when the respective switches are controlled by two nonoverlapping clock phases. Thus, a possible delay cell is that shown in Fig. 7 where a cascode current mirror is used to improve its performance, as well as to obtain error-free connection with adaptors realized using the same cascode current mirrors.

We used this cell in the fabricated filter. An aspect ratio of 60 μm/10 μm for the holding transistors, and minimum sized NMOS switches (4 μm/2 μm) with dummy switch (2 μm/2 μm) were chosen. A simple charge injection reduction technique was used since, in the cascade of two memory cells, as is our case, charge injection offset errors can be nearly equal in the two cells and thus almost cancelled.

Alternative delay cells may be built resorting to dynamic current mirrors [12]; the main advantage of this approach is that it overcomes the matching limitations of standard current mirrors. However, since two basic dynamic current copiers are still needed to provide the required isolation between input and output, the mismatching errors are still evident between cells.

Charge injection due to clock feedthrough is the main cause of error in the delay cells, and specific techniques should be applied to reduce it. The use of dummy switches or adaptive cancellation circuits, together with small switch transistor area

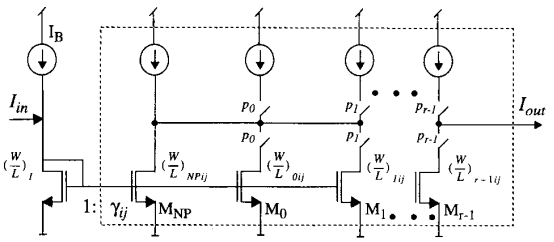


Fig. 8. Current mirror with programmable gain.

when compared with holding transistor area, are some of these techniques. However, the most effective charge injection cancellation technique seems to be the recently reported S^2I approach [13].

C) Programmability Issues

In Section II, we have shown that to make programmable WAF filters we must provide a way to vary the adaptor reflection coefficients. Since in SI realizations these parameters are attained as current mirror gains, we can modify them by using mirrors with variable gain. A simple technique for these mirrors is to alter the aspect ratio of transistors in the output branch of the mirror. This is easily done with an array of transistors connected in parallel through a set of digitally controlled switches. Fig. 8 illustrates this approach; assuming equal channel length for all transistors, the gain $\gamma_{ij} = W_{ij}/W_I$, which represents the i-th port coefficient of the j-th adaptor, is given by:

$$\gamma_{ij} = \frac{1}{W_I}(W_{NPij} + p_0 W_{0ij} + p_1 W_{1ij} + \ldots + p_{r-1} W_{(r-1)ij}) \tag{15}$$

where the subscript NP stands for a common output branch, $W_{lij}(l = 0 \text{ to } r-1)$ represents the channel widths of transistors in the extra output branches needed to implement the different gain values, and $p_l(l = 0 \text{ to } r-1)$ is the l-th bit of the digital control word.

The scheme in Fig. 8 allows us to realize a set of filter responses by incrementally programming the corresponding γ_{ij} coefficients. Since for any response the sum of coefficients in each adaptor must be 2, the sum of the total increments in its coefficients required to go from one response to another must be zero. In particular, the increments in the coefficients of a 3-port-parallel adaptor can be expressed as:

$$\Delta\gamma_{0j} = -\gamma_{0j}K_j \quad \Delta\gamma_{1j} = (2-\gamma_{1j})K_j \quad \Delta\gamma_{2j} = -\gamma_{2j}K_j \tag{16}$$

where K_j is a function of the increment $\Delta R_{1j} = R'_{1j} - R_{1j}$ imposed by the required change in the filter bandwidth,

$$K_j = \left(1 + \frac{\sum_{i=0}^{2} R_{ij}}{\Delta R_{1j}}\right)^{-1}. \tag{17}$$

TABLE I
γ_{ij} VALUES FOR THREE DIFFERENT BANDWIDTHS

	BW_{o0}	BW_{o1}	BW_{o2}
γ_{0j}	0.320	0.427	0.513
γ_{1j}	1.580	1.373	1.187
γ_{2j}	0.100	0.200	0.300

TABLE II
BANDWIDTH PROGRAMMING

p_0p_1	BW_{o0}	BW_{o1}	BW_{o2}
γ_{0j}, γ_{2j}	00	10	11
γ_{1j}	11	01	00

TABLE III
TRANSISTOR WIDTHS [μm] FOR THE THREE BANDWIDTHS

	W_{NPij}	W_{0ij}	W_{1ij}
γ_{0j}	19.20	6.40	5.2
γ_{1j}	71.20	12.40	11.20
γ_{2j}	6.00	6.00	6.00

The above relations facilitate the control signal; thus, the digital word controlling the γ_{1j} values in a 3-port adaptor is the complement of the word controlling the values of γ_{0j} and γ_{2j}. Since one of the responses can be determined by the coefficients implemented by the common fixed branches, the number of programming bits, r, which is determined by the number of tailored responses, f, will be $r = f - 1$. Let us illustrate the approach with the following example. Consider that the values of the γ coefficients for one of the 3-port adaptors in a filter corresponding to three different bandwidths, $BW_{oi}(i = 0, 1, 2)$, are those given in Table I. It is easy to verify that the channel widths in Table III result for the control word in Table II and for $W_I = 60\,\mu$m.

D) Accuracy Considerations

In practice, the above circuits suffer from limitations and errors which degrade their ideal performance. Known design tradeoffs and layout strategies given for current mirrors and memory cells can be considered to increase the accuracy of our building blocks. However, WAF accuracy considerations can be taken into account in the synthesis phase prior to the design of each component. This is due to the fact that there is not one-to-one correspondence between the filter coefficients and the adaptor coefficients; thus, values for the latter could be found which lead to more accurate implementations. To choose the most convenient set of adaptor coefficients we consider three sources of inaccuracy:

1) Quantization errors due to the fact that not all dimensions are integer multiples of the technological grid. Because of these errors, not all coefficients will be equally accurate in practice.
2) Mismatching random errors in current mirrors. Since these errors depend on mirror gains, they could be reduced by an appropriate choice of coefficient values.
3) Clock-feedthrough induced errors which are not exactly cancelled by any circuit technique.

Regarding quantization errors, we model them as functions of a parameter λ which represents the technological grid. Since

any coefficient γ (or β in 2-port adaptors) can be expressed as $\gamma = W_2/W_1$, if we assume an exact realization for W_1 then the actual gain γ_R in a technology with grid λ can be expressed as:

$$\gamma_R = \frac{\lambda}{W_1} \text{integer}\left(\frac{W_2}{\lambda}\right) \tag{18}$$

So, the percentage of relative error in the realization of γ is given by:

$$E^{0/0}\lambda(\gamma) = \left|\frac{\lambda}{\gamma W_1} \text{integer}\left(\frac{\gamma W_1}{\lambda}\right) - 1\right| \times 100. \tag{19}$$

(19) allows determining the γ values more convenient in a given technology and for a specific design with a particular W_1 value. For instance, for a $\lambda = 0.4\,\mu$m and a $W_1 = 60\,\mu$m, quantization errors higher than one percent can be expected for many γ values lower than 0.33.

Mismatching and clock feedthrough errors produce gain, dc offset, and linearity errors in the building blocks, which are the cause of deviations in the filter passband. In addition, charge injection provokes the movement of the zeros at $z = -1$, which also produces deviations in the attenuation band at high frequencies. We have studied the extent of these effects as a function of the adaptor coefficient values.

To evaluate transistor mismatch effects, the model given in [11] has been used for the random variations in current mirror gains produced by the fabrication process. The variances of gain mismatch errors associated with the actual realization of each filter component (delay cells and adaptors) are evaluated according to the following procedure. First, determine the number of current mirrors and their respective gains in the path from one input to one output. Second, assuming that the mismatching error in each mirror modeled as a Gaussian distribution is not correlated with the error in the other mirror, add all errors in each input-output path. Thus, considering that $\sigma'^2(1)$ is the relative variance of the unity-gain current mirror, given by:

$$\sigma'^2(1) = \frac{\sigma^2(I_1)}{I_1^2} = \frac{K_I}{WLN_1} \tag{20}$$

where N_1 is the number of unit transistors used in the realization of each transistor in the mirror and K_I is a process and bias dependent parameter [11], the following variance matrix results for the mismatching error in the 3-port parallel adaptors in Fig. 4

$$\begin{bmatrix} \sigma'^2_{00}(\gamma_0 - 1) & \sigma'^2_{01}(\gamma_1) & \sigma'^2_{02}(\gamma_2) \\ \sigma'^2_{10}(\gamma_0) & \sigma'^2_{11}(\gamma_1 - 1) & \sigma'^2_{12}(\gamma_2) \\ \sigma'^2_{20}(\gamma_0) & \sigma'^2_{21}(\gamma_1) & \sigma'^2_{22}(\gamma_2 - 1) \end{bmatrix} = \frac{\sigma'^2(1)}{2} \cdot \begin{bmatrix} \left(5 + \frac{1}{\gamma_0}\right) & \left(3 + \frac{1}{\gamma_1}\right) & \left(3 + \frac{1}{\gamma_2}\right) \\ \left(3 + \frac{1}{\gamma_0}\right) & \left(5 + \frac{1}{\gamma_1}\right) & \left(3 + \frac{1}{\gamma_2}\right) \\ \left(3 + \frac{1}{\gamma_0}\right) & \left(3 + \frac{1}{\gamma_1}\right) & \left(5 + \frac{1}{\gamma_2}\right) \end{bmatrix}. \tag{21}$$

On the other hand, the variance of the unit delay cells gain is given by:

$$\sigma^2(z^{-1}) = 2\sigma'^2_{(1)}. \tag{22}$$

Similar modeling was performed for series adaptors, as well as for the mismatching induced DC offset errors. More details on these models can be found in [14] and [15].

It can be seen from (21) that mismatching errors become more important as γ approaches zero. This effect can be taken into account in the design phase by implementing coefficients with low values as a set of current mirrors whose total gain is given by $(1 + \gamma) - 1$. Thus, alternative matrix entries of $(9 + 1/(1 + \gamma))$ or $(7 + 1/(1 + \gamma))$ appear, which means that using this alternative effectively reduces the mismatch error for $\gamma < 0.207$. As an illustration of the order of magnitude, consider the unity-gain mirror with $(W/L)_1 = 60\,\mu$m/$10\,\mu$m, $N_1 = 6$ and $(V_{GS1} - V_{T1}) = 0.6$ V; the standard deviation evaluated by (20) is about 0.28%, while the matrix of the standard deviation in the parallel adaptor with $\gamma_0 = 0.3\,\gamma_1 = 1.187$ and $\gamma_2 = 0.513$, is

$$\begin{bmatrix} \sigma'_{00}(\gamma_0 - 1) & \sigma'_{01}(\gamma_1) & \sigma'_{02}(\gamma_2) \\ \sigma'_{10}(\gamma_0) & \sigma'_{11}(\gamma_1 - 1) & \sigma'_{12}(\gamma_2) \\ \sigma'_{20}(\gamma_0) & \sigma'_{21}(\gamma_1) & \sigma'_{22}(\gamma_2 - 1) \end{bmatrix} = \begin{bmatrix} 0.57 & 0.39 & 0.44 \\ 0.50 & 0.48 & 0.44 \\ 0.50 & 0.39 & 0.52 \end{bmatrix} \tag{23}$$

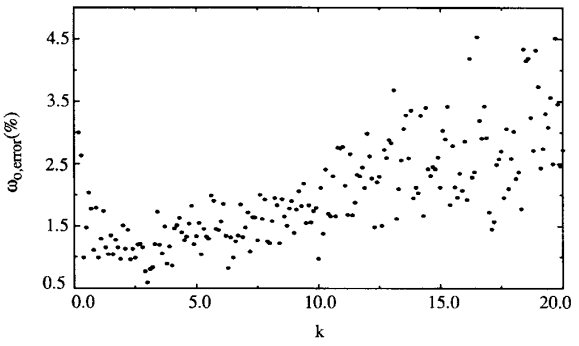
which means that the maximum standard deviation corresponds to the $(\gamma_0 - 1)$ coefficient, and is equal to 0.57%.

Clock-feedthrough in current memory cells can be modeled by an error voltage on the data holding node. Thus, defining this error as $\Delta\nu_f$, the equation for the delay cells including clock-feedthrough can be approximated by:

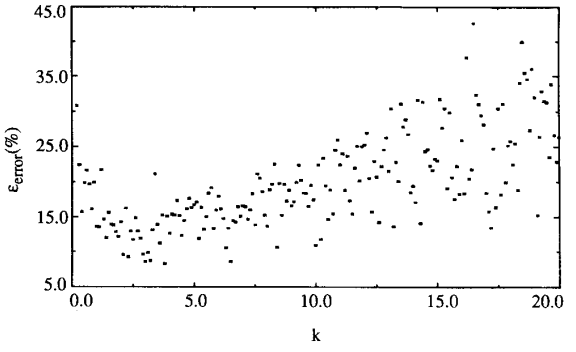
$$I_o(n) = I_{in}(n-1) + \Theta\left(\sqrt{I_B + I_{in}(n-1)} - \sqrt{(I_B - I_{in}(n-1)) - \frac{\Theta^2}{4} - \Theta\sqrt{I_B + I_{in}(n-1)}}\right) \tag{24}$$

where $\Theta = 2\sqrt{\beta_n}\Delta\nu_f$.

Using the above models, the sensitivity of the proposed filters to the main source of errors derived from their actual circuit structure can be evaluated in the synthesis phase. Since for a given filtering function, the induced errors differ for different values of the adaptor coefficients, we can explore the space of the possible coefficient values which allow us to select those which lead to more accurate implementations. We use an in-house program including these models to carry out numerical simulations, which eases our solving the performance trade-off in the synthesis phase [14]. Mismatching errors are randomly generated using the standard deviation derived from (20)–(22), and clock-feedthrough errors are included giving a value to $\Delta\nu_f$ in (24). As an illustration, Fig. 9 shows the relative errors in the ripple and cut-off frequency obtained in a third-order low-pass filter for different values of ratio $k = \gamma_{20}/\gamma_{00}$ and for $\Delta\nu_f = 1$ mV. It can be noted that there are values of k which produce low deviations in the filter characteristics.



(a)



(b)

Fig. 9. Evolution of (a) cutoff frequency and (b) ripple errors for different values of $k = \gamma_{20}/\gamma_{00}$ and for $\Delta\nu_f = 1$ mV in a low-pass WAF filter.

IV. IC Implementation and Experimental Results

An LC ladder reference filter for a third-order low-pass Chebyschev filter with 0.2-dB ripple in the passband and a normalized 0.25 cutoff frequency was chosen to demonstrate the feasibility of the proposed structure. The normalized values of the elements in the reference filter (which has the same schematic as in Fig. 1) were taken from a filter function table and are $L_1 = L_3 = 1.2275, C_2 = 1.1525$, and $R_i = R_0 = 1$. Applying the proposed methodology, we have derived a programmable filter prototype implementing: a) nine 6-th order band-pass functions with normalized bandwidths $\mathrm{BW}_{o0} = 0.0246$, $\mathrm{BW}_{o1} = 0.0563$, and $\mathrm{BW}_{o2} = 0.0957$, and normalized center frequencies $\Omega_{o0} = 0.167, \Omega_{o1} = 0.201$, and $\Omega_{o2} = 0.234$; and b) three third order low-pass functions corresponding to the three former bandwidths. The chip was designed in a single-poly standard 5-V 1.6-μm CMOS process, and the synthesis was carried out exploring the space of adaptor coefficients with better expected performance. Scaling was necessary due to non-homogeneous distribution of signal levels in the filter and to avoid distortion. Adaptor transformation and inclusion of some scaling constants [7] were performed, resulting in a final filter structure like that in Fig. 2, but with all 3-port adaptors of the parallel type. The above filtering functions are obtained as B_{22}/A_{00}; the respective complementary band-reject and high-pass functions

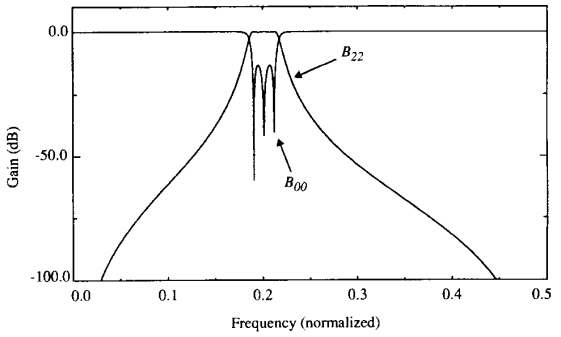


Fig. 10. Ideal band-pass (B_{22}) and band reject (B_{00}) functions corresponding to $BW_{o0} = 0.0246$ and $\Omega_{o1} = 0.2016$.

TABLE IV
Transistor Widths [μm] for the 3 Bandwidths and 3 Center Frequencies

	W_{NPij}	W_{0ij}	W_{1ij}
γ_{00}, γ_{22}	6.00	6.00	6.00
γ_{10}, γ_{12}	71.20	12.40	11.20
γ_{20}, γ_{02}	19.20	6.40	5.20
γ_{01}	2.40	5.20	6.80
γ_{11}	91.20	10.40	13.60
γ_{21}	2.40	5.20	6.80
	$W_{NP\beta}$	$W_{2\beta}$	$W_{3\beta}$
β	6.00	12.00	12.00

are also simultaneously obtained as B_{00}/A_{00} due to the Feldtkeller equation ($|B_{22}/A_{00}|^2 + |B_{00}/A_{00}|^2 = 1$), which is fulfilled in this kind of structures. Fig. 10 illustrates this property; the two expected functions corresponding to BW_{o0} and Ω_{o1} are plotted. Note that the theoretical attenuation level in the band-reject function (~ -14 dB) corresponds to the specified 0.2 dB ripple in the band-pass function.

The dimensions given in Table IV were obtained to implement the indicated adaptor coefficients for a 200 kHz clock frequency, an $I_B = 10\,\mu$A, and 60 μm/10 μm transistors in the input side of each mirror, ($L = 10\,\mu$m for all transistors). Two digital words, p_0p_1 and p_2p_3, independently control the γ and β values in the same way as illustrated in Table II. Note that the symmetry in the 3-port adaptors corresponds to the symmetry in the reference filter. The chip occupied 2.88 mm^2, and its microphotograph is shown in Fig. 11. The circuit was measured using an external simple V–I converter at the input and a 100 KΩ resistor at the output; some of the experimental filter functions are shown in Figs. 12–15. Note that the shape of the responses corresponds to that expected, and that the passband ripple in the low-pass filter is exactly as specified. A summary of the measured performance parameters for some of the implemented band-pass filtering functions is given in Table V; the error measured for the bandwidth and center frequency was less than the 4% and 1%, respectively, for the band-pass functions, and less than 1% in the cutoff frequencies of the low-pass functions. Although the circuit was designed for a 200-kHz clock, it has been measured up to 500 kHz, maintaining its functionality with a bandwidth error of 7% and a center frequency error of 1.25% in the worst case.

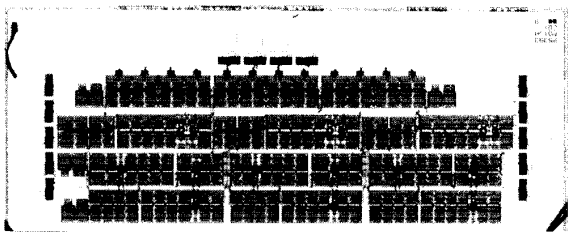


Fig. 11. Chip microphotograph.

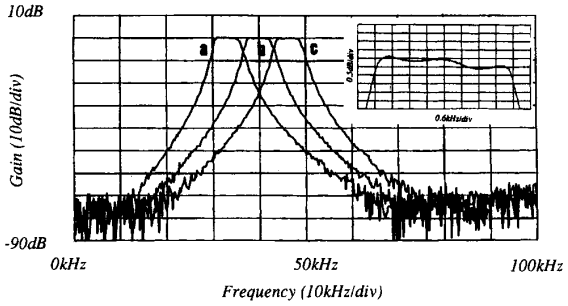


Fig. 12. Measured band-pass functions for a 200 kHz clock, $BW_{o0} = 0.0246$ and three different center frequencies: (a) $\Omega_{o0} = 0.1665$ (b) $\Omega_{o1} = 0.2016$ and (c) $\Omega_{o2} = 0.2340$.

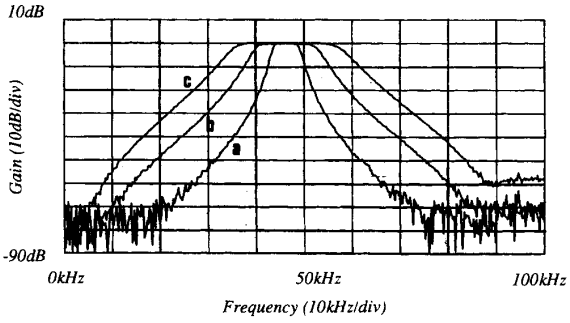


Fig. 13. Measured band pass functions for a 200-kHz clock, $\Omega_{o2} = 0.2340$ and three different bandwidths: (a) $BW_{o0} = 0.0246$ (b) $BW_{o1} = 0.05631$ and (c) $BW_{o2} = 0.09578$.

V. Conclusions

A methodology to realize programmable SI wave analog filters has been applied to simultaneously obtained different BP, BR, LP, and HP filters. Without modifying the global circuit structure, independently controlled bandwidths and center frequencies are established by merely changing the gains of current-mirrors using transistor arrays. A 2.88 mm^2 IC prototype has been designed in a 5-V 1.6-μm CMOS digital technology that is capable of implementing three LP (and their three complementary HP) and nine BP (and their nine complementary BR) Chebyschev filters. Most of the design work was carried out at the block coefficients determination phase because of the multiple possible solutions, with the result that some of them led to more accurate realizations. The chip was exhuastively measured and its performance levels met expectations in all the cases; the main deviation was found in the passband ripple of the band-pass functions, which affected the bandwidth measurement.

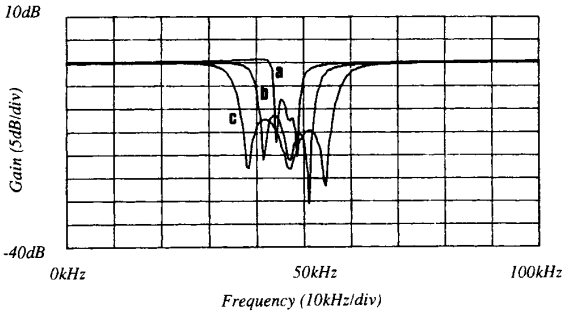


Fig. 14. Measured band reject functions for a 200-kHz clock, $\Omega_{o0} = 0.234$ and the three different bandwidths: (a) $BW_{o0} = 0.0246$ (b) $BW_{o1} = 0.05631$ and (c) $BW_{o2} = 0.09578$.

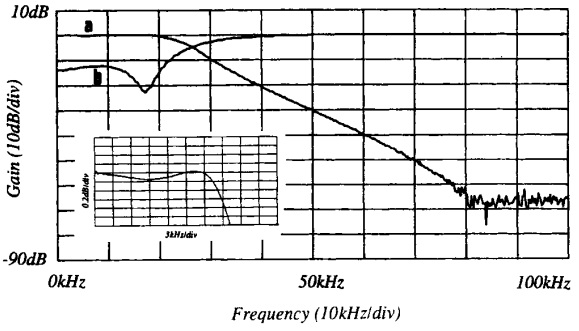


Fig. 15. Measured (a) low-pass and (b) high-pass functions for a 200 kHz clock and for $BW_{o2} = 0.09578$.

TABLE V
Some Band-Pass Filter Characteristics

	Simulated	Measured
f_{CLOCK}	200 kHz	200 kHz
BW_0^*	4.80 kHz	4.75 kHz
BW_1^*	11.08 kHz	10.80 kHz,
BW_2^*	18.80 kHz	18.10 kHz
$\Omega_0^\dagger$	33.50 kHz	33.55 kHz
$\Omega_1^\dagger$	40.44 kHz	40.15 kHz
$\Omega_2^\dagger$	46.88 kHz	46.90 kHz
Pass-band ripple	0.3 dB	0.5 dB
DR (6 μA input)	—	>78 dB
THD (6 μA input)	—	<0.2%
Floor-noise	—	70–80 dB
noise (BW_0)	—	6.5 nA $_{RMS}$
noise (100 Hz, 100 kHz)	—	10.3 nA $_{RMS}$
Power (DC)	4.9 mW	5.0 mW
Area (without pads)	—	2.88 mm^2

†Measured for $BW_0 = 4.8$ kHz
*Measured for $\Omega_{o0} = 33.5$ kHz

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