A Multi-Purpose CMOS Sensor Interface for Low-Power Applications

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***Abstract*— A dedicated low-power CMOS transponder microchip is presented as part of a novel telemetry implant for biomedical applications. This mixed analog-digital circuit contains an identification code and collects information on physiological parameters, i.e., body temperature and physical activity, and on the status of the battery. To minimize the amount of data to be transmitted, a dedicated signal processing algorithm is embedded within its circuitry. All telemetry functions (encoding, modulation, generation of the carrier) are implemented on the integrated circuit. Emphasis is on a high degree of flexibility towards sensor inputs and internal data management, extreme miniaturization, and low-power consumption to allow a long implantation lifetime.**

I. Introduction

In several biomedical research fields a great need emerges for reliable and miniature integrated sensor systems. The application of telemetric links hereby is imperative because they allow gathering of information without restraining their subjects. To support these research activities an expedient device is developed, based on previous research [1], [2], in the form of an implantable or portable telemetry system, monitoring body temperature and physical activity. A dedicated low-power mixed analog-digital CMOS integrated circuit combines several sensor interfaces, the processing and control circuitry and the telemetry unit.

II. Design Constraints

Perhaps the most stringent limitation for the design is the available time. Being only a small part of a comprehensive research project, the design time was limited to six man-months. Such a constraint has major implications on the design of a fairly complex system. In order to minimize the overall design time the standard-cell design technique is used whenever possible. On the one hand this technique reduces the design time substantially. On the other hand it might enlarge the required silicon area. Occasionally some specifications must be somewhat relaxed due to the fact that one appeals to readily available library circuits. The full custom design technique is only used when the standard cell approach is not satisfactory or is not capable of generating the desired circuit configuration or performance.

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Since the system is designed to be implantable, extreme miniaturization and low-power consumption are essential. The latter requirement is met using several techniques. First of all, by selecting a CMOS technology, a lower power consumption can be achieved in comparison to other IC technologies. However, it is also mandatory to optimize the analog circuitry towards low-power consumption. Extensive switching of the circuits even further reduces the consumed power. The analog input channels are only powered when necessary and their activity is kept to a strict minimum. Most of the power consumption is caused by the telemetry stage. Therefore the transmission time is reduced drastically, first, by limiting the amount of data to be transmitted. This is achieved by on-chip processing of the sensors' information without losing any vital data. This results in only 4 bytes of data: two bytes of temperature information, one byte of activity information, and another byte containing the identification code, the status of the battery and some control flags. Secondly, the baud rate of the transmission link is set to 4096 bits per second, which is relatively high for an implanted telemetry unit, but it allows it to keep the activation time of the telemetry stage to a strict minimum. The low-power consumption requirement demands on–off keyed AM transmission, so half of the time no carrier signal is transmitted. Finally the oscillator circuit responsible for the generation of the high-frequency carrier is switched on only during transmissions. Circuits are put in standby mode in between consecutive samples and transmissions, whenever possible.

Although miniaturization is of extreme importance, some redundant silicon area is granted for reason of testability and flexbility. In order to obtain this, the circuit's floor-plan is very modular. All digital circuits, including the 8-bit A/D-converter, are combined into one subchip. The analog input channels are placed on three other subchips, while the crystal oscillator forms the last subchip. A lot of bond pads are added for testing purposes.

III. General Concept

Fig. 1 shows the general block diagram for the integrated circuit. The shaded areas represent the analog circuits, while the non-shaded areas are digital circuits. The input and output control signals are marked for each block.

The black squares represent the bonding pads, which control part of the operation of the device. They define the 5-bit identification code and they select the time between consecutive transmissions (eight possible intervals are defined, ranging from 1 s to 512 s). Within a 36 h period the device transmits a

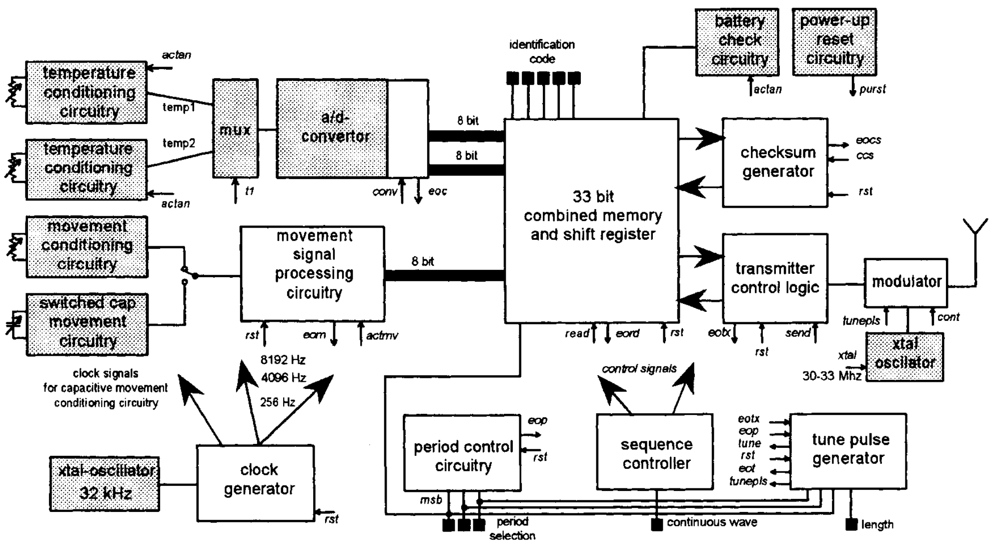

Fig. 1. The block diagram of the CMOS sensor interface chip.

long tuning pulse with an adjustable length (*length*), which allows the receiver station to lock in optimally into the transmitted frequency. A last control feature is the possibility to transmit a continuous carrier signal (*continuous wave*). This allows the fine tuning of the receiver station during start-up.

The period control circuitry controls the time between consecutive transmissions which is user adjustable. All internal clock signals are provided for by the 32-kHz low-power (16 μA @ 3 V) crystal clock generator. A crystal oscillator is preferred because of its low-power consumption and its high stability. The latter is needed, because the clock oscillator directly controls all timing functions, as well as the baud rate of the transmitted data.

The data input to the memory comes from different sources: the A/D-converter, the movement processing circuitry, the battery check circuitry, the checksum generator, and the user defined information.

The A/D-converter is the link between the shift register and the temperature measuring circuits. The input for these two independent channels is derived from two sensors, in this case, two thermistors. The analog output signals are multiplexed and one after the other presented to the A/D-converter, which digitizes the two analog measurements into 2 bytes of information.

The third information byte is produced by one of the movement channels and its processing circuitry, which is explained below.

Besides the 5-bit identification code, and some extra control bits, a battery check bit representing the battery condition and the checksum bit are clocked into the memory.

Once all the data are loaded into the memory, it is put in its second mode for cyclic shift operation. As a first action, a start bit is added and all data bits are shifted through the checksum generator to count the number of ones and to set the checksum bit accordingly. A second action consists of adding an 8-bit-wide start pulse preceding the 33 bits of information as well as an 8-bit-wide separation unit following the data bit stream. Finally, the data are transmitted four times by shifting the register cyclically. All these tasks are performed by the transmitter control unit, which also encodes the bits just before transmission according to the Manchester encoding technique to secure an even more reliable data transfer. The transmitter control unit sends the encoded bit train on to the AM on-off keying modulator where it is multiplied by the high frequency carrier in the 30 to 33 MHz band. This carrier frequency is derived from the on-chip crystal oscillator.

The operation of the entire system is supervised by the sequence controller, which makes sure that every event takes place at the proper time and in the right sequence, using the correct settings. The control logic is formed by a self-timed circuitry, often used in MOS logic because of its performance and component efficiency [3]. The essence of the control mechanism for a self-timed system consists of two signals and one state variable. The first signal is an input and acts to initiate the computation (GO). The second signal is an output and signals the completion of the computation (DONE). This signal acts often as the "GO" signal for the next logic block. A latch stores the information on whether the logic is inactive or active. If active, it passes the basic control clock signal used to time and synchronize all major events. The GO-Compute-DONE cycle is extended with a reset function, that is GO-Compute-DONE-RESET.

IV. Sensor Interfaces

A. The Temperature Channels

Two independent low-power (50 μA @ 3 V) temperature channels are implemented. This allows measurement at two different implantation sites, in order to obtain information

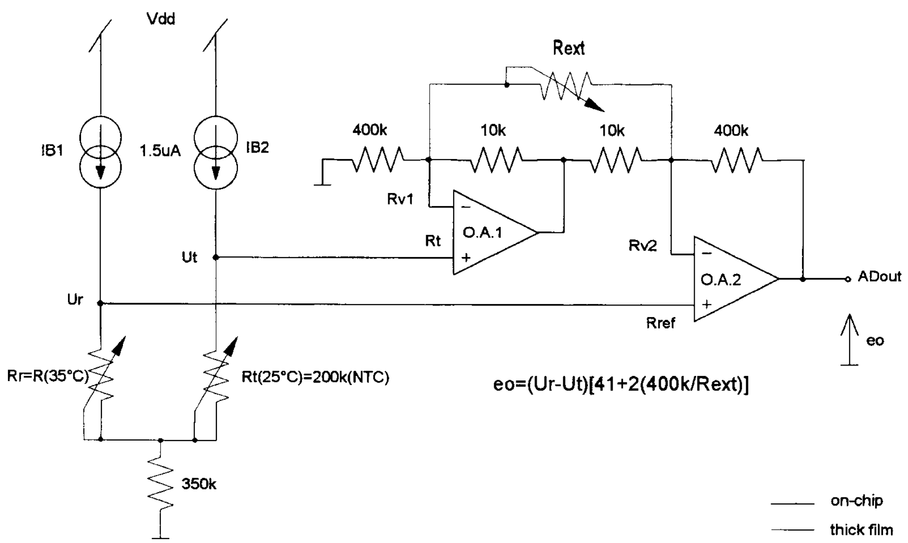

Fig. 2. The instrumentation amplifier for the temperature channels.

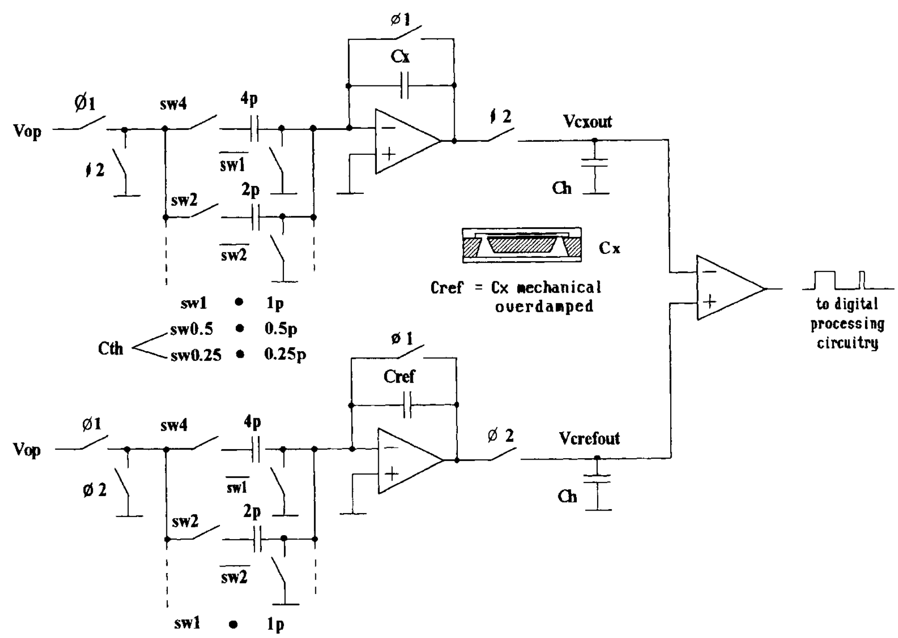

Fig. 3. The circuit diagram of the switched capacitor circuit.

on the thermal impedance of the tissue surrounding the implanted device. One channel can also be used to calibrate the other. Each channel is built around a two-opamp based instrumentation amplifier (Fig. 2), and can be adjusted in range and accuracy. To reduce the power consumption to a strict minimum, these channels are only activated during the A/D-conversion (about 4 ms).

The voltage across the thermistor R_t and the voltage across a reference resistor R_r, both generated by a bias current of $1.5\,\mu$A (IB_1 and IB_2), serve as inputs for the two opamp-based instrumentation amplifier. The reference resistor R_r is trimmed to the value of the thermistor at the minimum temperature value. The gain of the instrumentation amplifier, directly determining the accuracy and the range of the temperature measurements, is easily adjustable by a single external resistor R_{ext}.

B. The Activity Channels

1) The piezoresistive accelerometer circuit: One of both movement channels is an analog conditioning circuit for a

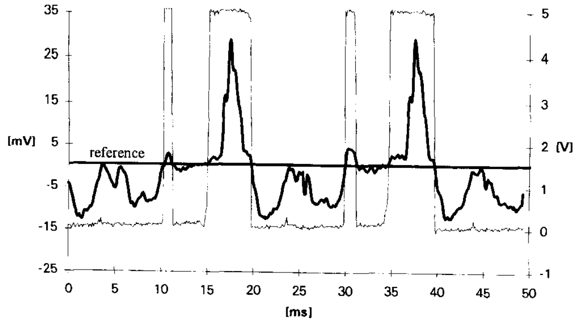

Fig. 4. The activity processing algorithm.

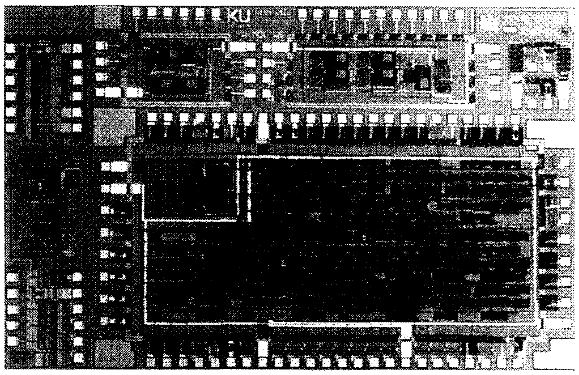

Fig. 5(a). Microphotograph of the CMOS sensor interface chip (4.7 × 7.1 mm^2).

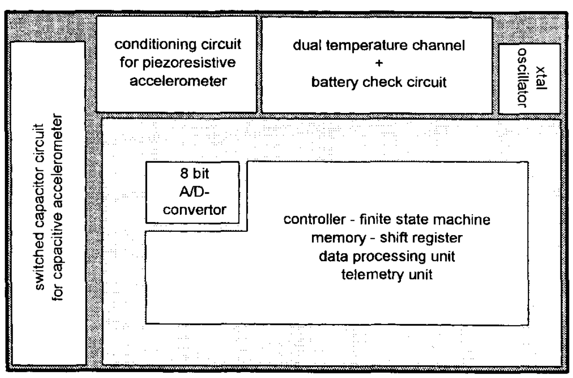

Fig. 5(b). The location of the major IC modules.

commercially piezoresistive accelerometer (IC Sensors 3021-005). This accelerometer has the basic Wheatstone-bridge configuration. Two of its terminals are connected to the inputs of a high impedance instrumentation amplifier with an internally generated ground reference of 1.5 V and a fixed amplification factor. The output signal is referred to the ground level and has a maximum signal frequency of 50 Hz for the given application. The mean current consumption is $380\,\mu$A @ 3 V, of which most is consumed by the piezoresistive accelerometer.

2) The switched-capacitor circuit: The second activity channel contains the interfacing circuitry for a subminiature ($1\,\mathrm{mm}^3$) capacitive accelerometer, which is under development at ESAT-MICAS [4]. The qualities of such a highly miniaturized capacitive sensor can only be fully utilized when the appropriate conditioning circuitry based on switched capacitor techniques is incorporated (Fig. 3). It performs conversion of the small sensing capacitance (1 pF) into a noise-insensitive output signal. This circuit is designed to suppress all negative effects of parasitic capacitors, leakage resistors and electrostatic forces. It is mainly optimized towards low-power consumption ($15\,\mu$A @ 3 V) and a high PSRR.

The analog activity signal is given by $V_{\mathrm{cxout}} = V_{op} * C_{th}/C_x$. To filter out the dc-component of the capacitive sensor, which is related to the position of the sensor (and the animal) at rest, an identical, but mechanically overdamped capacitive sensor C_{ref} is used to generate a threshold V_{crefout} with which to compare the activity signal V_{cxout}. The analog sensitivity of the circuit can be defined by controlling the switches SW0.25 to SW4, and hence the amplification factor of the stage.

3) The movement processing algorithm: Unlike the temperature signals, the frequency contents of the movement signal are quite high (50 Hz). Where temperature is only sampled just before transmission of the data, this method is clearly insufficient for sampling activity. However, the sampling of activity results in a massive amount of data to be transmitted. Therefore the activity data are processed before transmission to reduce the amount of data and to filter out the relevant information.

The processing algorithm, as recorded in Fig. 4, is embedded in the logic circuits of the chip. For the given application, the degree of activity, rather than the exact value of the amplitude of the signal versus time is relevant. In fact, one is merely interested in a relative expression for the physical activity during the chosen monitoring interval. Therefore, the analog output signal, derived from one of the two above-described movement channels, is compared with an adjustable dc reference value. The time during which the output of this comparator remains high, and is measured by the digital processing circuitry and related to the overall monitoring period (ranging from 1 to 512 s). This eventually results in only one byte of information representing the percentage of the time during which the animal had a predefined degree of activity.

V. Conclusion

In biomedical research a great need for multi-purpose, reliable, and possibly implantable telemetric tools exists. Using sensor inputs such devices allow the gathering of information on physiological parameters without restraining or stressing their subjects, on an automated basis.

For this purpose, a versatile implantable and 4-channel telemetry data-acquisition unit is implemented in a 2-μm n-well CMOS process. The dimensions of this single-chip implementation are $4.7 \times 7.1\,\mathrm{mm}^2$. A microphotograph of this dedicated integrated circuit is shown in Fig. 5(a). The location of the different IC modules is indicated in Fig. 5(b).

Special merits of the implemented system are its mixed-signal design, low-supply voltage (3 V), low-power consumption, small size, flexibility and capability of processing data.

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