A 10-Bit Pipelined Switched-Current A/D Converter

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Abstract—**A modified RSD algorithm has been implemented in a switched-current pipelined A/D converter. The offset insensitivity of the RSD converter reduces the effect of several nonidealities proper to current copier cells. Moreover, the benefits resulting from the large tolerances inherent to the RSD algorithm and the pipelined architecture result in an improved conversion rate. Measurements on a first prototype give an integral nonlinearity error less than 0.8 LSB for 10-bit accuracy. Power dissipation is 20 mW and silicon area is 2.5 mm^2. The measured sampling rate is 550 kS/s. It is an improvement by a factor of twenty compared to known equivalent CMOS switched-current converters. It is nevertheless still well below the predicted conversion rate of 4.5 MHz, which should be obtained once this A/D converter is integrated into an analog front-end. Full compatibility with standard digital technologies makes this kind of converter attractive for low power, medium-fast converters with 10-bit accuracy.**

I. Introduction

THE interest in switched-current circuits has been underlined by many authors, in the area of sampled-data filters [1], as well as in that of A/D [2], [3] and D/A [4] converters. The so-called "current-copier cell" [5], whose basic idea, accordingly to [6], was proposed by E. A. Vittoz, offers interesting features, for it samples current regardless of the nonlinear behavior of MOS capacitances. Current-mode analog circuits using this structure are therefore compatible with standard digital processes, while voltage-oriented implementations suffer increasingly from poor capacitances.

We focus our attention in this paper on a switched-current cyclic A/D converter. Various implementations have been reported in the literature [2], [7], [8]. Generally they support the idea that the current mode approach yields small area (a few square millimeters), low power (about ten milliwatts) but nevertheless accurate (up to 14 bits) A/D converters. The main limitation, however, is a rather low conversion rate, for the time needed to compare accurately current sources becomes very large with high resolution CMOS converters (for instance, the 10-bit converter described in [2] has a sampling rate that does not exceed 25 kS/s). In this paper, we present a new type of switched-current cyclic converter that overcomes this problem partly by means of implementing the RSD algorithm [9] and partly by means of a pipelined architecture.

In Section II, the main properties of the RSD algorithm are recalled. A modification of the algorithm is proposed to cope with the unidirectional nature of current delivered by current-copier cells. Section III presents the effects of nonidealities inherent to current-copiers considering an RSD offset-insensitive architecture. The implementation of the actual converter is presented in Section IV. Experimental results and conclusions are summarized in Sections V and VI respectively.

Manuscript received December 22, 1993; revised March 28, 1994.

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IEEE Log Number 9402476.

II. The RSD Algorithm

The RSD algorithm is based on the Sweeny-Robertson-Tocher division principle [9]. It has been implemented successfully in several voltage-mode cyclic A/D converters [10]–[12]. An extensive study showing how nonidealities affect the performances of both conventional cyclic and RSD converters can be found in [10]. Insensitivity to loop offset errors and comparison errors makes this algorithm very attractive for cyclic converters. That is why we implemented it in a cyclic switched-current converter. The constraints associated with the unidirectional nature of current delivered by the current-copiers, as well as the difficulty to match two equal and opposite reference currents, however, required to modify the original algorithm as follows: after multiplication by two, the signal to be converted is sampled against two comparison levels $Ic1$ and $Ic2$ for the determination of the MSB bit $(0 < Ic1 < Ic2)$. If the signal is smaller than $Ic1$, the output code is set equal to 0 and no operation is carried out. If the signal is larger than $Ic1$ but smaller than $Ic2$, the output code is set to +1 and the reference current Ir is subtracted from the signal. Finally, when the signal is larger than $Ic2$, the output code is set equal to +2 and two times the reference, $2Ir$, is subtracted from the signal. The actual difference, called the remainder of the division, undergoes the same treatment repeatedly until the LSB is obtained.

III. The RSD Algorithm and the Performances of the Current-Copier Cell

Although insensitive to capacitance nonidealities, current-copiers are prone to problems which are related to finite output impedance, noise, leakage current, and, above all, charge injection from the switch. Detailed studies about these effects can be found in the literature [5], [13], [16]. We focus our attention in this section exclusively on the benefits resulting from the implementation of the RSD algorithm in a current-copier architecture. The simplified schematic of a typical n-type current-copier circuit used in the actual converter is shown in Fig. 1. It consists of a regulated-cascode current-copier [14], where $M1$ is the copying-transistor. The drain voltage of this transistor is controlled by means of transistors $M2$ and $M3$. The switch Ms connects the output of the copier to the gate of $M1$ in order to copy the input current. The quiescent point of the copying transistor is fixed by two dc currents II and IJ. Using a regulated-cascode

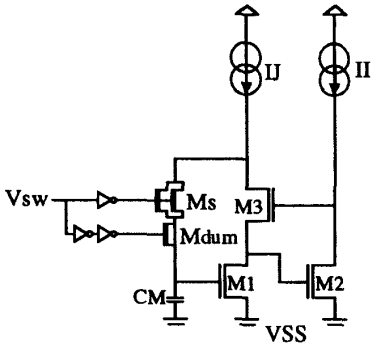

Fig. 1. Simplified schematic of n-type current copier cell.

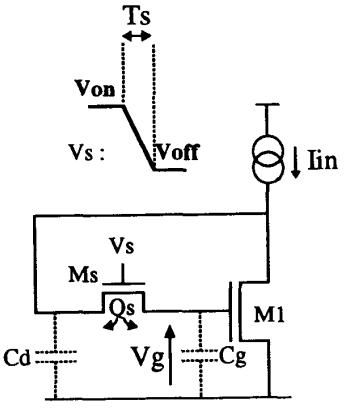

Fig. 2. Simplified diagram for charge injection calculation in current copier cells.

structure is justified by several reasons. Not only does it provide better power supply rejection comparatively to the simple cascode, but it allows keeping the copying transistor not saturated without too-severe penalty regarding output impedance. Hence the transconductance of the non-saturated transistor remains more or less constant. This keeps the drain current perturbation resulting from signal-independent gate voltage fluctuations more or less constant. Consequently, the perturbation can be assimilated to a constant offset error. Because the RSD algorithm is offset-insensitive, the linearity of the RSD converter remains unaffected. The decrease of output impedance which is the consequence of nonsaturation of $M1$ decreases the Early voltage of the regulated cascode and affects the accuracy adversely. This effect, however, is strongly attenuated for the high gain of the feedback loop around the regulated cascode. Indeed, the output impedance of the regulated cascode equals the output impedance of $M1$ multiplied by the loop gain around the cascode transistor $M3$ which usually is very high, typically 80 dB.

Charge injection from the switch is the worst non-ideality current-copiers have to cope with. This introduces a trade-off, underlined in [13], between speed and accuracy. This trade-off is alleviated in offset-insensitive circuits. Fig. 2 shows a simplified diagram of the current-copier through the switching phase. When the switch cuts off, a part α of the channel charge Qs is injected onto the gate capacitance Cg of $M1$. This produces a small perturbation $i(I)$ of the sampled current which can be expressed as:

$$i(I) = \frac{\alpha Q_s}{C_g} gm = \frac{\alpha C_S V_{GOV}}{C_g} gm$$

where:

$$V_{GOV} = V_{on} - V_g - V_T. \tag{1}$$

In this expression, gm represents the transconductance of the copying transistor, and C_s and V_{GOV} are respectively, the gate capacitance and gate voltage overdrive of the switching transistor Ms (V_{on} stands for the "on-state" gate voltage, V_T for threshold voltage and V_g for gate voltage of the copying transistor). Since the ratio C_g/gm is nothing else than the time constant of the current-copier cell [6], [13], the above mentioned trade-off between speed and accuracy is clearly outlined by (1). Hence, the faster the current copier (small C_g/gm), the higher the sensitivity to charge injection and the poorer the accuracy. However, the perturbation represented by (1) can always be expressed as the sum of two terms, one is a signal dependent current i_{rsd}, and the other is a constant current offset i_{mean}. Only the first component must be considered; the second hasn't any effect at all on the linearity of the RSD converter. It can be easily shown that, for a non-saturated copying transistor, the first term can be rewritten has:

$$|i_{rsd}|(\text{in percent}) < \frac{MAX(i_{rsd})}{I_{\max} - I_{\min}} = \frac{\alpha C_s}{2C_g} \tag{2}$$

where (I max - I min) represents the input dynamic range of the current copier cell. Hence, the signal-dependent perturbation is a function only of the ratio of gate (C_g) and switch (C_s) capacitances belonging to the copying transistor as well as of the charge distribution coefficient α of the switch [16]. Neither V_{GOV} nor gm influence this perturbation anymore. The accuracy-speed trade-off thus is alleviated, and we gain a degree of freedom which enables us to minimize the signal-dependent perturbation term i_{rsd}.

IV. The RSD Switched-Current Cyclic Converter Architecture

As mentioned earlier, measures were taken in order to improve the conversion rate of the switched-current cyclic converter. The first is, of course, the automatic compensation of incorrect decisions taken during bit evaluation thanks to the RSD algorithm. This alleviates, to some extent, the relative slowness of high-accuracy switched-current converters, for it does not require a lot of time in order to achieve accurate discrimination of currents. The price paid therefore, is of course the double comparison opposed to the usual single. But this turns out to be an advantage more than a penalty. Indeed, the tolerances on the RSD algorithm comparison levels may reach as much as 25% of the total dynamic range while those required with the conventional cyclic algorithm must be kept either smaller or equal to a half LSB. Consequently, the

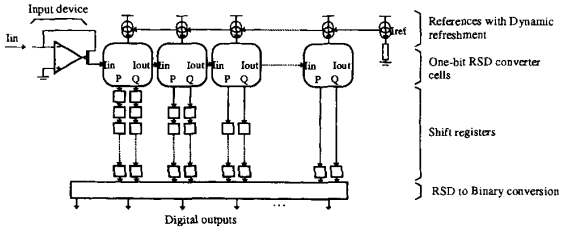

Fig. 3. Schematic diagram of the pipelined RSD A/D converter.

RSD comparator can be very simple, yet fast, compared to the offset compensated comparator required in high accuracy conventional cyclic converters.

Another measure taken in order to improve speed is the choice of a pipelined implementation which makes the overall conversion time equal to a single cycle time. The resulting architecture of the converter is presented in Fig. 3. It consists of a set of 1-bit RSD cells in cascade. The analog output of each cell serves as an input signal for the next cell, while digital data collected along cells are delayed to rebuild the proper RSD codes corresponding to the samples. In order to avoid the conversion from RSD to binary data off-chip, a simple digital transformation is achieved on-chip. This in the same time reduces the number of output pins ($n + 1$ binary outputs instead of $2n$ bits for the corresponding RSD code).

So far no pipelined implementations of CMOS switched-current converters have been reported. The matching problem of the reference currents distributed to adjacent cells may explain this. In order to cope with the problem, we investigated the suitability of dynamic refreshment of all the current-copying cells feeding the reference current converters cells. This is achieved under control of a token ring logic.

The simplified schematic diagram of a single converter cell is illustrated in Fig. 4. It consists of two n-type current-copiers $CN1, CN2$ and one p-type buffer-copier $CP1$. The two comparison levels are represented by the two currents $Ic1$ and $Ic2$. Three phases are needed to perform one conversion cycle. During the first phase $PH1$, the input current from the p-type current-copier is sampled by $CN1$. During the second phase $PH2$, the same input current is sampled by $CN2$, while the current stored in $CN1$ is compared with the threshold levels $Ic1$ and $Ic2$ in order to generate the bits P and Q which map the RSD code accordingly to the data in Fig. 4. The two bits monitor the reference currents $Ir1$ and $Ir2$ during the last phase $PH3$, when the new partial remainder is calculated and stored into the next p-type buffer in view of a new conversion cycle.

As stated before, regulated cascode circuits are used for n and p-type current-copier cells. The electrical characteristics of these cells are summarized in Table I with emphasis on speed. Simulations of the complete current copier cell predict that the time to reach 10-bit accuracy can be smaller than 70 ns. A full conversion cycle thus should take more or less 210 ns (three phases per conversion cycle). This corresponds to a sampling rate of 4.5 MHz. In practice, however, the actual conversion rate may be overruled by unavoidable additional

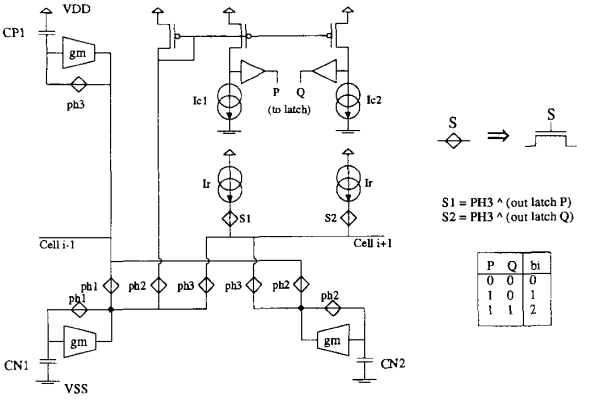

Fig. 4. Simplified diagram of 1-bit A/D converter cell.

TABLE I
ELECTRICAL FEATURES OF CURRENT COPIER CELLS AND REFERENCES

Current copier cells	Reference currents
$IJ = 90\,\mu$A	$Ir = 50\,\mu$A
$\Pi = 5\,\mu$A	$IM = 45\,\mu$A
$C_g = 850$ fF	$Iad = 5\,\mu$A
$C_g/gm = 7$ ns	gm (cop. trans.) $= 20\,\mu$A/V
$Z_{\text{out}} \approx 550\,\text{M}\Omega$	$Z_{\text{out}} > \text{G}\Omega$

parasitic capacitance associated with the input node so that the sampling rate is substantially reduced. This point is addressed in Section V.

The reference current source uses an architecture similar to that presented in [4]: a static current mirror delivers the main part of the reference current I_M, while a small additional current I_{ad} is provided by means of an additional current copier. The reference is periodically refreshed so that the total current $I_M + I_{ad} = Ir$. As shown in Table I, I_{ad} represents only 10% of the total current. Moreover, the transconductance of the actual current copier is small. Hence, charge injection effects, as well as noise and leakage current of the copying transistor affect only 10% of the global current. The efficiency of this technique was demonstrated in [4], where it was implemented to match current sources for a 16-bit D/A converter.

Since the comparator's accuracy does not affect the linearity of the RSD converter, it is simply realized by means of strobed cross-coupled inverters, making silicon area and dissipated power very small. Moreover, all transistors are minimal size.

RSD to binary conversion is implemented after delaying the digital output from each cell. In accordance with the truth table presented in Fig. 4, the conversion is achieved simply by binary addition of the two P and Q bits of each RSD cell. A cascade of full adders is used therefore.

V. EXPERIMENTAL RESULTS

The circuit was implemented in a standard 2.4 μm process. The layout is fully-compatible with digital processes (no use is made of resistors nor poly II masks). The prototype dissipates 20 mW with a 5-V power supply. Separate analog and digital power supply lines are used. The active area is 2.5 mm^2. All reference currents are fixed at 50 μA. Reference

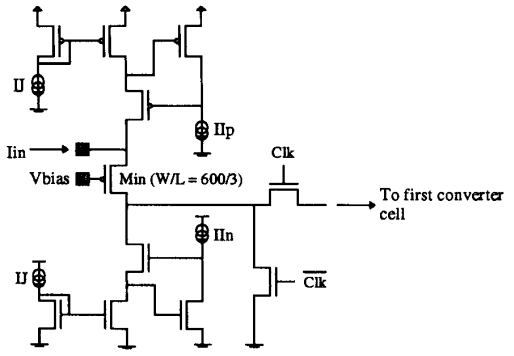

Fig. 5. Schematic of input device ($IJ = 5\,\mu\text{A}, gm(\text{Min}) = 250\,\mu\text{A/V}$).

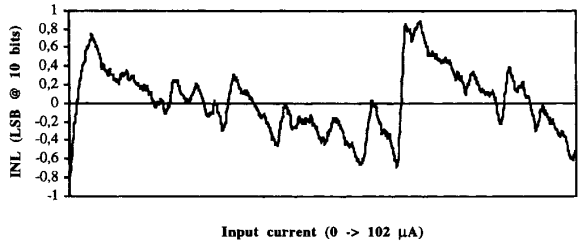

Fig. 6. Integral non-linearity at 550 Ks/s.

TABLE II
COMPARISON OF CMOS SWITCHED-CURRENT A/D CONVERTERS USING CYCLIC ALGORITHMS

	Effect. Res. [bits]	Fs [kHz]	Area[2]	Power [mW]
[8]	14	5.7	1	2.5
[2]	10	25	2.5	3.5
[7]*	9	83	0.7**	15
RSD	10	550(4500***)	2.5	20

*extrapolated values
**1.2μ technology (others 2.5 or 3 μ technology)
*** simulated value without input pole.

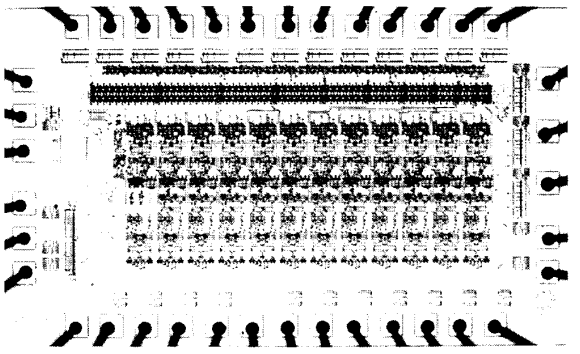

Fig. 7. Microphotograph of the chip.

and polarization currents are externally adjustable. In current-mode circuits, the input node impedance should be kept always as small as possible in order to avoid unwanted poles. In the present converter, the input node, however, is the sampling node of the first current-copier. Any parallel parasitic capacitance thus slows down substantially the maximum sampling rate. If for instance, the input node is connected directly to an off-chip current source, the large capacitance associated with the input pad impairs considerably the maximum sampling rate. Once the A/D converter is integrated within a complete analog front-end however, the converter senses only the internal on-chip capacitances and the problem is less severe. In order to alleviate the testing problem, we introduced a high-gm common-gate transistor in series with the input, as shown in Fig. 5, in order to reduce the resistance of the input pad as much as possible. The measured maximal sampling rate did not exceed 550 kS/s. With an input current conveyor or a voltage-to-current converter, we should have obtained a sampling rate near the above-predicted 4.5-MHz clock rate.

The integral non-linearity error curve is plotted in Fig. 6, considering the above-mentioned 550 kS/s sampling rate. The maximal INL error observed reaches ± 0.8 LSB with a 10-bit resolution.

Table II compares the performances of this RSD current-mode A/D converter with those of other known CMOS switched-current converters. Table II shows that the conversion rate is increased by a factor of more than twenty compared to converters with the same accuracy, notwithstanding the lower sampling rate mentioned above. These performances were reached with little power and area increases. We found that the actual 10-bit accuracy was determined mainly by poor design of a dummy switch compensation in the copiers storing the references.

A microphotograph of the chip is shown in Fig. 7.

VI. CONCLUSION

A modified RSD algorithm has been implemented in a switched-current pipelined A/D converter. The offset insensitivity of the RSD converter reduces the effect of several nonidealities proper to current copier cells. Moreover, the benefits resulting from the large tolerances inherent to the RSD algorithm and the pipelined architecture, result in an improved conversion rate. Measurements show that a factor of twenty is obtained compared to known equivalent CMOS switched-current converters. This sampling rate is still well below the predicted conversion rate of 4.5 MHz, which should have been obtained if this A/D converter were integrated into an analog front-end. Full compatibility with standard digital technologies makes this kind of converter attractive for low power, medium-fast converters with 10-bit accuracy.

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