An Analog CMOS Front-End for a D2-MAC TV Decoder

W. Redman-White, M. Bracey, J. Tijou, B. Murray, and C. Hopwood

Abstract—**This paper describes the analog front-end of a fully integrated CMOS TV decoder, suitable for the reception of terrestrial as well as satellite signals, based on the D2-MAC transmission system. While the video reconstruction is undertaken using DSP, the front-end subsystem incorporates many linear and non-linear analog functions, including amplitude measuring, AGC, clamping, data slicing, clock recovery and of course, A/D conversion for the MAC signal processing.**

The chip is fabricated in 1-μ CMOS, and operates from a single 5-V supply.

I. Introduction

THE Multiplexed Analog Component (MAC) family of TV transmission systems has been developed to avoid the well-known problems of the familiar NTSC/PAL systems, with particular emphasis on satellite broadcasting. Time division (as opposed to frequency division) multiplexing is used to separate the luma and chroma components of the composite video. The video signal components are compressed in time; this requires that the signals be expanded and overlaid, a job best done by a DSP system. Given the relative complexity of the digital circuitry needed, there is a clear requirement to include the analog pre-processing on the same die, using a "digital" CMOS process [1]. Similar approaches have been followed for other modulation schemes [2].

The transmitted D2-MAC waveform (Fig. 1) looks very different from the familiar NTSC/PAL signal. On each line there is a burst of high-speed data (approximately 5-MHz bandwidth duobinary encoded) followed by a clamp period setting the reference grey level. This data burst also contains the audio signal. The chroma and luma signals follow sequentially in time-compressed form. Further, there is no familiar sync pulse; instead, synchronization is accomplished by means of recognition of an alignment word in the transmitted data. Consequently, the data must be correctly extracted before the decoder can be properly synchronized and begin video processing. An additional complication is that signals originating from satellite systems will often have superimposed a triangular waveform of several hundred millivolts amplitude, intended to disperse the signal energy across the spectrum used by the transponder.

This paper describes the analog front-end circuitry of a fully integrated D2-MAC decoder, which performs the signal conditioning and pre-processing of the signal from the IF section of the receiver, as required by the main DSP section. The tasks of the front-end are thus:

1) Apply AGC to the input to account for receiver sensitivity variations.
2) Digitize the luma and chroma for the main DSP block.
3) Clamp the video DC level at a reference grey level.
4) Slice the data signal and recover the data for video line and master clock synchronization.

The front end is broadly divisible into two parts, the video path and the data path; since the main connection between these parts is in the form of timing signals, they will be treated independently. In this application, there are separate inputs to the chip, fed by specific passive low-pass filter blocks.

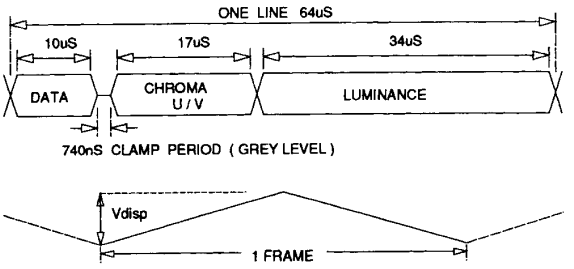

Fig. 1. D2-MAC signal structure, with dispersal signal.

II. Video Path and AGC

This section is the interface between the receiver and the DSP-based decoding circuitry, and, as such, has a critical influence on the quality of the picture produced. At the heart of the video path subsystem is an 8-bit flash A/D converter [3], operating at 20.25 MHz. Given the difficulties in realizing true 8-bit performance at video frequencies in a mixed-signal CMOS, the goal for the design of the surrounding analog circuitry was to preserve the video quantization at close to the full range of the A/D for optimum picture quality, and not to use part of the dynamic range for other functions.

To maintain accurate video levels in the presence of receiver gain tolerances and signal variations, an automatic gain control (AGC) is required with a ± 3 dB range. Variable gain video amplifiers in CMOS are not easy to realize with the signal range needed for the A/D. In this design, smooth AGC over this limited range is achieved without incurring excessive distortion by varying the reference current to the A/D ladder (Fig. 2). The converter design is sufficiently robust that the demanded performance is still realized with these variations in reference levels.

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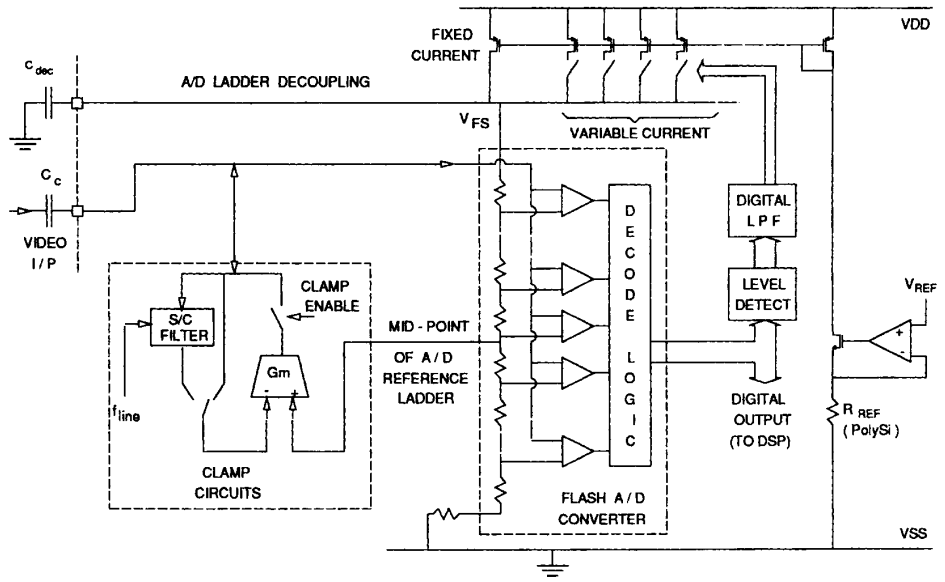

Fig. 2. Video signal path structure, showing AGC system. (Clamp circuits in terrestrial mode).

For predictable AGC operation, an accurate measurement of the video signal amplitude must be made, and this is done in the digital domain to take account of the "gain" through the A/D converter itself. Line 624 in each D2MAC frame is a defined reference signal, with mid grey, peak white, and peak black levels transmitted sequentially after the data burst (Fig. 3). The digital values corresponding to these levels are first low-pass filtered and then compared with the nominal values to yield a correction value. This, in turn, is used to set the A/D reference ladder current by means of a simple current output D/A (Fig. 2). A fixed current source in parallel with this defines the maximum "gain" set by the A/D. The current sources feeding the A/D ladder are controlled by a reference generator which uses a polysilicon resistor to define a current from a set reference voltage. Hence, since the A/D ladder is also fabricated from the same polysilicon layer, the "gain" of the A/D can be accurately set in absolute voltage terms. An external decoupling capacitor serves to smooth current increments to the point of invisibility on the screen, as well as to reduce HF noise on the A/D ladder.

Fig. 4 shows the measured voltage at the top of the A/D reference ladder as the incoming video signal amplitude is changed by a step function. As the video signal envelope increases, so the A/D reference voltage is raised, reducing the analog voltage per step, and hence the signal path "gain."

III. Video Path Clamping

The clamping function of a MAC decoder is of particular importance, since the analog reference level is used to define both the mid-scale luminance and the zero chrominance value. Hence, errors in this function lead to both brightness changes and color tinting of neutral images.

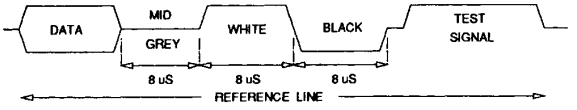

Fig. 3. Reference levels in line 624.

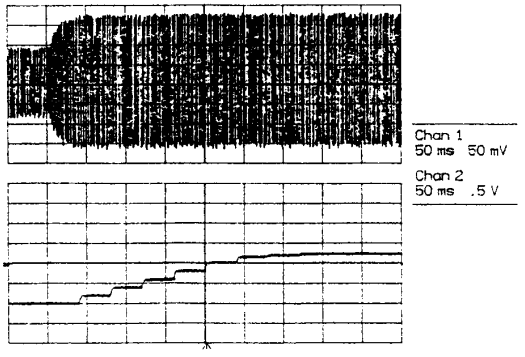

Fig. 4. Measured response of AGC to step in video envelope. Upper trace, video envelope, lower trace, voltage at top of A/D reference ladder.

The grey level reference voltage on the chip is defined by the midpoint of the A/D resistor ladder. Clamping of terrestrial video signals to this value when in sync is relatively straightforward. A transconductor is attached to the input for a defined duration during the clamp period, which compares this value with the reference voltage. An error current then charges the coupling capacitor with a (long) time-constant set by the transconductance. When the signal originates from a satellite system, this approach is not satisfactory. In this case, a simple

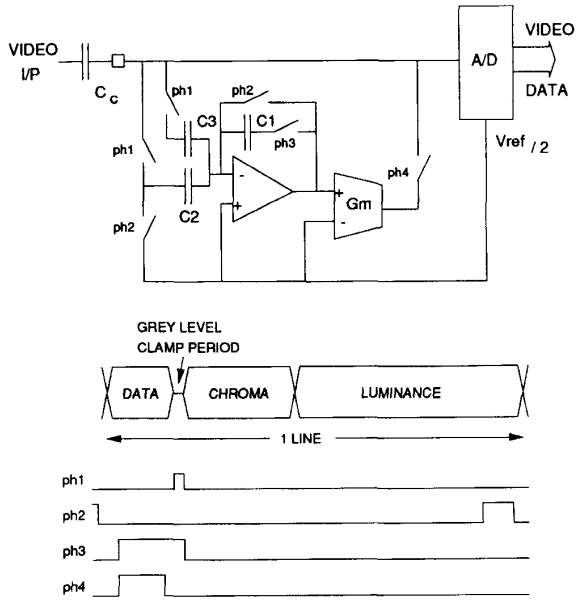

Fig. 5. Switched capacitor clamp circuit for satellite signals.

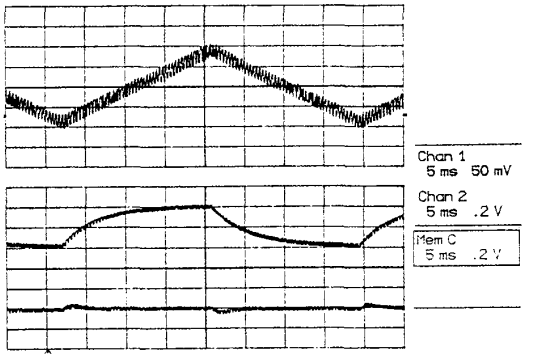

Fig. 6. Measured clamp circuit responses. Upper trace, free running triangle test signal applied via coupling capacitor, center trace, response at input pin of single pole clamp showing line-to-line offset, lower trace, response of two pole SC clamp circuit.

switched capacitor circuit clocked at line rate (Fig. 5) is used to modify the basic clamp response to a higher frequency second-order high-pass function, preventing the dispersal signal from becoming visible as flicker on the screen. Auto-zero techniques are used to ensure minimum DC offset.

The behavior of these two clamp circuits can be best seen by applying a triangle input of the same magnitude of the dispersal signal, but without video information. The clamp circuits will then free run, sampling at the nominal line rate in the absence of sync information. Fig. 6 shows the measured voltages on either side of the input coupling capacitor for both clamps. The line-to-line offset left by the simple single pole clamp is visible in the center trace, while the switched capacitor circuit reduces the effects of the triangle signal to negligible levels, and the small settling transient is not displayed.

IV. Data Slicing

The efficient recovery of the data in the MAC signal is essential to the basic functionality of the decoder. The data must be extracted *before* line lock is acquired, since the sync information is contained within it. Hence the two slicing levels for the duobinary signal must be obtained quickly at the start of a line using run-in bits even in the presence of an added dispersal waveform.

During the data burst, the two peak detectors act as "ideal diodes," one clamping the negative peaks to an internal reference voltage, and the other determining the positive data peaks with respect to this. These two reference levels are then used to drive a potentiometer chain, which sets the slicing levels of two fast comparators to detect the duobinary data. Fig. 7 shows the scheme. Out of sync, a more approximate estimate of slicing levels is obtained from the complete video waveform, but this is sufficiently accurate to gain line lock.

Given the demands of very fast level detection with the 5 Mbit/s data, the peak detectors are required to have high bandwidth and good settling behavior. A form of unidirectional transconductor is used, based on a folded cascode structure (Fig. 8). Unlike a conventional opamp, the folding source is made equal to half the tail current of the differential pair. Hence, in balance no current flows in the output cascode to the (external) storage capacitor. Thus, for signals in one sense, the charge on the capacitor remains fixed; for the other sense, the capacitor is charged by a current up to the value of the tail current, with a defined time constant set for noise considerations. For moderate input–output differences, the circuit's g_m is just that of the differential pair. This arrangement provides adequate dc gain to keep offsets negligible while giving near-ideal single pole settling under active conditions. A small negative bleed current provides a slow decay path.

V. Data and Timing Recovery

The raw outputs of the slicing comparators are first converted to binary with an OR gate. Latching of the data for maximum noise rejection should be performed at the midpoint of the symbol period. To enable the timing recovery PLL to provide clock edges at this optimum point, the data transitions are detected (Fig. 7). For this, the data stream is passed to an EXOR gate, both directly and also through a monostable delay. This delay must be accurately set to half the symbol period for the best eye height. The value is set on-chip without trimming by means of an adaptive delay circuit; the master clock period can be used as a time reference for this, since even out of lock, the error in the VCXO frequency can only be of the order of 0.02%.

The master oscillator runs at twice the data rate and delivers edges skewed by half the symbol period (i.e., I and Q outputs) via a twisted ring counter. The data transition signals and the data-edge synchronous clock output are combined in a conventional PLL. To allow easy inclusion of the varicap circuitry, a Colpitts VCXO design is used (similar to [4]) with an AGC circuit to set a low operating level for the crystal.

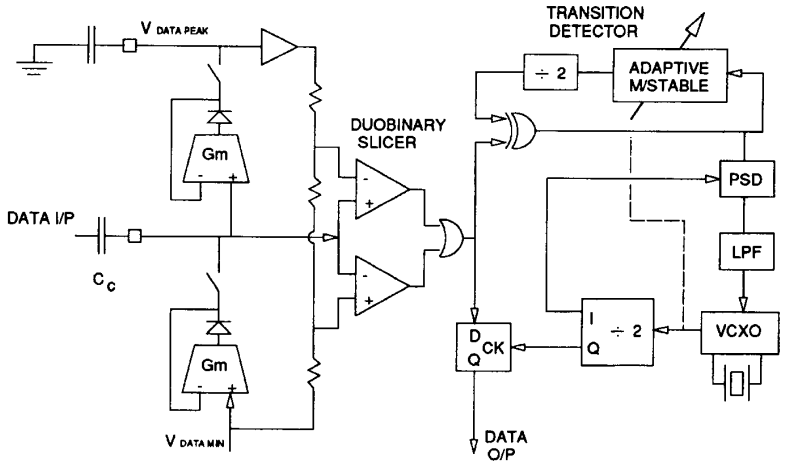

Fig. 7. Data signal path slicing and timing recovery structure.

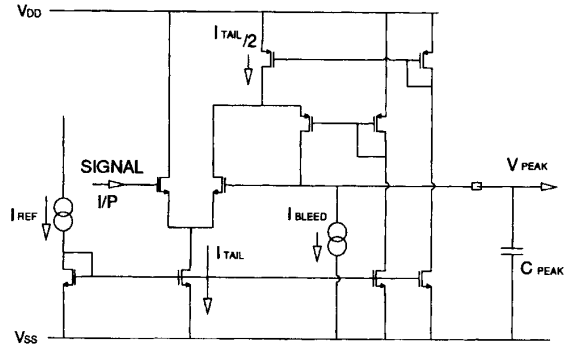

Fig. 8. Peak detector circuit.

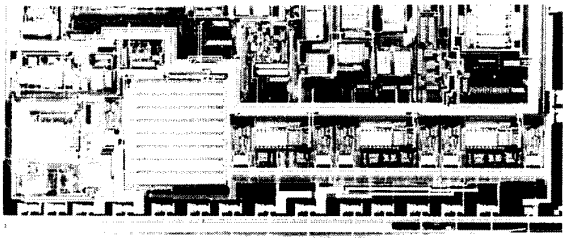

Fig. 9. Microphotograph of analog section of the decoder IC.

Care is needed in the biasing of the logic level slicer for this oscillator as the twisted ring counter requires an even mark: space ratio for accurate I and Q outputs.

VI. Results and Conclusions

As in any large IC incorporating both digital and high-performance analog sections, considerable care is needed in the execution of the final design, with floorplanning and layout critical. The analog front-end occupies one edge of the decoder; supplies are separated and the section is carefully shielded in the usual ways. On-chip D/A converters and buffers [5] provide a direct output at 75-Ω impedance. Test bus access allows the signal at the output of the A/D to be observed in the digital domain, or routed to the D/A converters. Fig. 9 is a microphotograph of the subsystem: the front-end is on the left with the SC circuit clear; to the right are the YUV output buffers. The circuitry is fabricated in 1-μm CMOS and occupies approximately 7 mm^2.

Results have been presented for the subsystems. The data path circuits can achieve lock quickly, with the adaptive edge detection adding negligible time to the acquisition of signals. The AGC is smooth in operation without measurable degradation of the A/D performance, and creates no visible artifacts. The clamping circuits provide accurate reference grey levels without, as required. Results of the overall performance are clearly less easy to present in print, since subjective picture quality and freedom from annoying screen artifacts are most important, but the system fully meets these demands. This subsystem has replaced an existing separate bipolar analog IC and A/D converter, providing a fully integrated decoder in CMOS with a minimum of external components.

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