New Efficient Designs for XOR and XNOR Functions on the Transistor Level

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***Abstract*— Two new methods are proposed to implement the exclusive-OR and exclusive-NOR functions on the transistor level. The first method uses non-complementary signal inputs and the least number of transistors. The other one improves the performance of the prior method but two more transistors are utilized. The latter uses the same number of transistors as [1] but with more driving capability additionally. Both of them have been fully simulated by HSPICE on a SUN SPARC 2 workstation.**

***Index Terms*—Threshold voltage, XOR, XNOR, CMOS circuit design, simulation.**

I. Introduction

THE exclusive-OR (XOR) and exclusive-NOR (XNOR) functions are the fundamental units in various circuits, such as comparator, parity checker, full adder, and so on. If these functions are implemented on the logic gate level, by elementary gates, AND, OR, and NOT, the redundancy will be very large. As the advancing of VLSI technology, MOS circuits have been widely applied to many fields. There are two kinds of MOS, i.e., the NMOS and the PMOS. It is well-known that the NMOS transistor can transmit the signal "LO" (or "0") completely, but it has poor performance on transmitting the signal "HIGH" (or "1"). If one takes an NMOS transistor to implement a switch device, a control signal is added to the gate terminal, and sets one end to the signal "HIGH," the other end will drop voltage V_{NT}, where V_{NT} is the threshold voltage of NMOS. To the contrary, the PMOS transistor can pass a signal "HIGH" fully but handles badly on a signal "LO." As a switch device, if a signal "LO" appears on the source end of the PMOS transistor, the destination end will not sink to signal "LO;" it will keep on a higher voltage $|V_{PT}|$, the threshold voltage of PMOS, than expected.

While the amount of fanout is small, the poor signal level can still drive other circuits correctly. If the amount of fanout is no longer small or the poor signal has to pass through several improper transistors, i.e., transmit signal "HI" by NMOS or pass signal "LO" by PMOS, then the poor signal level may degenerate by and by and no longer guarantee working right. In order to overcome the individual defect, combining an NMOS and a PMOS to carry on a transmission gate can pass both signal "HIGH" and signal "LO" with excellent performance.

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TABLE I
THE FUNCTION OF XOR AND XNOR

A	B	A XOR B	A XNO R
0	0	0	1
0	1	1	0
1	0	1	0
1	1	0	1

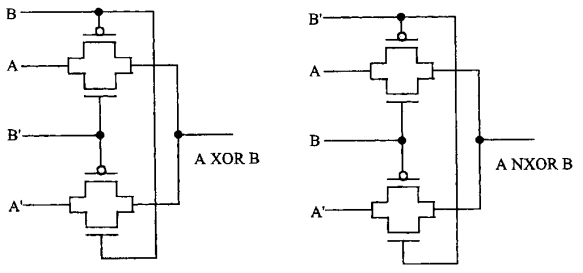


Fig. 1. The XOR and XNOR functions implemented by transmission gates.

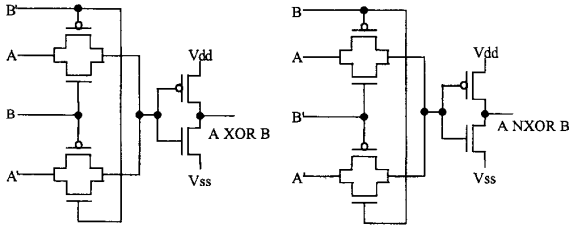


Fig. 2. The XOR and XNOR functions implemented by transmission gates with driving output.

Although a CMOS transmission gate has better quality, there is a main drawback in a CMOS transmission gate, i.e., it needs complementary signal values to control gates of PMOS and NMOS, respectively. Sometimes the complementary inputs are troublesome under some situations. Usually, we need an inverter to fit the request of complementary input. It is wasteful! By way of rearranging the configuration of PMOS and NMOS transistors, this drawback can be removed.

Conventionally, a logical circuit can be realized by canonical CMOS transistors. As usual, the direct conversion from logical gates needs many more transistors. A conversion based on gate level, not on transistor level, will create too much

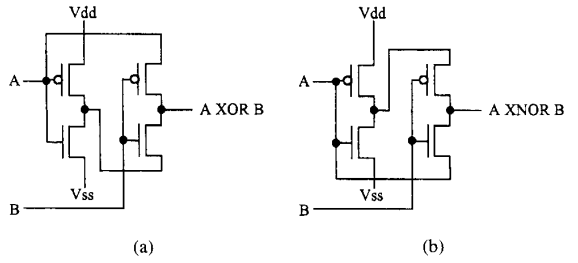


Fig. 3. (a) Inverter-based XOR structure. (b) Inverter-based XNOR structure.

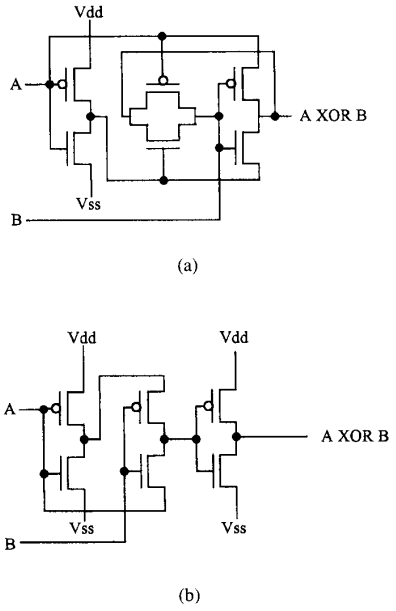


Fig. 4. (a) An improved version of exclusive-OR structure. (b) Another improved version of exclusive-OR structure.

redundancy in the circuit. With the transmission gate theory [2], the high impendence state is available, the less transistors can be used on the transistor level. In this paper, the novel designs for XOR and XNOR functions will be developed and verified. The performances are better than the past designs [1] and proved after a careful analysis of simulation.

The remaining portion of this paper is organized as follows. We introduce the previous designs of XOR and XNOR functions in Section II. In Section III, we represent our new designs for XOR and XNOR structures. To verify the performances of the proposed methods, fully realistic simulations using HSPICE are demonstrated in Section IV. Finally, we make our conclusion in Section V.

II. The Previous Works

The exclusive-OR and exclusive-NOR functions are shown in Table I. Assume the input signals are A and B, then the exclusive-OR of A and B, denoted as $A \oplus B$, is logically equivalent to $A'B + AB'$; and the exclusive-NOR of A and

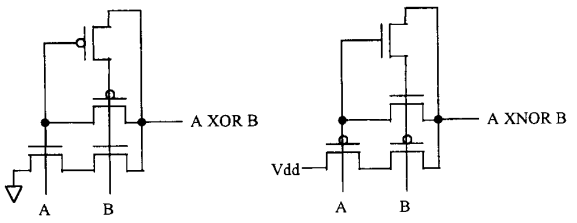


Fig. 5. The proposed XOR and XNOR structures.

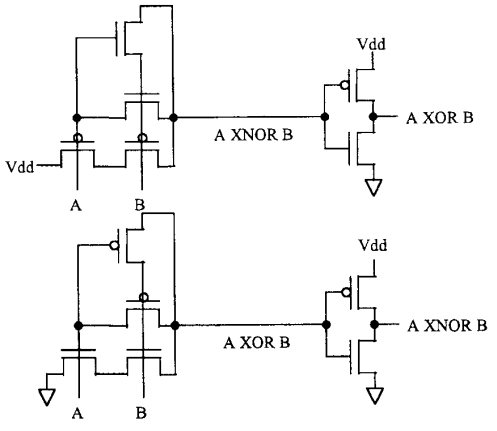


Fig. 6. The proposed XOR and XNOR structures with driving output.

B, denoted as $A \odot B$, is logically equivalent to $AB + A'B'$. There are several methods that can implement these functions.

1. Based on the transmission gate theory, the realized circuit using transmission gates is shown in Fig. 1. This structure needs only 4 transistors, but the drawbacks are the required complementary inputs and the loss of driving capability. In general, if the output signal of a circuit comes from V_{DD} or V_{SS} directly, we say this circuit has driving capability. It is well-known that a transmission gate has no driving capability. If the circuit output will drive other circuits, it does better to cascade a canonical CMOS buffer to do so. For example, if a function $f(\bullet)$ is implemented by transmission gates, then one can resemble the structure for implementing the complementary output $f(\bullet)'$ and attach a tailing inverter. Using this technique, it also has the configurations of XOR and XNOR in Fig. 1, and adds an inverter behind each case, therefore, the improved versions are illustrated in Fig. 2. In the improved versions both designs use 6 transistors to achieve the same functions as Fig. 1 and, additionally, driving outputs are present. But the complementary input problems are not resolved in the improved versions yet.

To follow, without the loss of generality, all the methods we discuss will focus on the XOR function, mainly because the XNOR structure is very similar to XOR structure symmetrically. The skill for the XOR function can be applied to the XNOR function without question.

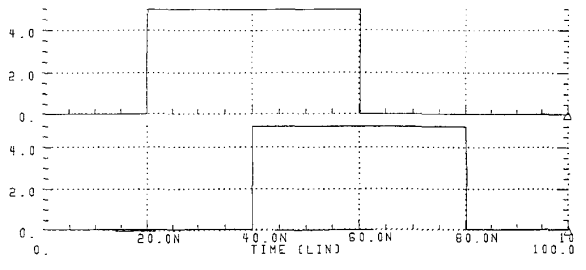


Fig. 7. The input signals A and B.

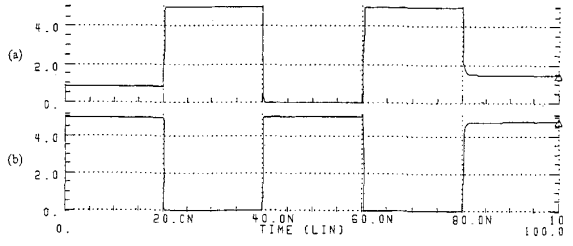


Fig. 8. (a) The output of 4–transistor XOR and (b) the 6–transistor XNOR.

2. Based on the inverter configuration, we can arrange two inverters appropriately for the XOR function as well as the XNOR structure. The layout is sketched in Fig. 3. Analysis of these two cases for the input signals A and B, the output of the second inverter is nearly an XOR/XNOR function. For the structure stated in Fig. 3(a), when A = "HI,"A' must be "LO." A and A' signals are connected to the V_{DD} end of PMOS and the V_{SS} end of NMOS in the second inverter, respectively. Then the output of the second inverter functions are like a standard inverter, and outputs the signal B'. Therefore, the output signal will be a perfect AB' signal. On the other hand, when A = "LO,"A' must be "HI." The output of the second inverter will be a poor signal B because it transmits a signal "HI" by NMOS and a signal "LO" by PMOS. That is, if we use only 4 transistors to implement an XOR function, based on the inverter configuration, its output will be complete on AB' but poor on $A'B$. To improve this phenomenon, an additional transmission gate can correct this defect. In Fig. 4(a) [2], when signal A = "HI," the output of the structure is B', as we described above, the additional transmission gate does nothing. It will be a good AB' signal level. When signal A = "LO," the transmission gate will pass signal B to the output end directly and fully. Hence the output will be a good $A'B$ signal level. This function will be complete on all of the input cases. In Fig. 4(b), an additional tailing inverter can also improve the poor signal which comes from the output end of the 4-transistor XNOR structure, and output the good signal level. For these two cases, they do not need the complementary signal inputs, and the driving property is better than Fig. 1 as well. However, these structures still have some defects, such as no full driving capability on the output end, or more delay time.

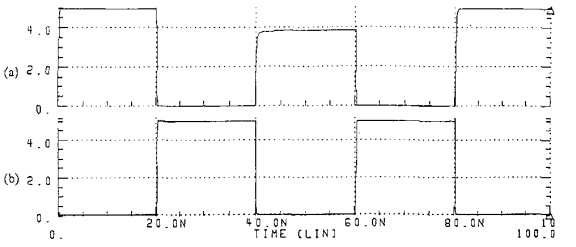


Fig. 9. (a) The output of 4–transistor XNOR and (b) the 6–transistor XOR.

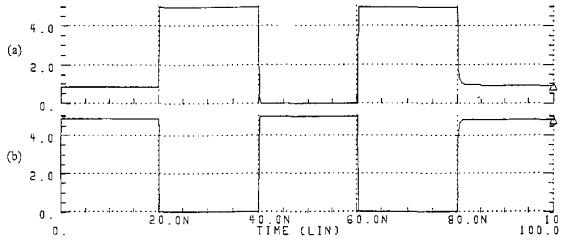


Fig. 10. (a) The output of 4–transistor XOR and (b) the 6–transistor XNOR.

III. The Proposed Method

On the 4-transistor design, the new proposed structures require non-complementary inputs and their output will be nearly perfect. The configurations are shown in Fig. 5. Analysis on XOR structure, the output signals in the cases of input signal $AB = 01, 10, 11$ will be complete. When $AB = 00$, each PMOS will be on and will pass a poor "LO" signal level to the output end. That is, if $AB = 00$, the output end will display a voltage, threshold voltage $|V_{PT}|$, a little higher than "LO," but double path driving capability exists, due to two PMOS's being on. Hence, though the output is not complete, the driving current will increase. For the XNOR function, the output signal in the case of $AB = 00, 01, 10$ will be complete. While $AB = 11$, each NMOS will be on and pass the poor "HI" signal level to the output end. The analysis of driving capability is the same as XOR structure. The proposed structures stated above are the versions of 4 transistors without a driving output. By cascading a standard inverter to the XNOR circuit, a new type of XOR, as shown in Fig. 6, will have a driving output, and the signal level at the output end will be perfect in all cases. The same property is present in the XNOR structure. The defect property of a 4-transistor type is that the output level will be higher or lower than the normal case by the voltage $|V_T|$, the threshold voltage of MOS. Under the condition of $|V_T|$ value, this poor level can still drive the inverter and make the inverter action correct!

IV. The Results of Simulation and Comparisons

The technology we used here is "CMOSTSMC" 0.8-μm technology[1], the parameters in NMOS and PMOS transistors

[1]This technology is developed by and used in Taiwan Semiconductor Manufacturing Company, Ltd., Hsin-Chu, Taiwan. The authors are very grateful for this support from TSMC.

TABLE II
INPUT/OUTPUT SIGNAL OF FIGS. 3(a) AND (b)

A	B	A XOR B	A XNOR B
1	1	0	poor 1
1	0	1	poor 0
0	1	poor 1	0
0	0	poor 0	1

TABLE III
THE PARAMETERS OF TRANSISTOR

TSMC 0.8 μm Typical SPICE Model CArd			
.MODEL nmos NMOS Level=3			
+VTO=-0.9	LD=60 N	WD=50 N	NFS=2E11
+TOX=19 N	UO=556	RSH=55	THETA=0.078
+NSUB=5.3E16	XJ=530 N	ETA=0.025	
+DELTA=0.8932	VMAX=150 K	KAPPA=0.085	MJSW=0.25
+CJ=350 U	CJSW=245 P	MJ=0.39	
+PB=0.85	CGSO=185 P	CGDO=185 P	RD=1830
+XL=0	XW=0	ACM=2	
+LDIF=250 N	TPG=1.0		
.MODEL pmos PMOS Level=3			
+VTO=-0.9	LD=60 N	WD=25 N	NFS=1E11
+TOX=19 N	UO=180	RSH=90	THETA=0.012
+NSUB=3.3 E16	XJ=60 N	ETA=0.037	
+DELTA=1.9	VMAX=158 K	KAPPA=1.2	MJSW=0.30
+CJ=595 U	CJSW=245 P	MJ=0.46	
+PB=0.81	CGSO=370 P	CGDO=187 P	RD=2900
+XL=0	XW=0	ACM=2	
+LDIF=250 N	TPG=-1.0		

are listed in Table III. All the processes are simulated by HSPICE on a SUN SPARC 2 workstation. The gate area ratio in PMOS and NMOS are about 2:1. The physical W/L size of PMOS and NMOS is 4.8 μ/0.8 μ and 2.4 μ/0.8 μ, respectively. The input signals are depicted in Fig. 7. The simulation of our design results are shown in Fig. 8 and Fig. 9. In Fig. 7, input signals for A and B cover 4 types of combinations, i.e., 00, 01, 10, and 11. The outputs of the 4-transistor XOR and the 6-transistor XNOR (a 4-transistor XOR cascaded by a tailing inverter) are shown in Fig. 8. The worst case occurs on $AB = 00$. The output signal level in XOR structure can't sink to "LO." In such a condition, the poor signal level can still drive the next inverter stage correctly! See the waveform in Fig. 8(b). For the 4-transistor XNOR and 6-transistor XOR, the output results are illustrated in Fig. 9. The worst case happens on $AB = 11$. The output signal level can't pull-up to "HIGH," but can still make the next inverter stage work correctly.

The results can be better, if the threshold value $|V_T|$ decreases. The lower $|V_T|$, the smaller the gap between the defect case and the normal case. In Fig. 8 and Fig. 9, $V_{NT} = 0.75$ V and $V_{PT} = -0.9$ V shown in Table III. These parameters of the NMOS and PMOS are used by the SPICE simulator. Fig. 10 is the other simulation result of the proposed XOR structure with the same parameters in Table III except $V_{NT} = 0.25$ V, and $V_{PT} = -0.25$ V. From the waveforms of Fig. 8 and Fig. 10, we can conclude that the smaller $|V_T|$ used, the better performance will be achieved, such as signal level and delay time. The higher $|V_T|$, the further away from the ideal case. If one uses the proposed methods of 4-transistor to drive canonical CMOS circuits, it can still work correctly. When the output levels of both 4-transistor cases are poor, an added tailing inverter can improve this defect, and the driving

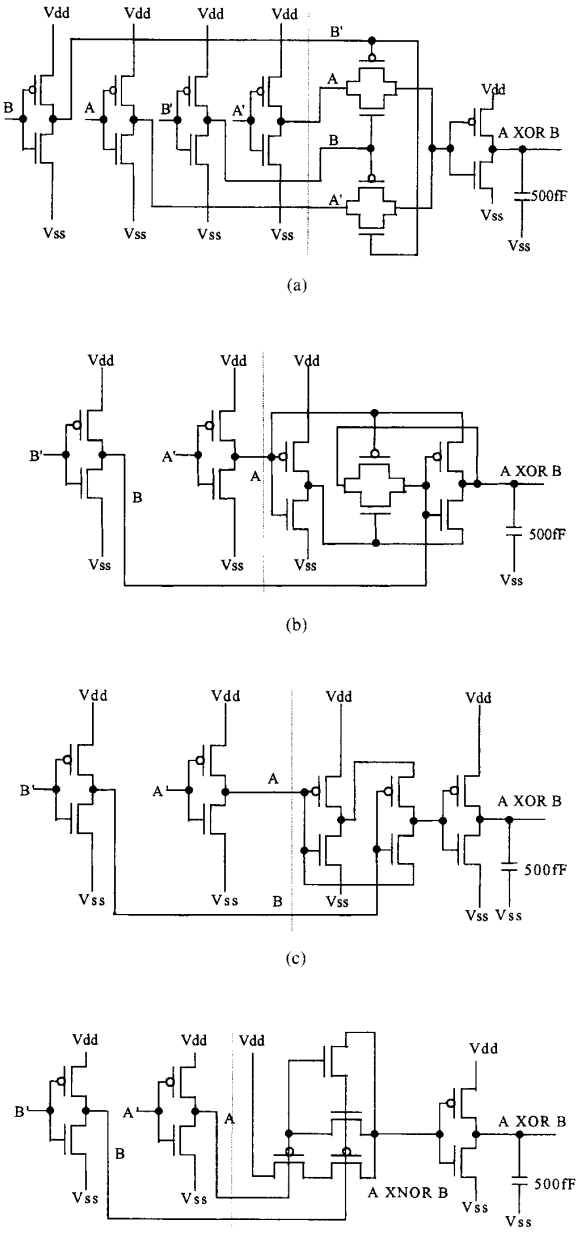
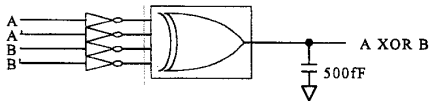


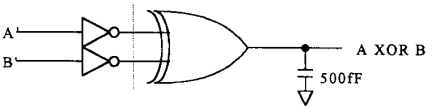
Fig. 11. (a) Realistic-simulated circuit for Fig. 2. (b) Realistic-simulated circuit for Fig. 4(a). (c) Realistic-simulated circuit for Fig. 4(b). (d) Realistic-simulated circuit for Fig. 6.

capability is present! For the proposed 6-transistor version, one can utilize it as a generalized XOR or XNOR function.

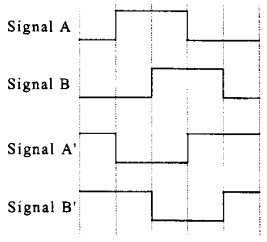
We simulated all the 6-transistor structures, ours and previous ones, Fig. 2, Fig. 4(a) and (b), and Fig. 6, under nearly realistic conditions for the analysis of driving capability. For the XOR structure, the circuits are redrawn in Fig. 11(a)–(d), respectively, and the equivalent logical diagrams are shown in (e) and (f).



(e)



(f)



(g)

Fig. 11 (continued). (e) The equivalent logic diagram for (a). (f) The equivalent logic diagrams for (b) and (c). (g) Input signals.

First, it inputs a signal, an off-the-shelf signal, to each inverter. The output waveform of an inverter will be a signal more like a realistic signal in a physical design. For convenience, we use A' and B' signal as inputs, pass them through the inverters. The signals display at the input ends of the XOR function will be A and B, and the output value at the output end of XOR function will be $A \oplus B$. In order to determine the driving capability, an additional capacitor is connected to the output end of each case. Then the driving capability can be reflected by its rising time and falling time. If a circuit has strong driving output, the rising time and falling time will be shorter than the one with poor driving output. In Fig. 11 (a)–(d), all the simulation conditions are the same except the structures of the XOR circuit. The simulation results of Fig. 11 (a)–(d) are revealed in Figs. 12–15, respectively.

From the waveforms of Figs. 12–15, we see the proposed method is better than the canonical methods, with respect to the driving property. The comparison of their outputs is depicted in Fig. 16. The rising time and falling time in Fig. 15 are shorter than the ones in Figs. 12–14. The delay and rising/falling time of all four XOR structures are illustrated in Table IV and Table V, respectively. Besides the driving property, an additional phenomenon is explored. That is, the waveforms of A and B in Fig. 13 are not smooth: they look like injected noise. To analyze this event, while any one of signal A or B changes state, due to propagation delay, *on* or *off* of the transmission gate element will not be fully synchronized to the first inverter in the XOR structure of Fig.

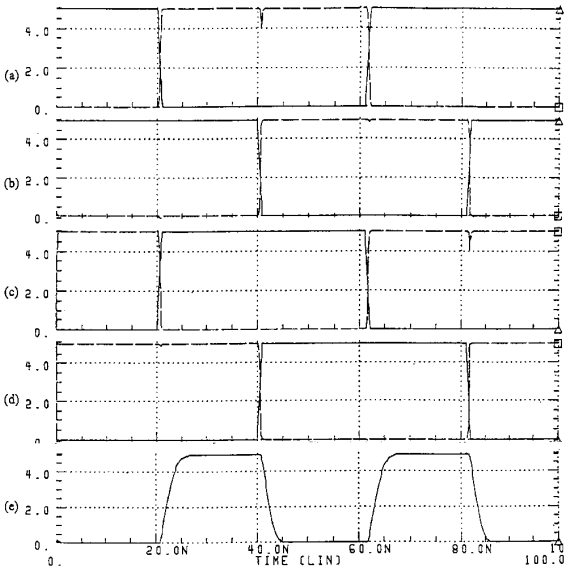


Fig. 12. The simulation result of Fig. 11(a). (a) _____: Input signal A of inverter. ___ ___: Input signal A' of 6–transistor XOR. (b) _____: Input signal B of inverter. ___ ___: Input signal B' of 6–transistor XOR. (c) _____: Input signal A' of inverter. ___ ___: Input signal A of 6–transistor XOR. (d) _____: input signal B' of inverter. ___ ___: input signal B of 6–transistor XOR. (e) Output signal of 6–transistor XOR.

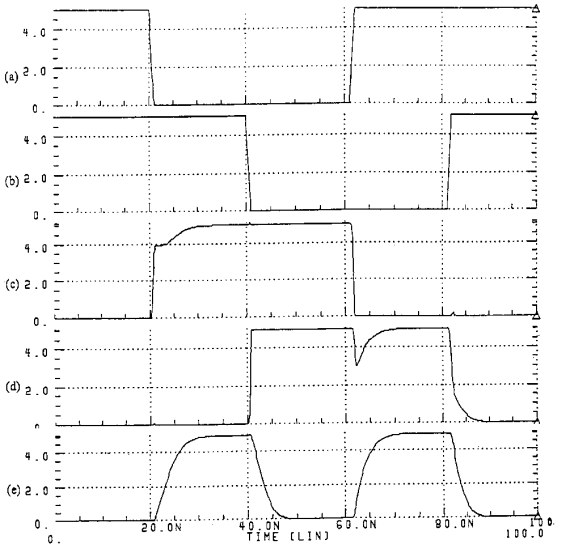


Fig. 13. The simulation result of Fig. 11(b). (a), (b) Input signals A', B' of inverters. (c), (d) Input signals A, B of 6–transistor XOR. (e) Output signal of 6–transistor XOR.

4(a). It results in both NMOS transistor and PMOS transistor turn on instantly. Hence the signal in the input end will drop amazingly (like the B signal in Fig. 13(d)). This defect will induce a upshot that the digital-typed simulator (e.g., Esim) often can't work right. In our proposed method, it doesn't have such noise-like weakpoint and shows nice response as depicted

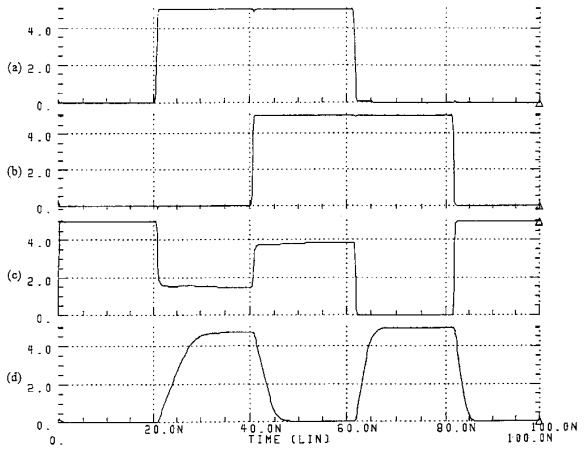


Fig. 14. The simulation result of Fig. 11(c). (a), (b) Input signals A, B. (c) Output signal of 4–transistor XNOR. (d) Output signal of 6–transistor XOR.

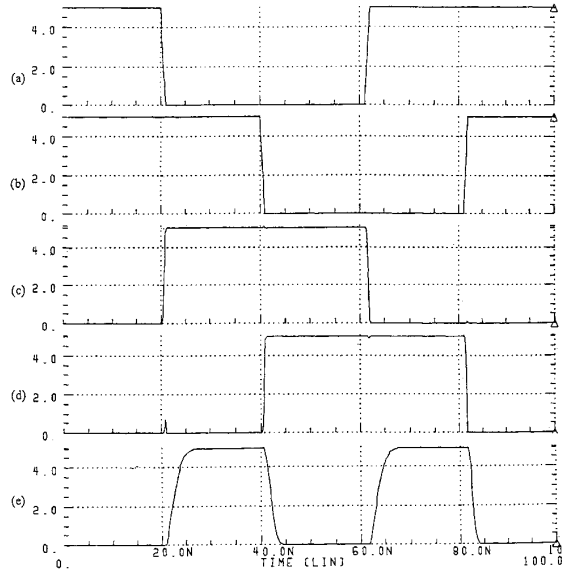


Fig. 15. The simulation result of Fig. 11(d). (a), (b) Input signals A', B' of inverters. (c), (d) Input signals A, B of 6–transistor XOR. (e) Output signal of 6–transistor XOR.

in Fig. 15. The comparison of all the methods we described and proposed in this paper are addressed in Table VI. The competing factors are the number of transistors, the driving capability, non-complementary signal inputs, and the output signal levels. From Table VI, it is obvious that our designs are the most competitive ones among all methods. The average power dissipation of each design is given in Table VII for reference.

V. Conclusion

In this paper, we proposed new configurations of CMOS designs for the exclusive-OR and exclusive-NOR functions.

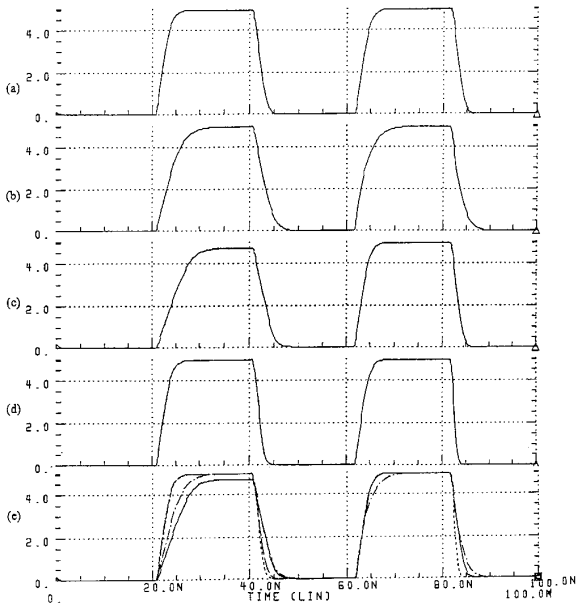


Fig. 16. The comparison of four XOR structures. (a) The simulation results of Fig. 11(a). (b) The simulation results of Fig. 11(b). (c) The simulation results of Fig. 11(c). (d) The simulation results of Fig. 11(d). (e) (a): ___ ___, (b): ___.___, (c): _____, (d): _ _ _ _ _ .

TABLE IV
Delay Time Analysis of Each XOR Structure

Unit: ns	00→10	10→11	11→01	01→00	Average
Fig. 2	1.64	1.45	1.71	1.59	1.6
Fig. 4(a)	2.86	2.11	1.72	1.6	2.07
Fig. 4(b)	3.98	8.1	1.67	1.59	3.84
Fig. 6	1.75	1.26	1.68	0.98	1.42

Remark: 00→10: input signals AB change from 00 to 10. delay time=time difference between input transition (50% level) and the 50% output level. (This is the time taken for a logic transition to pass from input to output).

TABLE V
Rising/Falling Time Analysis of Each XOR Sructure

Unit: ns	00→10 rising	10→11 falling	11→01 rising	01→00 falling	Average rising	Average falling
Fig. 2	3.2	2.56	3.19	2.6	3.2	2.58
Fig. 4(a)	5.89	4.21	4.96	3.75	5.43	3.98
Fig. 4(b)	8.04	4.06	3.2	2.59	5.62	3.33
Fig. 6	3.2	2.08	3.22	1.36	3.21	1.72

Remark: rising time=time for a waveform to rise from 10% to 90% of its steady-state value.
falling time: time for a waveform to fall from 90% to 10% of its steady-state value.

For all 4-transistor configurations, as we stated before, our designs no longer need complementary signal inputs and only one poor signal level on output end. For the 6-transistor types, the proposed designs have non-complementary inputs, good signal level outputs and the best driving capability. According to the simulation results of both 4-transistor and 6-transistor types, our designs are the better and more competitive ones than others, respectively.

TABLE VI
COMPARISON OF EACH XOR FUNCTION

	00	01	10	11	#Tr.	Driving Output	Complementary Output
Fig. 1	O	O	O	O	4	No	Yes
Fig. 2	O	O	O	O	6	better	Yes
Fig. 3	X	X	O	O	4	No	No
Fig. 4(a)	O	O	O	O	6	good	No
Fig. 4(b)	O	O	Δ	O	6	worse	No
Fig. 5	O	O	O	X	4	No	No
Fig. 6	O	O	O	O	6	best	No

Symbols: $AB = 00, 01, 10, 11$. #TR.: number of transistors. O: good signal level. X: poor signal level. Δ: nearly good signal level.

TABLE VII
AVERAGE POWER DISSIPATION FROM 0 THROUGH 100 ns

Unit: W	Power Dissipation
Fig. 2	3.1181 E-04
Fig. 4(a)	2.8901 E-04
Fig. 4(b)	4.1612 E-04
Fig. 6	3.1927 E-04

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