Optimization of Chopper Amplifiers for Speed and Gain

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Abstract— **This paper presents design techniques to optimize the performance of chopper-stabilized ac-coupled CMOS inverter amplifiers. These amplifiers are used as comparators in high-speed flash analog-to-digital converters extensively [1]–[3]. For any given process technology, as the required conversion speed and resolution are increased, the amplifiers are required to increase their conversion speed and resolution, and to have higher switching speed as well as higher gain. Although these two requirements are in general contradictory, they can be optimized by proper design. In this paper, analytical expressions are derived which can be used to optimize these amplifiers. The results obtained from these analytical expressions and SPICE simulations agree well.**

I. Introduction

During the past few years, several high speed CMOS flash analog-to-digital converters (ADC) using ac-coupled inverter amplifying stages as comparators have been reported [1]–[3]. For a given process, these comparators achieve the maximum switching speed. As the speed of the flash ADC increases, each amplifier within the comparator has to be optimized for speed as every nanosecond becomes important. One way of maximizing the speed of an ac-coupled inverter stage is to minimize the gain per stage and trade off gain for bandwidth. In an ADC, the required gain of the comparator is determined by the reference voltage and the resolution of the ADC as given by:

$$A_t = V_{\rm dd}2^n/V_{\rm ref} = (A_V)^N \tag{1}$$

where A_t is the total gain, $V_{\rm ref}$ is the reference voltage, n is the resolution of the ADC, A_v is the gain of each amplifying stage, and N is the number of stages in the comparator. Once the gain per stage, A_v, is minimized to achieve the maximum speed, the number of stages, N, can be calculated from (1).

This simple design technique has several drawbacks. First, with minimum A_v, the total number of stages, N, may be too large, which in turn will decrease the speed of the comparator. Second, minimizing A_v in general requires minimum channel length for the CMOS transistors. This could produce unacceptably large supply current variations over process corners.

In [4], a detailed analysis is done on the small signal transient response of cascade of resettable amplifiers. The analysis assumes that the amplifiers start from high-gain region with zero initial conditions prior to amplification and arrives at an equation giving the output voltage, $V_o(t)$, versus time and other circuit parameters. This equation is given below:

$$V_o(t) = [V_{\rm ref}(g_m R/2)^n][1 - e^{-t/(t1 g_m R)}\sum_{k=0}^{N-1}(t/g_m R t_1)^k/k!] \tag{2}$$

where g_m is the transconductance and R is the total output resistance of the stage, $t_1 = C_o/g_m$ with C_o being the total output capacitance, N is the number of stages, and $V_{\rm ref}$ and n are as defined earlier.

If the propagation delay, T_{pd}, is defined as the time it takes for $V_o(t)$ to reach $V_{\rm dd}$, then from (2) $T_{\rm pd}$ can be optimized as a function of N. That is, for a given $t_1, g_m, R, n, V_{\rm dd}$, and $V_{\rm ref}$ there is a value for N that minimizes T_{pd} from (2). It is shown in [4] that if the product of $g_m R \gg 1$, then (2) can be simplified and an analytical expression can be derived for T_{pd} as given in (3) below:

$$T_{pd}(N) = t_1(V_f 2^n N!/V_{\rm ref})^{1/N} \tag{3}$$

where V_f is the final output voltage, usually taken to be equal to $V_{\rm dd}$. Knowing t_1, n, V_f, and $V_{\rm ref}, T_{pd}(N)$ can be minimized with respect to N. Fig. 1 shows the plot of $T_{pd}(N)$ versus N, as obtained from (3) and SPICE simulations, for typical parameters of $V_f = 5$ V, $V_{\rm ref} = 1.28$ V, $n = 8$ bits, and $t_1 = 0.3$ ns. It can be calculated from (3) that the minimum value of T_{pd} is obtained for $N = 8$. This minimum is very broad, and in fact, any N in the range of $6 < N < 12$ will yield a reasonable minimum for $T_{pd}(N)$.

This optimum value of $N_{opt} = 8$ and its corresponding minimum value of T_{pd} is obtained assuming that all the amplifying stages start from their high-gain linear regions prior to amplification and consequent voltage comparison. For ac-coupled chopper amplifiers discussed above, this re-

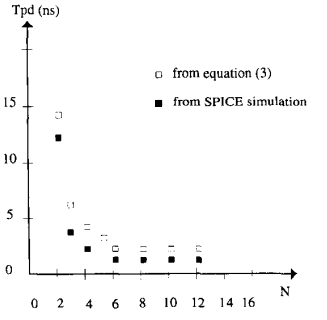

Fig. 1. Plot of T_{pd} versus N obtained from (3) and SPICE simulations with $A_1 \gg 1$.

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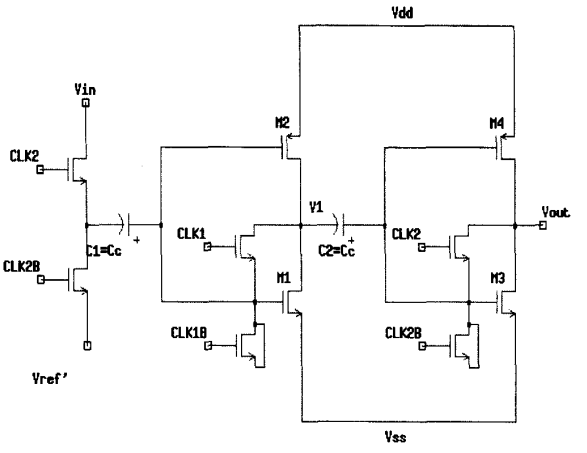
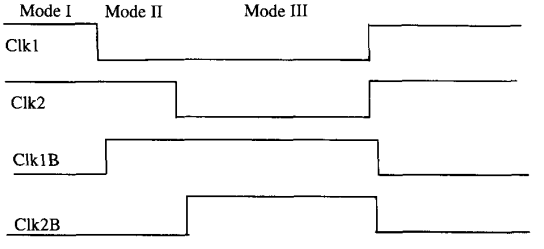


(a)



(b)

Fig. 2. a) Simplified schematic diagram of two-stage ac-coupled inverter chopper amplifier. b) Required timing diagram.

quirement can only be met by staggering the clocks of the feedback switches [6] (see Fig. 2(b)). If N_{opt} is used and the clocks are staggered, i.e., turned off in succession, this will require eight non-overlapping clocks which increase the effective propagation delay of the comparator. If the clocks are not staggered, the residual clock feedthroughs, in spite of the clock-feedthrough-cancellation techniques, will saturate the amplifiers which in turn increase the propagation delay. Therefore the optimum value of N, N_{opt}, calculated from (2) or (3) may not be feasible in practice. However, since the local minimum of T_{pd} versus N is relatively broad, as depicted in Fig. 1, it is possible to choose $N < N_{opt}$ and still achieve a reasonable small T_{pd}.

In this paper, simple analytical equations are derived which give the inverter amplifier switching delay, T_d, and the gain, A_v, as a function of process, device, and circuit parameters. Using these equations, one can optimize the performance of an ac-coupled inverter amplifier optimizing the performance of the comparator built from cascade of such amplifiers. These equations are also compared to SPICE simulation results for accuracy.

II. Analysis of AC-Coupled Inverter Amplifiers

In order to optimize the speed of an ac-coupled inverter amplifier, one should determine the interaction among the various process, device, and circuit parameters under various modes of operation of the amplifier. There are three basic modes of operation in these comparators as shown in the simplified schematic diagram of a two-stage comparator in Fig. 2. Mode I, or offset cancellation mode, during which both clocks clkl and clk2 are on. During this mode, the input as well as the offset voltages of the inverters are sampled onto the interstage capacitors, C_1 and C_2. Mode II, or clock-feedthrough cancellation mode, when clkl is turned off and clk2 is on. During this mode the feedthrough of clock clkl is stored on the interstage capacitor C_2 and successively cancelled if enough time is allowed for the stages to settle before clock clk2 is turned off. Mode III, or amplification mode, during which the comparator amplifies the difference between the input and the appropriate binary fraction of the reference voltage, $V_{\text{ref}'} = D\,V_{\text{ref}}/2^n$ where D is an integer, generating a decision bit [5].

To optimize the comparator performance, its operation during Modes I–III should be well understood. To this end, simplified equations characterizing the operation of the comparator during these modes are derived. In the following analysis, a simple quadratic current versus voltage relationship as well as small signal operation is assumed. These assumptions are later justified by comparing analytical results with that obtained from SPICE simulations.

During Mode I, devices $M1 - M4$ in Fig. 2 operate in the saturation region, in particular the drain currents of devices M1 and M2 are given by:

$$I_1 = (\beta_1/2)(V_1 - V_{t1})^2 \tag{4}$$

$$I_2 = (\beta_2/2)(|V_{\text{dd}} - V_1| - |V_{t2}|)^2 \tag{5}$$

where,

I_1 and I_2	drain currents,
$\beta_1 = k_{p1}(W_1/L_1)$ and $\beta_2 = k_{p2}(W_2/L_2)$,	
k_{p1} and k_{p2}	conduction factors,
W_1 and W_2	effective channel widths,
L_1 and L_2	effective channel lengths of transistors M1 and M2, respectively,
V_{dd}	supply voltage,
V_1	output bias voltage, and
V_{t1} and V_{t2}	threshold voltages for the PMOS and NMOS devices.

Setting $I_1 = I_2$, and defining $m = (\beta_1/\beta_2)^{0.5}$ and $n_1 = W_1/L_1$, and assuming $V_{t1} = V_{t2} = V_t$, (4) and (5) can be solved to obtain:

$$I_1 = (1/2)n_1 \cdot k_{p1}[(V_{\text{dd}} - 2V_t)/(1+m)]^2 \tag{6}$$

$$V_1 = [V_{\text{dd}} + V_t(m-1)]/(1+m). \tag{7}$$

The dc gain, Al, of the first inverter in Modes II and III of operation is given by:

$$A_1 = (g_{m1} + g_{m2})/(g_{ds1} + g_{ds2}) \tag{8}$$

where g_{m1}, g_{m2} and g_{ds1}, g_{ds2} are the transconductances and output conductances of devices M1 and M2, respectively. Using $m = (\beta_1/\beta_2)^{0.5}, g_{m1} = (2\beta_1 I_1)^{0.5}$ and $g_{m2} = (2\beta_2 I_1)^{0.5}$ and assuming $g_{ds1} = aI_1/L_1, g_{ds2} = aI_1/L_2$ where a is a process parameter responsible for channel length modulation, assumed to be the same for n- and p-channel devices, one obtains

$$A_1 = 2L_1(1+m)(1+m^2)/m^2[a(V_{\rm dd} - 2V_t)]. \tag{9}$$

During comparison mode or Mode III, the switching delay, T_d, of each stage is given by $T_d = r_0 \cdot C_1$ where r_0 is the output resistance of the inverter and C_1 is its load capacitance. C_1 can be approximated by:

$$C_1 = C_c/(C_c/C_{\rm in} + 1) \tag{10}$$

where C_c is the interstage coupling capacitor and $C_{\rm in}$ is the total input capacitance of the following stage given by:

$$\begin{aligned} C_{\rm in} = &(C'_{gs1} n_1 L_1^2 + C'_{gs2} n_2 L_2^2) \\ &+ (1 + A_1)(C'_{gd1} n_1 L_1 + C'_{gd2} n_2 L_2) \end{aligned} \tag{11}$$

where C'_{gs1} and C'_{gs2} are the gate-to-source capacitance per unit channel area, C'_{gd1} and C'_{gd2} are the gate-to-drain capacitance per unit channel width of the n- and p-channel devices, respectively. $n_2 = W_2/L_2$ is the aspect ratio of the p-channel transistor M2.

The value of n_2 can be obtained from the expression for m as follows.

$$\begin{aligned} m &= (\beta_1/\beta_2)^{0.5} \\ &= [(k_{p1} W_1/L_1)/(k_{p2} W_2/L_2)]^{0.5} \\ &= (3.6 n_1/n_2)^{0.5} \end{aligned} \tag{12}$$

where, $k_{p1} = 3.6k_{p2}, W_1 = n_1 L_1, W_2 = n_2 L_2$, and $L_1 = L_2$. From (12), n_2 is given by

$$n_2 = 3.6 n_1/m^2. \tag{13}$$

From (6), solving for n_1,

$$n_1 = 2I_1(1+m)^2/[k_{p1}(V_{\rm dd} - 2V_t)^2]. \tag{14}$$

Using (9), (13), and (14) in (11), and assuming $C'_{gs1} = C'_{gs2} = C'_{gs}, C'_{gd1} = C'_{gd2} = C'_{gd}$, and $A1 \gg 1$, one obtains,

$$\begin{aligned} C_{\rm in} = &\{1 + 3.6/m^2\}\{2C'_{gs} I_1 L_1^2 (1+m)^2/[k_{p1} \\ &\cdot (V_{\rm dd} - 2V_t)^2] \\ &+ 4C'_{gd} I_1 L_1^2 (1+m)^3 (1+m)^2/[m^2 a k_{p1} 7 \\ &\cdot (V_{\rm dd} - 2V_t)^3]\} \end{aligned} \tag{15}$$

The time constant of the stage, using (10), is given by

$$T_d = r_0 C_1 = L_1 C_c/[aI_1(1 + C_c/C_{\rm in}] \tag{16}$$

where, $r_0 = L_1/(aI_1)$. Substitution of (15) into (16) will give the equation for the time constant T_d of the stage as a function of the process parameters $C'_{gs}, k_{p1}, V_t, C'_{gd}, a$, and device parameters L_1 and m, and circuit parameters $I_1, V_{\rm dd}$, and C_c.

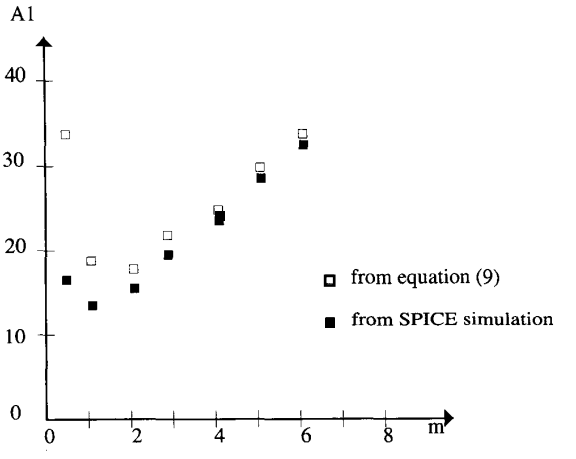


Fig. 3. Plot of A_1 versus m from (9) and SPICE simulations.

Using A_1 as given by (9), the low-frequency gain, A_v, of the ac-coupled inverter can be calculated. Due to ac coupling between stages, the total gain will be somewhat lower than A_1. This attenuation is given by:

$$k = 1/(1 + C_{\rm in}/C_c). \tag{17}$$

Therefore,

$$A_v = A_1 k. \tag{18}$$

Substituting (9) and (17) into (18) yields

$$\begin{aligned} A_v = &2L_1(1+m)(1+m^2)/[am^2(V_{\rm dd} - 2V_t) \\ &\cdot (1 + C_{\rm in}/C_c)]. \end{aligned} \tag{19}$$

(19) in conjunction with (15) give the low frequency gain of the ac-coupled inverter.

A_1, T_d, and A_v as a function of inverter aspect ratio parameter, m, as given by (9), (15)–(16) and (15), (17)–(19) are plotted in Figs. 3–5, respectively. Also shown in Fig. 4 is the average propagation delay of inverter, $T_{\rm avg}$, of high-to-low and low-to-high output transitions obtained from SPICE simulations. As it can be seen $T_{\rm avg}$ is smaller than T_d. This is because as the input signal is amplified in the stages within the comparator, the succeeding stages are driven by stronger signal and thus switching speed is increased [6]. The following typical parameters are assumed in generating these plots:

$$\begin{aligned} &C'_{gd} = 5e-10F/m, \quad C'_{gs} = 1.7e-3F/m, \quad V_t = 1v, \\ &a = 1.5e-7m/v, \quad k_{p1} = 90e-6A/v^2, \quad L_1 = 1\,\mu{\rm m}, \\ &C_c = 0.3\,{\rm pF}, \quad I_1 = 100\,\mu{\rm A}, \quad \text{and} \quad V_{\rm dd} = 5\,{\rm V}. \end{aligned}$$

Also shown in Figs. 3–5 are the results obtained from SPICE simulations. As it can be seen, the agreement between the simplified equations (9)–(19) and SPICE simulations are satisfactory.

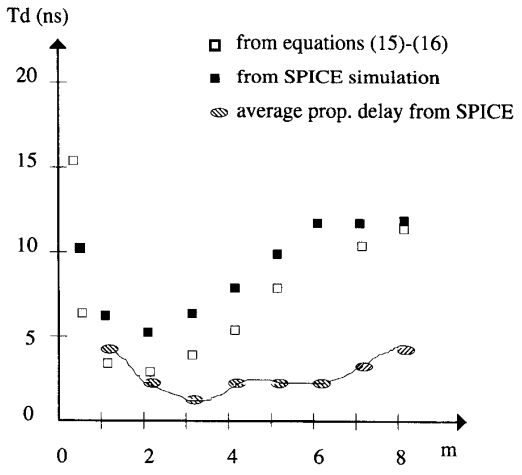


Fig. 4. Plot of T_d versus m from (15) and (16) and SPICE simulations. The average propagation delay, T_{pd}, obtained from SPICE simulations is also plotted.

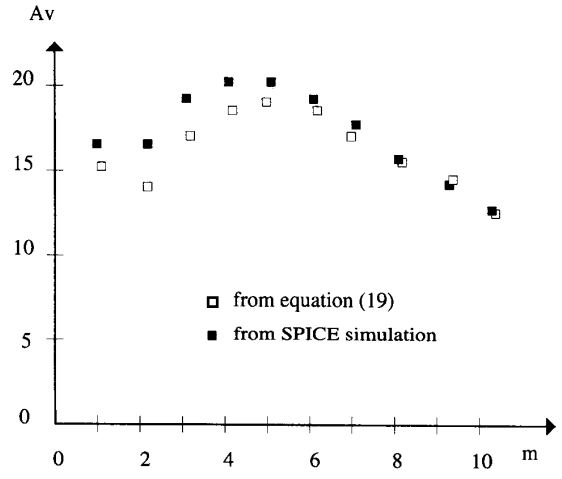


Fig. 5. Plot of A_v versus m from (19) and SPICE simulations.

III. Design Optimization

For a given process, the design parameters at one's disposal are the device parameters L_1 and m, and circuit parameters $V_{\rm dd}, N, C_c$, and I_1. $V_{\rm dd}$ is usually determined by process as well as application. The value of N can be first estimated from (3) such that $N = N_{opt}$ and then somewhat reduced if this value of N_{opt} is deemed unfeasibly too large. The value of the inverter current, I_1, can be first estimated from the total current allocation, I_t, of the entire chip. for an n-bit flash ADC, the current per comparator, I_c, can be approximated by $I_c = (b\,I_t)/2^n$, where, ($b\,I_t$) is the fraction of the total current allocated to the comparators in the flash ADC, I_1 is then given by $I_1 = I_c/N$ where the value of N is as estimated above. At this point in the design the value of N is only an estimate and it may have to be revised later to make sure that all the design requirements are met.

The value of C_c is determined from clock feedthrough considerations. The clock feedthrough of the feedback switches in Fig. 2 is inversely proportional to C_c. This feedthrough causes a voltage step at the input of the inverter changing its output. The amount of change at the output should be small enough not to cause the stage to saturate [6]. The magnitude of clock feedthrough at the input as well as the inverter gain, A_1, will vary with process. Therefore the size of C_c and the feedback switches are determined from the following two considerations: 1) to minimize clock feedthrough, one needs a large C_c and small size feedback switches, and 2) to minimize the time required for offset and input acquisition in Mode I, as well as settling time during feedthrough cancellation in Mode II, a small C_c and large switches are needed.

These two requirements are contradictory and a compromise should normally be reached. However, if the feedthrough at the input is cancelled by the use of dummy devices as in Fig. 2, then the disturbance of the output voltage will be at a minimum and thus the size of C_c can be somewhat reduced to speed up feedthrough cancellation mode. If CMOS transmission gates have to be used for the feedback switches because of the value of the dc bias voltage V_1, then first p-channel switch should be turned off while n-channel switch is still on. Then the n-channel switch is turned off and its feedthrough successively cancelled by a dummy n-channel transistor. This is necessary since n-and p-channel transistor switches normally do not cancel each other's feedthroughs due to unequal lateral diffusions. To simplify the design, the value of m should be chosen such that V_1 is biased low enough (see (7)) so that only an n-channel transistor is required for the feedback switch.

With the value of $V_{\rm dd}, C_c$ and the initial values of N and I_1 decided upon, the only parameters remaining are the effective channel length, L_1, and the inverter aspect ratio parameter, m. For a given process, one should plot A_1, A_v, and T_d as a function of m with L_1 as a parameter in the plots to determine the variation of these parameters with process corners. Since m is equal to the square root of the ratio of the betas of the n- and p-channel devices, as given before, its value could change from the designed value by as much as $\pm 100\%$ due to process variations. Therefore the parameters A_1 and T_d should be chosen to minimize their variation with respect to m. Minimizing variation of A_1 with m reduces the possibility of any stage saturating due to the clock feedthrough as explained earlier. Minimizing the variation of T_d with m helps maintain relatively constant propagation delay over process.

The optimum design is therefore obtained for the values of m that minimize A_1 and T_d. From these optimum values of m, the largest possible value of m is chosen to minimize the bias voltage V_1 according to (7) as explained before. This optimum value of m does not necessarily minimize the variation of A_v with m, however. The variation of A_v with m does not present any design problems as long as a given minimum total gain, A_t, is realized. Once each stage is optimized, the value of N can be obtained from (1). This value of N, should then be compared with N_{opt} determined earlier and the corresponding value of T_{pd} calculated using (3). Several iterations may be necessary to make sure that the per-stage current requirement

is also met. The values obtained at this point can then be used as a starting point for final optimization using SPICE.

For example, from Figs. 3 and 4 the optimum value for m is $1 < m < 2$. Using $m = 2, V_{\rm dd} = 5$ V, and $V_t = 1$ V, gives $\beta_1/\beta_2 = 4$ and from (7) $V_1 = 1.33$ V. From Figs. 3 and 5, the inverter gain, $A_1 = 19$, and the stage gain, $A_v = 17$. Therefore, from (1), for a 10-bit flash ADC with $V_{\rm ref} = 1.28$ V, $N = 3$. From Fig. 1, a better choice for N is $N = 4$. Values larger than four will require considerable amount of staggered clocks and actually increase T_{pd}.

IV. Circuit Implementation

The techniques described above were applied to the design of a 20 MHz 6- and 8-bit flash analog-to-digital converters. The process was 1.2-μm CMOS with maximum supply of $V_{\rm dd} = 5$ V. First, using (3) N_{opt} was calculated to be equal to 8. Referring to Fig. 1, it can be seen that a comparator with $N = 5$ will basically have the same T_{pd} as with $N = 8$, in fact a comparator with $N = 5$ will be faster due to the fact that it will require a fewer number of non-overlapping clocks. Next, comparing a five-stage comparator, $N = 5$, to a three-stage comparator, $N = 3$, it can be seen that for $N = 5, T_{pd}$ is only 3 ns shorter. This time can be easily used up to generate the additional two non-overlapping clocks required for $N = 5$. Therefore, it was decided that any value of N in the range of $3 < N < 5$ is acceptable as long as it provides the sufficient gain as given in (1). A value of $C_c = 0.3$ pF was chosen as a good compromise to achieve the required speed with reasonable amount of feedthrough. The current in each stage, I_1, is set to be 100 μA. With the initial values of $V_{\rm dd}, N, C_c$, and I_1 chosen as above, the only parameters remaining are the inverter aspect ratio, m, and the effective channel length L_1. In order to decide on the proper values of m and L_1, the variables A_1, T_d, and A_v as given by the aforementioned equations were plotted as a function of m with L_1 as a parameter over process corners. Plots similar to Figs. 3–5 were obtained.

From these plots, it was decided that the optimum value for L_1 and m were $L_1 = 1.15\,\mu$m and $m = 2$; giving $n_1 = 2.22, n_2 = 2$, and $V_1 = 1.33$ V. These parameters provided the following typical values: $A_1 = 17, T_d = 5$ ns, $A_v = 16$, and $T_{pd} = 6$ ns. Extensive SPICE simulations indicated that with the typical value of I_1 increased to 150 μA, $m = 2, n_1 = 3.33, n_2 = 3, V_1 = 1.33$ V, and $N = 3$, the comparator meets the 20 MHz operation requirements.

V. Conclusions

In this paper a design technique to optimize the performance of CMOS comparator constructed from ac-coupled inverter amplifier stages have been presented. First order analytical equations were derived that can be used to arrive at the optimum comparator design under a given design constraints. The equations show the interactions among process, device, and circuit parameters and indicate how these interactions can be utilized for the best possible circuit solution. The results predicted compared favorably to that obtained from SPICE simulations.

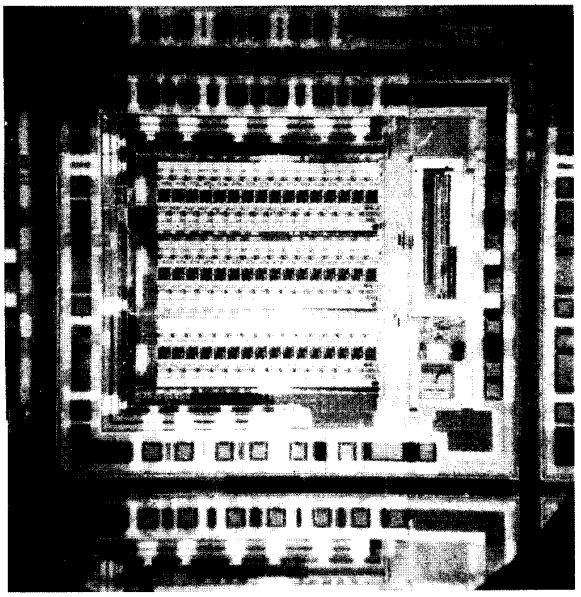


Fig. 6. The die photo of the 20 MHz triple 6-bit ADC chip.

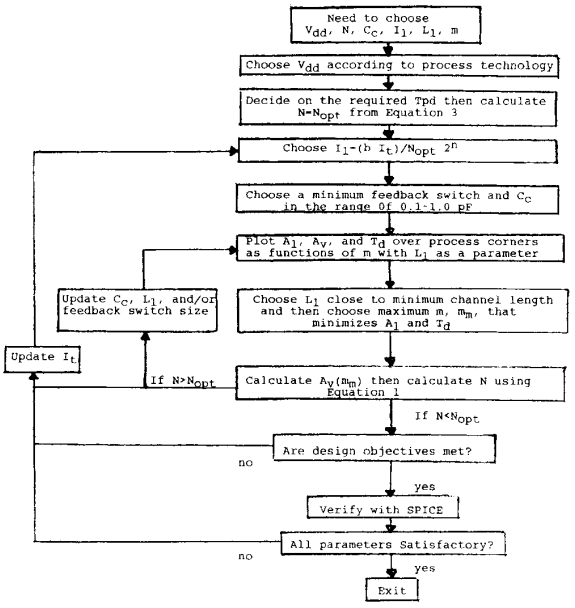


Fig. 7. The design flow chart.

Using these equations a CMOS comparator utilizing three ac-coupled inverter stages was designed for a 20 MHz triple 6-bit flash ADC chip using 1 V reference. The die photo of the chip is shown in Fig. 6. The chip achieves less than 1/4 LSB integral nonlinearity with differential nonlinearity of less than 1/8 LSB drawing 66 mA from a 5 V supply operating at 20 MHz. The 160 × 160 mil chip is fabricated in 1.2 μm n-well CMOS process. Extensive SPICE simulations

were done to varify the design over process corner variations. Although these equations were derived for single-ended ac-coupled inverter amplifiers, they can be used equally well in the design of differential ac-coupled amplifiers.

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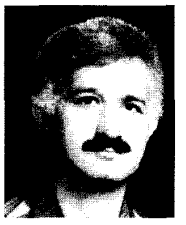

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