High-Speed Low-Power Direct-Coupled Complementary Push–Pull ECL Circuit

C. T. Chuang and K. Chin

Abstract—**This paper presents a high-speed low-power direct-coupled complementary push–pull ECL (DC-PP-ECL) circuit. The circuit features a direct-coupled pnp pull-up and npn pull-down scheme with no extra biasing circuit for the push- and pull-transistor. The bias of the pull-up pnp transistor is established entirely by direct tapping of the existing voltage levels in the current switch. The scheme provides a sharp self-terminating dynamic current pulse through the pull-up pnp transistor during the switching transient, thus completely decoupling the collector load resistor from the delay path. Based on a 0.8-μm double-poly self-aligned complementary bipolar process, the circuit offers 2.0X (2.2X) improvement in the loaded delay at 1.0 (0.5) mW/gate and 2.2X improvement in the load driving capability at 1.0 mW/gate compared with the conventional ECL circuit.**

I. Introduction

THE power dissipation of high-speed bipolar ECL circuits (Fig. 1(a)) has long been known to limit their VLSI applications. The power/speed limitation of the ECL circuit comes primarily from the passive resistors in its delay path where the pull-up delay is limited by the collector load resistor R_C and the pull-down delay is limited by the emitter-follower resistor R_{EF}. Recently, an ac-coupled complementary push–pull ECL (AC-PP-ECL) circuit (Fig. 1(b)) with significantly improved power-delay has been described [1], [2]. The circuit utilizes two capacitors to couple a transient voltage pulse from the common-emitter node of the switching transistors to the bases of a pair of pnp-npn push–pull transistors to achieve a non-saturating complementary push–pull configuration. Implemented in a 0.8-μm fully-complementary bipolar technology, the circuit has been shown to achieve a 2X improvement in the power-delay product compared with the conventional ECL circuit [3]. However, the use of capacitor coupling requires careful design, and additional devices (and power) are needed to implement the biasing circuit for the push–pull transistors.

In this paper, we present a high-speed low-power direct-coupled complementary push–pull ECL (DC-PP-ECL) circuit (Fig. 1(c)). The circuit features a direct-coupled pnp pull-up and npn pull-down scheme, where the bias of the pull-up pnp transistor is established entirely by direct tapping of the existing voltage levels in the current switch. The scheme provides a sharp self-terminating dynamic current pulse through the pull-up pnp transistor during the switching transient, thus completely decoupling the collector load resistor R_C from the delay path and allowing a very small switching current to be used for the current switch without degrading the performance. In addition, the scheme eliminates the need for the extra biasing circuit and power for the push- and pull-transistor, thus achieving a complementary push–pull configuration with minimum power consumption.

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II. Circuit Configuration and Operation

In the present scheme, an additional pnp transistor Q_P and a diode D_1 are added to the conventional ECL circuit as shown in Fig. 1(c). Transistor Q_P and diode D_1 are biased at "cut-in" condition (with very low dc current) when the input is "High." Notice that this bias is established naturally by the voltage difference across Node $\bar{C}$ and Node A since

$$V_{\bar{C}} = V_{CC} = V_{O,High} + V_{BE,Qu}$$
$$V_A = V_{IN,High} - V_{BE,Q1}$$

when the input is "High." Therefore,

$$V_{\bar{C}} - V_A = V_{BE,Qu} + V_{BE,Q1}$$

and there is a voltage drop of $2V_{BE}$ across Q_P and D_1. The collector load resistor R_{C2} serves to limit the (standby) current through Q_P.

When the input falls from "High" to "Low," the voltage at Node A follows immediately. Since the voltage at Node $\bar{C}$ will remain at V_{CC} until the current switch switches, the voltage across Node $\bar{C}$ and Node A will increase momentarily, resulting in base-emitter over-drive for Q_P and D_1, and thus large dynamic current through Q_P to charge up the output node. Notice that:

1) the biasing of the pull-up pnp is established entirely by direct tapping (hence the name "direct-coupled") of the existing voltage levels in the current switch,
2) the large dynamic pull-up current is available before the current switch switches,
3) the maximum base-emitter voltage over-drive for Q_P and D_1 is ΔV/2 (ΔV/4 for individual device), where ΔV is the logic swing, due to the emitter dotted-OR configuration of the input transistor and the reference transistor Q_2,
4) the dynamic current is drawn from Node $\bar{C}$. Thus the voltage at Node $\bar{C}$ will decrease as the dynamic current increases, providing a self-terminating action to ensure a sharp dynamic current pulse during the transient.

Once the input crosses the reference voltage (Ground in Fig. 1), the current switch switches and the voltage at Node $\bar{C}$ will be pulled down by the switching current through the reference transistor Q_2. In the final steady-state (with the input at "Low" now), the voltage at Node $\bar{C}$ drops by an amount equal to the voltage swing ΔV, while the voltage at Node A drops only by ΔV/2. The voltage difference between Node $\bar{C}$ and Node A thus decreases by ΔV/2, and Q_P and D_1 are now near cut-off.

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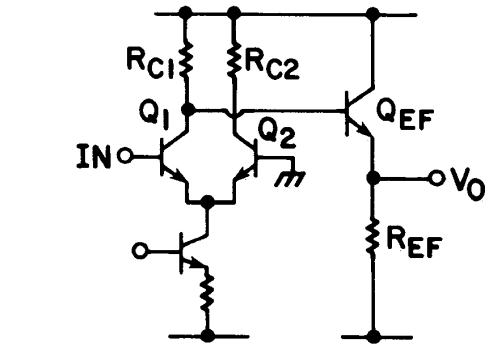
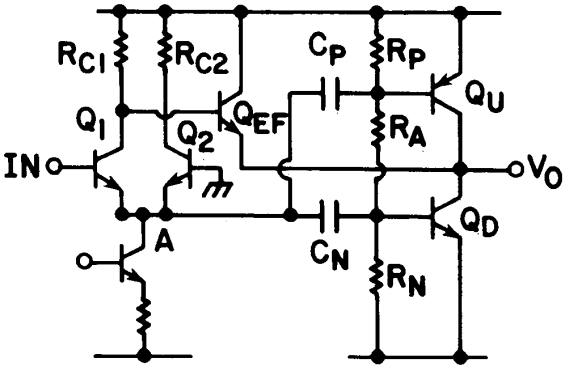


(a)



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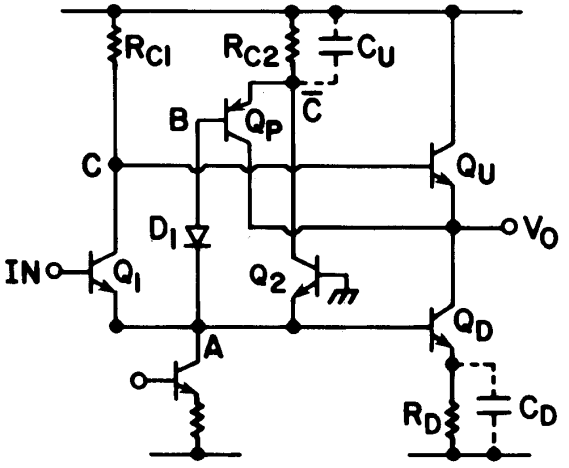


(c)

Fig. 1. Schematics of (a) conventional ECL circuit, (b) AC-PP-ECL circuit, and (c) DC-PP-ECL circuit (C_U and C_D are speed-up capacitors if desired).

When the input rises from "Low" to "High," the voltage at Node A follows once the input crosses the reference voltage. Q_P and D_1 remain at cut-off initially until Node $\bar{C}$ is pulled up through the collector load resistor R_{C2}. As the voltage at Node $\bar{C}$ rises to approach its steady-state value of V_{CC}, Q_P and D_1 enter the "cut-in" condition as described previously.

Notice that the bias across the pnp transistor Q_P and diode D_1 can be changed by tapping the voltage at different point of R_{C2} (instead of connecting the emitter of the pnp transistor Q_P to Node $\bar{C}$ as shown in Fig. 1(c)).

Combination of this direct-coupled pnp pull-up scheme with a Darlington-like active-pull-down stage (transistor Q_D) [4] results in a complementary push–pull configuration as shown in Fig. 1(c).

TABLE I
TYPICAL DEVICE PARAMETERS AT 0.8-μm DESIGN RULE

Device	npn	pnp
Design Rule	0.80 μm	0.80 μm
A_E (Wafer, μm^2)	0.50 × 4.0	0.50 × 4.0
Base Transit Time	6.0 ps	6.0 ps
C_{EB}	6.6 fF	16 fF
C_{CB}	3.9 fF	14 fF
C_{CS}	12 fF	9.3 fF
R_E	14 Ω	15 Ω
R_{BX}	164 Ω	82 Ω

III. CIRCUIT PERFORMANCE

The performance of the circuit is assessed based on a 0.8-μm double-poly self-aligned complementary bipolar process [5], [6] with typical measured device parameters listed in Table I. Both npn and pnp parameters have been calibrated against the conventional ECL circuits. Fig. 2 compares the net pull-up and pull-down current of the present circuit and the conventional ECL circuit for a loaded gate (FI/FO = 3, C_L = 0.3 pF) at a power consumption of 1.0 mW/gate. Clearly, the present circuit offers much larger and sharper pull-up and pull-down current during the switching transient. The delay in this case is 104 ps for the present circuit, representing a 2.0X improvement over the 208 ps for the conventional ECL circuit. The input/output voltage waveforms and the current through the pull-up pnp transistor during the switching transient are shown in Fig. 3(a) and 3(b), respectively. The large pull-up current spike through the pnp transistor can be clearly seen (Fig. 3(b)). Also, notice that the entire pnp current waveform is consistent with the circuit operation described in the previous section.

Fig. 4 shows the pull-up currents through the pnp transistor ($I_{C,Qp}$) and the emitter-follower transistor ($I_{E,Qu}$) in expanded time scale. While the peak current through the emitter-follower transistor is only slightly less than that through the pnp transistor, the presence of a high dc current component (about half the peak value) renders the available charging current (the current above dc component) through the emitter-follower much smaller than that through the pnp transistor. The pull-up delay, therefore, is almost completely determined by the transient current through the pnp transistor, and the collector load resistor R_C is used merely for setting the final output voltage level through the emitter-follower transistor as in the AC-PP-ECL circuit [1], [2].

The power-delay characteristics for the conventional ECL circuit, the AC-PP-ECL circuit, and the present circuit at 0.8

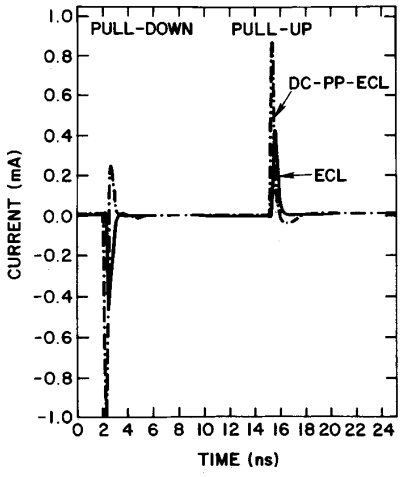


Fig. 2. Net pull-up and pull-down currents during the switching transient for the conventional ECL circuit and DC-PP-ECL circuit. (0.8 μm design rule, FI/FO = 3, C_L = 0.3 pF, 1.0 mW/gate).

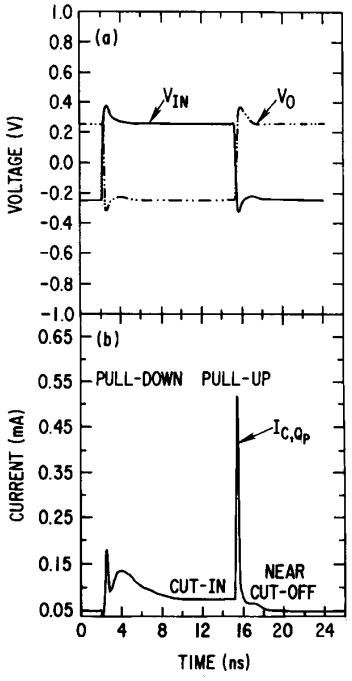


Fig. 3. Pertinent waveforms during the switching transient for DC-PP-ECL circuit. (a) Input and output voltage waveforms, and (b) current through the pull-up pnp transistor Q_P. (0.8 μm design rule, FI/FO = 3, C_L = 0.3 pF, 1.0 mW/gate).

μm design rule are shown in Fig. 5. For the unloaded case (FI/FO = 1, Fig. 5(a)), the speed improvement at 1.0 mW/gate is 32% with respect to ECL and 11.1% with respect to AC-PP-ECL (47 ps for ECL, 36 ps for AC-PP-ECL, and 32 ps for present circuit). The improvement with respect to the AC-PP-ECL circuit comes mainly from the elimination of the biasing circuit (and power) for the push–pull transistors in the present

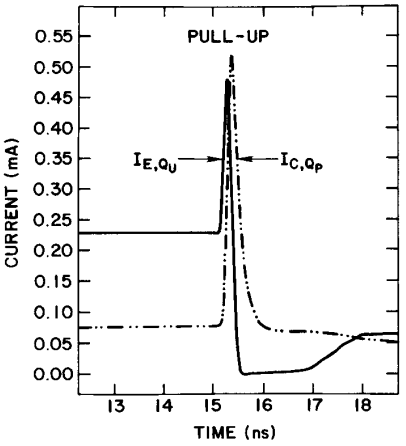


Fig. 4. The pnp pull-up current (I_{C,Q_P}) and the emitter-follower pull-up current (I_{E,Q_U}) during the switching transient in expanded time scale. (0.8 μm design rule, FI/FO = 3, C_L = 0.3 pF, 1.0 mW/gate).

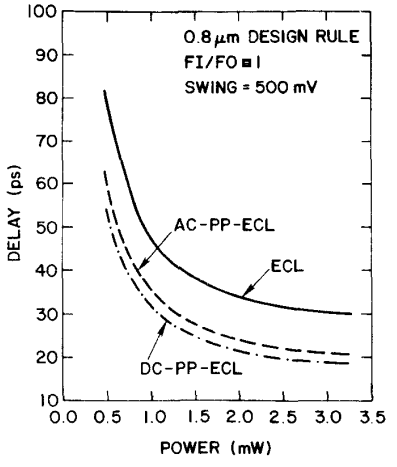
circuit. For the loaded case (FI/FO = 3, C_L = 0.3 pF, Fig. 5(b)), delay improvement of 2.2X at 0.5 mW/gate (364 ps for ECL, 174 ps for AC-PP-ECL, and 168 ps for present circuit) and 1.86X at 3.0 mW/gate (104 ps for ECL, 65 ps for AC-PP-ECL, and 56 ps for present circuit) are achieved compared with the conventional ECL circuit.

The superior load driving capability of the present circuit is illustrated in Fig. 6. At 0.8 μm design rule with FI/FO = 3 and 1.0 mW/gate, the circuit achieves a driving capability of 158 ps/pF, a 2.2X improvement over the 351 ps/pF for the conventional ECL circuit.

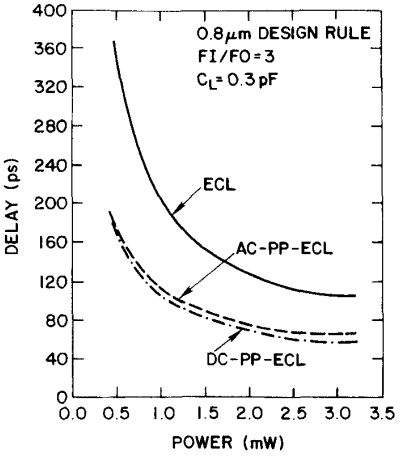
IV. Discussion

The pull-up delay path of the present circuit is from the input to the common-emitter node of the switching transistors (Node A in Fig. 1(c)), and then through the pnp pull-up transistor Q_P to the output node. Thus, the collector load resistor R_C is completely decoupled from the pull-up delay path. Large resistor value, hence small switching current, can be used without degrading the pull-up switching speed.

For the output pull-down transition, notice that in the conventional ECL circuit, the voltage at the output node falls only after the voltage at Node C does, and the process is sequential. The net output pull-down current (the difference between the current flowing through the emitter-follower resistor and the current supplied by the emitter follower transistor) is "zero" until the voltage at Node C starts to fall. In the present circuit scheme, the voltage at Node A follows the input once the input crosses the reference voltage, providing a transient over-drive at the base of Q_D and hence a large dynamic current for fast pull-down of the output node. This large dynamic pull-down current is supplied earlier compared with the conventional ECL circuit, and the output voltage falls almost simultaneously with the voltage at Node C, thus improving the pull-down delay. The present circuit scheme also allows a small standby current in the output stage to reduce power consumption without degrading the pull-down switching speed.



(a)



(b)

Fig. 5. (a) Unloaded (FI/FO = 1), and (b) loaded (FI/FO = 3, C_L = 0.3 pF) power-delay characteristics for the conventional ECL circuit, AC-PP-ECL circuit, and DC-PP-ECL circuit at 0.8 μm design rule.

Looking from the common-emitter Node A, both the pull-up circuit (Q_P, R_{C2}, and C_U) and the pull-down circuit (Q_D, R_D, and C_D) resemble the front-end of an NTL circuit. Hence, NTL-like speed and noise immunity are expected for the present circuit. Furthermore, since the over-drive of the pull-down npn transistor Q_D during the output pull-down transition is ΔV/2, while the over-drive for the pull-up pnp transistor Q_P during the output pull-up transition is only ΔV/4 (as explained in Section II), the speed-up capacitor C_U has to be larger than C_D to ensure a better balance between the pull-up and pull-down delay.

Compared with the conventional ECL circuit, the implementation of the present circuit scheme requires two more transistors (Q_P and Q_D) and two more capacitors (C_U and C_D) (see Fig. 1(c)). The two extra transistors normally do not have significant impact on the cell size since the ECL

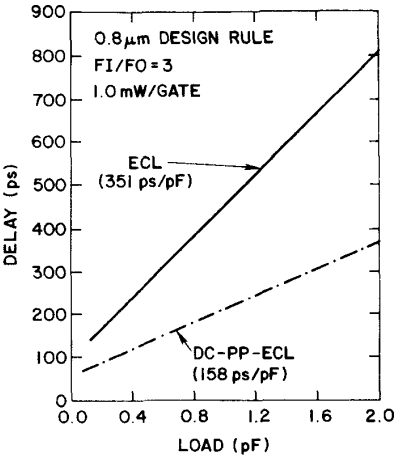


Fig. 6. Delay versus capacitive loading for the conventional ECL circuit and DC-PP-ECL circuit. (0.8 μm design rule, FI/FO = 3, 1.0 mW/gate).

gate array, in general, is not dense. Typical values for R_{C2} and R_D are in the normal resistance value range used in the conventional ECL circuit (R_{C2} and R_D are about 2.3 KΩ and 1.10 KΩ for a loaded gate at 1.0 mW/gat), and therefore do not cause any implementation problem. The values of the capacitors C_U and C_D are chosen according to the loading condition to optimize performance. These capacitance values should be comparable to the loading capacitance (typically several tenths of a pF) at the output node to have significant speed-up effect. Depending on how the capacitor is implemented (thin dielectric capacitor with high capacitance per unit area, or junction capacitor with low capacitance per unit area), the impact on cell area may range from 10% to 20%.

V. Conclusion

In summary, we have described a new direct-coupled complementary push–pull ECL circuit. The circuit utilizes a direct-coupled pnp pull-up scheme to decouple the collector load resistor from the delay path. The superior power-delay performance and load driving capability of the circuit were illustrated and the design considerations of the circuit discussed.

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