Series-Parallel Association of FET's for High Gain and High Frequency Applications

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***Abstract*—This paper presents a simple approach in the design of composite field effect transistors with low output conductance. These transistors consist of the series association of two transistors, with the transistor connected to the drain terminal wider than the transistor connected to the source terminal. It is shown that this composite transistor has the same dc characteristics as a long-channel transistor of uniform width. A composite transistor has two main advantages over its "dc equivalent" transistor of uniform width: significant area savings and a higher cutoff frequency. The main application is low-voltage, high-frequency analog circuits. The proposed technique is particularly suited for analog design in gate arrays.**

I. Introduction

THE MOS technology has proved to be well-suited for the implementation of mixed analog-digital systems. The growing trend towards smaller feature sizes and, consequently, lower supply voltages, leads to new challenges in the design of analog VLSI circuits [1]. A basic problem to be solved is the design of high-gain single-stage amplifiers [2]. High-gain amplifiers are typically obtained using long-channel transistors and/or cascode structures [3]. However, the transistor cutoff frequency is inversely proportional to the square of the channel length [4]. This property restricts the long-channel solution to low frequency applications. On the other hand, cascoding transistors results in a loss in linear output swing for the amplifier [3].

In this paper we propose a structure that has been inspired by a 1984 paper by Riccó [12]. This structure consists of the series association of two transistors where the transistor connected to the drain terminal is wider than the transistor connected to the source terminal. This composite transistor has a transconductance-to-output conductance ratio as high as that of a long-channel transistor but a shorter "physical channel length." Hence, the composite transistor has a cutoff frequency higher than the cutoff frequency of its dc equivalent long-channel transistor. Therefore, the design of high-frequency, low-voltage simple analog sections [5] can benefit from the high attainable dc gain and high cutoff frequency of composite transistors. Moreover, composite transistors can be used for gate array implementation of analog sections in combined analog-digital circuits [6]–[8]. Two decisive advantages of composite transistors for gate array design are significant area savings and simple modeling.

This paper describes the electrical performance of composite transistors as well as a set of equations for design purposes. The dc characteristics of composite transistors for both the triode and saturation regions are presented in Section II. Their dynamic behavior is analyzed in Section III. Experimental results for various prototypes of composite transistors are presented in Section IV while the conclusions are stated in Section V.

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II. DC Characteristics of Composite MOS Transistors

In this section, we demonstrate the dc equivalence between series connectedand single transistors. Consider the series association shown in Fig. 1, which will be called a composite transistor in the text that follows. The gate and bulk terminals are common to both transistors. The channel lengths L_S and L_D are equal to or longer than the minimum length provided by the technology. We assume the gates of transistors M_S and M_D have rectangular geometries. This assumption does not represent any serious practical limitation because the rectangular geometry is the prevalent in VLSI layouts.

A. Triode Region

In the triode region, using the gradual channel approximation, the drain current of an MOS transistor can be written [4], [9] as:

$$I_D = \frac{W}{L}[g(V_G, V_S) - g(V_G, V_D)] \tag{1}$$

where all voltages are referred to the substrate, emphasizing the symmetry between drain and source. W and L are the channel width and channel length, respectively and $g(V_G, V)$ is a function that describes the dc behavior of the MOS transistor, including body effect and mobility reduction. Secondary effects in the triode region such as drain-induced barrier lowering and velocity saturation [4], which can have some influence on the drain current, have not been included in the analysis that follows. Actually, the secondary effects do not necessarily have a significant influence in the triode region, as shown in the experimental section of this paper.

For the series connection of transistors (Fig. 1), assuming the drain voltage V_D is such that transistor M_D is biased in the triode region and the drain currents of M_S and M_D are

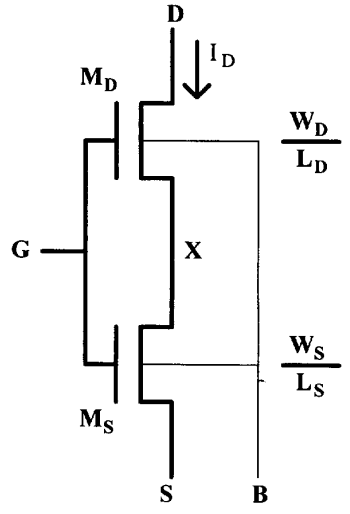


Fig. 1. Composite transistor.

equal, one obtains

$$g(V_G, V_X) = \frac{\left(\frac{W}{L}\right)_S g(V_G, V_S) + \left(\frac{W}{L}\right)_D g(V_G, V_D)}{\left(\frac{W}{L}\right)_S + \left(\frac{W}{L}\right)_D} \tag{2a}$$

from the application of (1) for both transistors. It should be pointed out that the value of function $g(V_G, V_X)$ at the intermediate node X is the mean value of the values of $g(V_G, V)$ at the source and drain terminals of the composite transistor. From (1) and (2a) the drain current in the composite transistor is

$$I_D = \left(\frac{W}{L}\right)_{eq} [g(V_G, V_S) - g(V_G, V_D)] \tag{2b}$$

where

$$\left(\frac{W}{L}\right)_{eq} = \frac{\left(\frac{W}{L}\right)_D \left(\frac{W}{L}\right)_S}{\left(\frac{W}{L}\right)_D + \left(\frac{W}{L}\right)_S}. \tag{2c}$$

In the triode region, the composite transistor has a dc behavior equal to that of a single transistor whose aspect ratio is given by (2c). Hence, the geometric composition rule for the series connection of linear resistors (with the same sheet resistance) is also applicable to series-connected transistors [10].

On the verge of saturation the drain voltage is equal to the pinch-off voltage V_P, defined by the relation $g(V_G, V_P) = 0$. Obviously, the saturation voltage V_P is equal for transistors M_S, M_D and also for the series composition of M_S and M_D. Hence, (2a) and (2b) reduce to:

$$g(V_G, V_X) = \frac{g(V_G, V_S)}{1+m} \tag{3a}$$

$$I_D = \frac{m}{1+m}\left(\frac{W}{L}\right)_S g(V_G, V_S) \tag{3b}$$

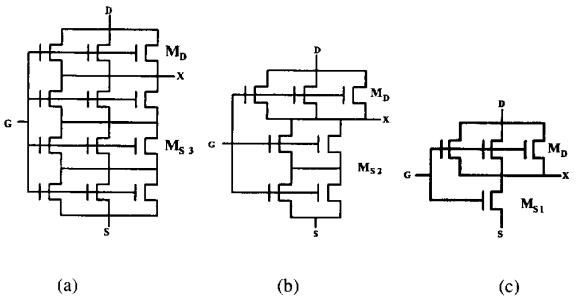


Fig. 2. Arrays of unit transistors with the same drain width($W_D = 3W_u$) and the same aspect ratio $(W/L)_{eq} = 3/4$. (a) $(L/W)_{eq} = 3L_u/3W_u + L_u/3W_u$, (b) $(L/W)_{eq} = 2L_u/2W_u + L_u/3W_u$, (c) $(L/W)_{eq} = L_u/W_u + L_u/3W_u$.

where m is the quotient of the aspect ratios

$$m = \frac{(W/L)_D}{(W/L)_S}. \tag{3c}$$

From (3a), if M_S and M_D have equal channel lengths but M_D is much wider than M_S, then $g(V_G, V_X)$ tends towards zero, i.e., the voltage at node X tends towards the pinch-off voltage. Hence, the aspect ratio of the composite transistor equals $(W/L)_S$ and the current density in transistor M_D is much lower than in transistor M_S.

Obviously, the results of this section can be extended to a series association of any number of transistors and to the association of unit transistors in a rectangular array such as the one shown in Fig. 2(a). The aspect ratio of this type of array is equal to the aspect ratio of the unit transistor multiplied by the number of parallel-connected transistor and divided by the number of series-connected transistors. Transistors M_S and M_D (Fig. 1) of different widths and lengths can be implemented with rectangular arrays, as shown in Fig. 2. Arrays of unit transistors are useful either for gate array design [6]–[8] or in precision analog circuits [2].

B. Saturation Region

In this section we demonstrate that the equivalence of any composite transistors in the triode region is extended to the saturation region if the composite transistors have, in addition to the same aspect ratio, the same channel width at the drain end. These two conditions are fulfilled by the composite transistors illustrated in Fig. 2. In these arrays, transistor M_D, identical for the three structures, is the transistor connected between nodes X and D. Transistors M_{S1}, M_{S2} and M_{S3}, connected between nodes X and S, have the same aspect ratio but different channel lenghts.

The behavior of these composite transistors in saturation can be better understood with the aid of Fig. 3, which presents the classical determination of the operating point [11] from the output characteristics of transistors M_{S1}, M_{S2}, M_{S3} and from the load curve that represents transistor M_D. The difference in the two load curves shows that transistor M_D, which operates in the saturation region, presents a high output conductance. The near coincidence of the output characteristics of M_{S1}, M_{S2}, and M_{S3} in the triode region indicates, that

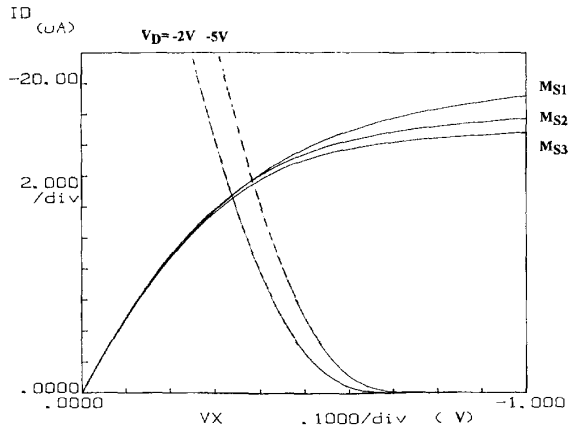


Fig. 3. Output characteristics of transistors M_{S1}, M_{S2}, M_{S3} and load curve due to transistor M_D from Fig. 2 at $V_G = -1.8$ V.

transistors with the same aspect ratio have the same dc characteristics in this region despite the existence of short-channel effects. As expected, the operating point for the M_S transistors is in the triode region even if M_D is in the saturation region. Hence, the drain currents of the composite transistors of Fig. 2 in saturation and, consequently, their output conductances are approximately equal. Even though these conclusions have been reached through the analysis of an example, it should be clear that they can be extended to any composite transistors satisfying the trivial geometrical constraints enunciated at the beginning of this section.

For simplicity, we name two (composite) transistors as dc equivalent if they have the same dc current for the same bias. Generally, a composite transistor is not equivalent to itself if drain and source are interchanged [12]. Therefore, source and drain terminals should be physically identified.

Summarizing, any composite transistors with the same technological parameters are dc equivalent if they have:

1) the same aspect ratio,
2) the same channel width at the drain end, and
3) equal short-channel effects in the triode region (for both M_S and M_D).

From conditions (i) and (ii), the "dc equivalent" electrical width and length of the composite transistor can be easily derived:

$$W_{eq} = W_D \tag{4a}$$

and from (2c) it follows that

$$L_{eq} = L_D + mL_S. \tag{4b}$$

Therefore, in order to obtain a composite transistor equivalent to a long-channel transistor, we should choose a transistor with $m > 1$, i.e., a composite transistor wider at the drain end than at the source end. The conventional way to obtain a low output conductance by means of a rectangular long-channel transistor reduces the electrical field along the whole transistor channel, giving rise to a long transit time, as shown in the next section. (4b) shows that a composite transistor

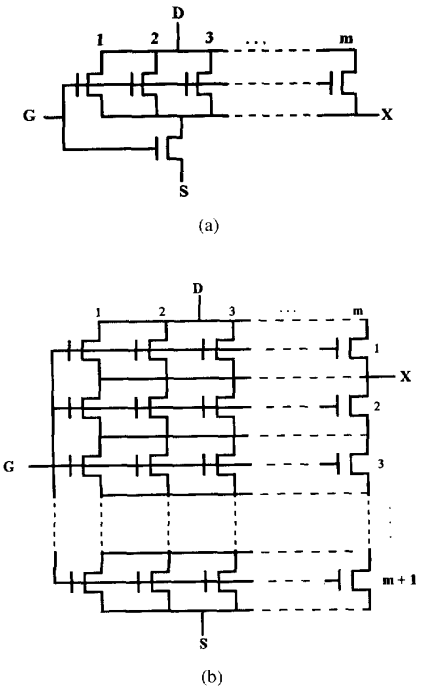


Fig. 4. Composite transistors: (a) Trapezoidal type composite transistor (T_m-transistor) $(L/W)_{eq} = L_u/W_u + L_u/mW_u$. (b) Rectangular type composite transistor (R_m-transistor) $(L/W)_{eq} = mL_u/mW_u + L_u/mW_u$.

equivalent to a long-channel transistor can be obtained from the series association of two minimum length transistors.

Fig. 4 shows an example of two dc equivalent arrangements of unit transistors. The trapezoidal transistor (T-transistor), whose drain end is wider than the source end, has the same aspect ratio and the same drain width as the rectangular transistor (R-transistor).

It should be noticed that the dc equivalence of transistors does not depend on the physical mechanisms of conduction provided the short-channel effects in the triode region are roughly the same (condition (iii)). This condition has been verified for transistors with minimum channel length in a 1.2-μm standard CMOS process. Even if condition (iii) is not satisfied, the composite transistor wider at the drain end has a low output conductance in saturation due to the lower current density at the drain side.

III. Transit Time

In this section we include an analysis concerning the dynamic behavior of the MOS composite transistor.

Usually, the transistor response to dynamic signals is characterized by the transit time (τ) and/or the intrinsic cutoff frequency (ω_T). For the saturated MOS transistor in strong inversion these two parameters are related [4] by

$$\tau\omega_T = 2. \tag{5a}$$

We demonstrate in Appendix A that (5a) is also approximately valid for a composite transistor.

The transit time in an MOS transistor is given [4] by:

$$\tau = \frac{Q_I}{I_D} \tag{5b}$$

where Q_I is the total inversion charge.

Therefore, the transit time in a composite transistor is

$$\tau = \frac{Q_{IS} + Q_{ID}}{I_D} \tag{5c}$$

where Q_{IS} and Q_{ID} are the total inversion charges in the transistors connected to the source and drain terminals, respectively. We calculate the drain current for the MOS transistor in strong inversion using the expressions from [2], [14]:

$$g(V_G, V) = \frac{\mu C'_{ox}}{2} n[V_P(V_G) - V]^2 \tag{6a}$$

where

$$V_P(V_G) \cong \frac{V_G - V_{TO}}{n} \tag{6b}$$

μ is the carrier mobility in the channel, C'_{ox} the gate capacitance per unit area, n the slope factor, which allows modeling the body effect, and V_{TO} the gate threshold voltage for the channel at equilibrium. All voltages are referred to the bulk. From (3) and (6) we determine the voltage at node X and the drain current in saturation

$$V_P - V_X = \frac{V_P - V_S}{\sqrt{1+m}} \tag{7a}$$

$$I_D = \frac{\mu C'_{ox} m W_S}{2(1+m)L_S} n(V_P - V_S)^2. \tag{7b}$$

On the verge of saturation, the drain voltage is equal to the pinch-off voltage V_P. The inversion charges [2], [13] are

$$Q_{IS} = \frac{2}{3} W_S L_S n C'_{ox} \frac{(V_P - V_S)^3 - (V_P - V_X)^3}{(V_P - V_S)^2 - (V_P - V_X)^2} \tag{7c}$$

$$Q_{ID} = \frac{2}{3} W_D L_D n C'_{ox} (V_P - V_X). \tag{7d}$$

We compute the transit time in the saturation region from (5c) and (7). For the MOS device shown in Fig. 4(a), the transit time is

$$\tau = \tau_u \left\{ \left[\left(1 + \frac{1}{m}\right)^2 - \frac{\sqrt{1+m}}{m^2} \right] + \sqrt{1+m} \right\} \tag{8a}$$

$$\tau_u = \frac{4L_u^2}{3\mu(V_P - V_S)}. \tag{8b}$$

In the previous analysis we have assumed that the transistors connected to thesource and drain terminals have the minimum channel length, equal to L_u, provided by the technology. In this case, m is the ratio W_D/W_S and τ_u is the transit time of the minimum-length transistor. In (8a) the first term, between square brackets, represents the transit time of the transistor connected to the source terminal while the second term is associated to the transit time of the transistor connected to the drain terminal. For high values of m, (8a) becomes

$$\tau \cong \tau_u \{1 + \sqrt{1+m}\}. \tag{8c}$$

The increase in the transit time for increasing values of m is due to the reduction of the electrical field in the channel of the composite transistor at the drain side. In fact, the electrical field at the channel of M_D decreases with the square-root of m, as can be inferred from (7a).

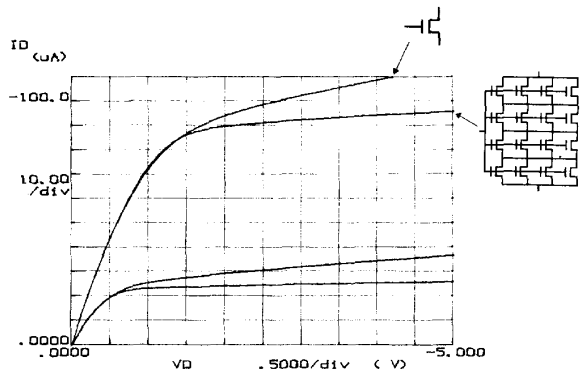


Fig. 5. Dc output characteristics of a unit transistor (W_u/L_u) and of a square composite transistor ($4W_u/4L_u$), $L_u = 1.2\,\mu$m, $W_u = 3\,\mu$m.

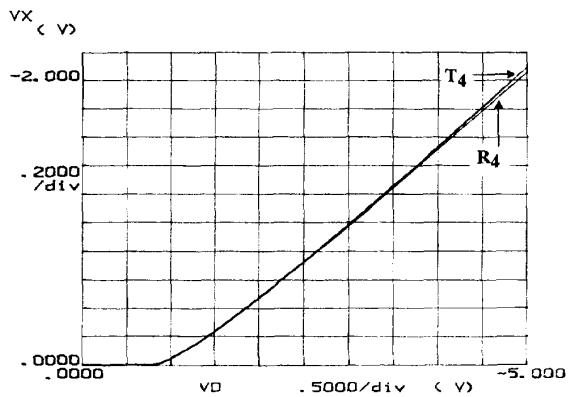
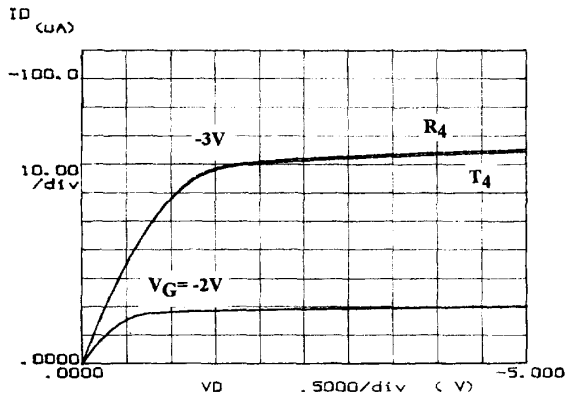


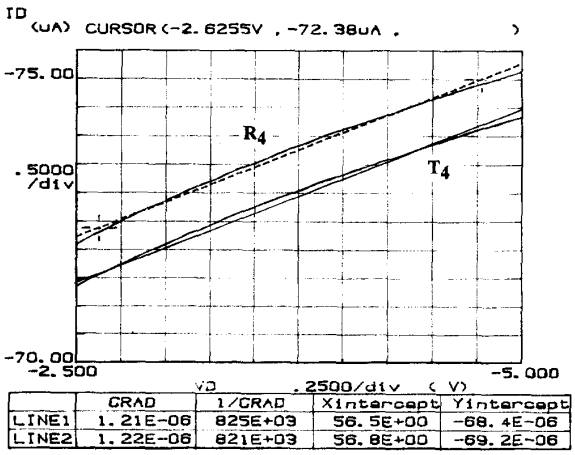
Fig. 6. Voltages at internal nodes X of the composite rectangular (R_4) and trapezoidal (T_4) transistors for $V_D = V_G$, with m, the number of parallel transistors at the drain side, equal to 4.

IV. Experimental Results

In order to demonstrate the theoretical results, arrays of transistors of minimum channel-length in a 1.2-μm CMOS n-well process ($V_{TN} = 1.1$ V, $V_{TP} = -0.7$ V) have been built. Fig. 5 shows the dc output characteristics of a single transistor and of a square array of transistors. Their equivalence in the triode region confirms that short-channel effects are negligible in this region. Indeed, the difference in the output conductances is evident. Fig. 6 displays the plots of the internal voltages V_X for the R-transistor and the T-transistor from Fig. 4, at $V_D = V_G$. Fig. 7 shows the output characteristics of the two arrays of transistors in Fig. 4. These characteristics are almost coincident, especially the output conductances in the saturation region. Hence, in spite of having a shorter physical channel, the T-transistor is dc equivalent to the R-transistor. The plots of the attainable low frequency gains (g_m/g_o) for both p and n-channel integrated composite transistors are presented in Fig. 8. Voltage gains up to 60 dB are attainable with a



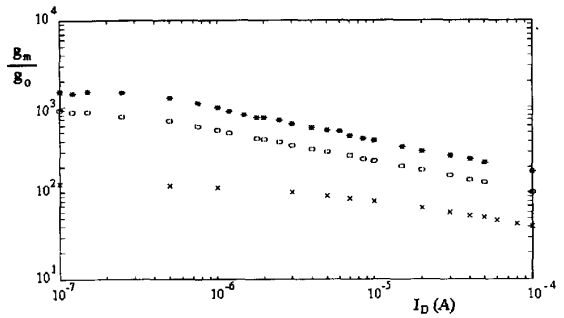
(a)



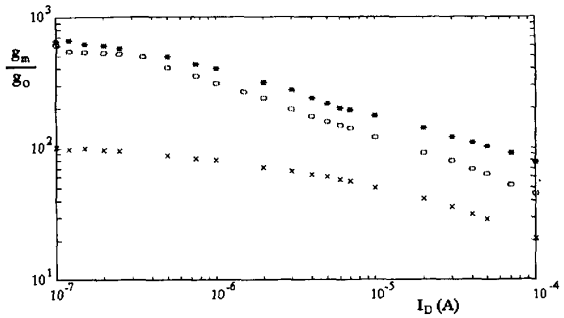
	GRAD	1/GRAD	Xintercept	Yintercept
LINE1	1.21E-06	825E+03	56.5E+00	-68.4E-06
LINE2	1.22E-06	821E+03	56.8E+00	-69.2E-06

(b)

Fig. 7. (a) Dc characteristics of the composite rectangular (R_4) and trapezoidal (T_4) transistors. (b) Detail in the saturation region for $V_G = -3$ V. The slopes of the straight lines represent the mean values of the output conductances.



(a)



(b)

Fig. 8. Attainable low frequency gain (g_m/g_o) for the unit transistor ($L_u = 1.2\,\mu$m) and in composite transistors: x, unit transistor; o, trapezoidal transistor T_3; *, trapezoidal transistor T_9. (a) n-channel. (b) p-channel.

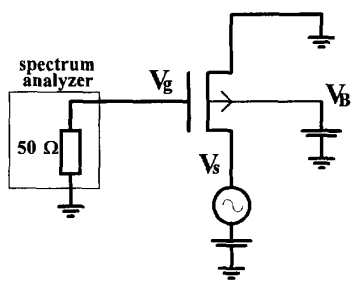


Fig. 9. Circuit to measure the gate-to-source capacitance.

single stage of n-channel composite transistors, as shown in Fig. 8(a). Therefore, very high-gain amplifiers can be achieved by a single cascode stage of composite transistors.

As a means to verify experimentally the dependence of the transit time on the drain width (8a) we have written the normalized transit time (Appendix A) in strong inversion as:

$$\frac{\tau}{\tau_u} = \frac{g_{mu}}{g_m}\frac{C_{gs}}{C_{gsu}} \tag{9}$$

where $Cgs(Cgsu)$ and $g_m(g_{mu})$ are the intrinsic gate-to-source capacitance and the small-signal gate transconductance of the composite (unit) transistor.

In order to measure the normalized transit time, we have built composite transistors with p-channel devices of the $C4007$ off-the-shelf circuit because of the very small capacitance of the available integrated transistors. We have determined the transit time for composite transistors that consist of a single transistor connected to the source end and m parallel-connected transistors to the drain side. The values of the transconductances have been measured in a semiconductor parameter analyzer while the capacitances have been measured according to the scheme shown in Fig. 9. The experimental results obtained from the circuit in Fig. 9 for both a T-transistor and its dc equivalent uniform-width transistor are shown in Fig. 10. The capacitive coupling and, in consequence, the transit time in the R-transistor is about 6 times larger than in the T-transistor.

Fig. 11 exhibits the normalized transit time of the composite transistor in terms of m, the number of unit transistors connected to the drain terminal. The transit time depends weakly on m, in particular for low values of m. As an example of the usefulness of the composite transistor, let us compare some properties of the dc equivalent transistors T_9 and R_9. The area of R_9 is 9 times larger than the area of T_9 and the transit

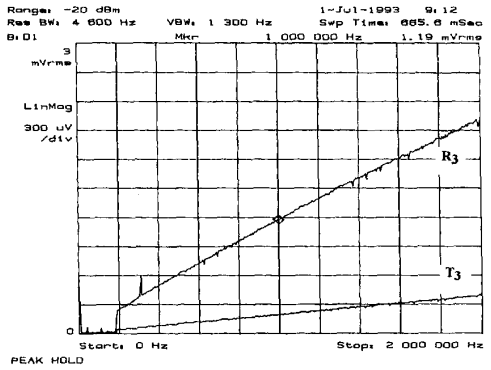


Fig. 10. Experimental results for the gate-to-source transadmittance in the rectangular (R_3) and trapezoidal (T_3) transistors $V_{DB} = V_{GB} = -3$ V, $V_{SB} = 0$ V.

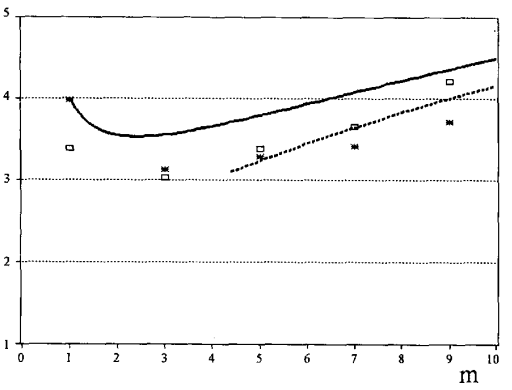


Fig. 11. Normalized transit time of theT_m-transistor (m is the number of parallel-connected transistors at the drain side): _____ theoretical; ----, asymptotic curve for high values of m; □, experimentally determined at $V_{GS} = -2$ V; *, experimentally determined at $V_{GS} = -3$ V.

time of R_9 is roughly 25 times longer than the transit time of T_9 (Fig. 11).

The transistors employed for the transit time determination have large overlap capacitances. However, the effect of these overlap capacitances on the total gate-to-source capacitance varies in almost the same proportion as the intrinsic gate-to-source capacitances, as shown in Appendix B. Hence, the ratio $Cgs/Cgsu$ in (9) is little affected by the extrinsic overlap capacitances.

Up to now we have considered only the transit time to analyze the dynamic behavior of the composite transistor. However, the effects of the gate-to-drain overlap capacitance should be taken into account for a specific design. In fact, increasing the number of parallel-connected transistors at the drain end increases simultaneously the transit time and the capacitances related to the drain terminal.

V. Conclusions

We have proposed a method to design composite transistors by the series-parallel association of single transistors.

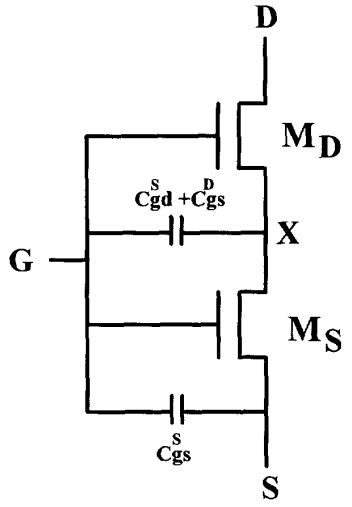


Fig. 12. Intrinsic capacitances in the composite transistor for the evaluation of the intrinsic gate-to-source capacitance.

The composite transistor has the high transconductance-to-output conductance ratio of a long-channel transistor with a reduced area and a higher cutoff frequency. Hence, composite transistors are very useful for the design of simple scheme analog sections for high-speed and low-voltage applications. Composite transistors also provide a natural solution for gate array design of analog circuits.

VI. Appendix A

Intrinsic Cutoff Frequency of the Composite Transistor

The gate-to-source capacitance C_{gs} is defined as [4], [13]:

$$C_{gs} = -\left.\frac{\partial Q_G}{\partial V_S}\right|_{V_G, V_D} \tag{A1}$$

Using (A1) and the quasi-static operation approximation [4], the gate-to-source capacitance of the composite transistor (Fig. 12) can be written in terms of the gate capacitances of M_S and M_D as:

$$C_{gs} = C_{gs}^S + \frac{dV_X}{dV_S}(C_{gd}^S + C_{gs}^D) \tag{A2}$$

where C_{gs}^S and C_{gd}^S are the gate-to-source and gate-to-drain capacitances of transistor M_S and C_{gs}^D is the gate-to-source capacitance of transistor M_D.

In strong inversion, the expressions for gate-to-source and gate-to-drain capacitances of a rectangular transistor are [13]:

$$C_{gs} = \frac{2}{3}C_{ox}\left[1 - \frac{(V_P - V_D)^2}{(2V_P - V_S - V_D)^2}\right] \tag{A3}$$

$$C_{gd} = \frac{2}{3}C_{ox}\left[1 - \frac{(V_P - V_S)^2}{(2V_P - V_S - V_D)^2}\right] \tag{A4}$$

where $C_{ox} = C'_{ox}WL$. We compute the gate-to-source capacitance C_{gs} of the composite transistor biased at saturation from (A2) to (A4) with V_X and its derivative with respect to

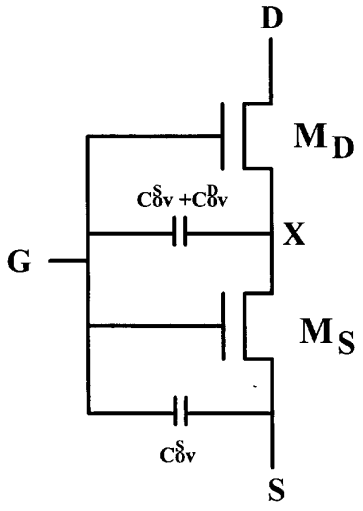


Fig. 13. Overlap capacitances in the composite transistor for the evaluation of the extrinsic gate-to-source capacitance.

V_S determined from (7a). In the case of practical interest, $L_S = L_D = L_u$, the gate-to-source capacitance of the saturated composite transistor is given by

$$C_{gs} = \frac{2}{3}C'_{ox}W_S L_u \left[1 - \frac{\frac{1}{1+m} + \frac{1}{\sqrt{1+m}}}{\left(1 + \frac{1}{\sqrt{1+m}}\right)^2} + \sqrt{1+m}\right]. \tag{A5}$$

The intrinsic cutoff frequency is calculated [4] from

$$\omega_T = \frac{g_m}{C_{gs} + C_{gb}} \cong \frac{g_m}{C_{gs}}. \tag{A6}$$

From (A5) and (A6), after some algebra, it follows that

$$\frac{1}{\omega_T} \cong \frac{C_{gs}}{g_m} = \frac{2L_u^2}{3\mu(V_P - V_S)} \cdot \left[\left(1 + \frac{1}{m}\right)^2 + \left(1 - \frac{1}{m^2}\right)\sqrt{1+m}\right]. \tag{A7}$$

Therefore, (9) results from the comparison between (A7) and (8a).

VII. Appendix B

Effects of the Overlap Capacitances on the Gate-to-Source Capacitance of the Composite Transistor

Using the quasi-static operation approximation as in Appendix A, it follows (Fig. 13):

$$C_{ov} = C^S_{ov} + \frac{dV_X}{dV_S}(C^S_{ov} + C^D_{ov}) \tag{B1}$$

where C_{ov} is the equivalent extrinsic gate-to-source capacitance due to overlap capacitances C^S_{ov} and C^D_{ov} of transistors M_S and M_D. For $L_S = L_D$, it is readily verified that $C^D_{ov} = mC^S_{ov}$. Hence:

$$C_{ov} = C^S_{ov}(1 + \sqrt{1+m}). \tag{B2}$$

(B2) shows the same law for the extrinsic gate-to-source capacitance as that of the asymptotic behavior of the transit time for high values of m (8c).

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References

[1] P. E. Allen, "Future of analogue integrated circuit design," in *Analogue IC design: The Current-Mode Approach*, C. Toumazou, F. J. Lidgey and D. G. Haigh, Eds. London: Peter Peregrinus Ltd., 1990.
[2] E. Vittoz, "MOS transistor," Intensive Summer Course on CMOS VLSI Design, Analog & Digital, Lausanne (EPFL), Switzerland, 1989.
[3] P. J. Crawley, G. Roberts, "Designing operational transconductance amplifiers for low voltage operation," in *Proc. IEEE Int. Symp. on Circuits and Syst.*, Chicago, Il., May 1993, pp. 1455–1458.
[4] Y. P. Tsividis, *Operation and Modeling of the MOS Transistor*. McGraw Hill, New York, 1987.
[5] L. Moore, R. S. Soin, F. Maloberti, "Mixed analogue digital ASICs–circuit techniques, design tools and applications," Workshop on Analogue-Digital ASIC's, 5th Annual IEEE Int. ASIC Conf. and Exhibit, Rochester, NY, 1992.
[6] S. Masuda *et al.*, "A CMOS analog and digital masterslice LSI," in *ISSCC Dig. Tech. Papers* , 1987, pp. 146–147.
[7] P. Duchene and M. J. Declercq, "A highly flexible sea-of-gates structure for digital and analog applications," *IEEE J. Solid-State Circuits*, vol. 24, no. 3, pp. 576–584, June 1989.
[8] S. Kawada *et al.*, "1.5-μm CMOS gate arrays with analog/digital macros designed using common base arrays," *IEEE J. Solid-State Circuits*, vol. 24, no. 4, pp. 985–990, August 1989.
[9] H. Wallinga and K. Bult, "Design and analysis of CMOS analog signal processing circuits by means of a graphical MOST model," *IEEE J. Solid-State Circuits*, vol. 24, no. 3, pp. 672–680, June 1989.
[10] E. Vittoz and X. Arreguit, "Linear networks based on transistors," *Electron Lett.*, vol. 29, no. 3, pp. 297–299, Feb. 1993.
[11] A. S. Sedra and K. C. Smith, *Microelectronic Circuits*, 2nd. Ed. Fort Worth: Holt, Rinehart and Winston, 1987.
[12] B. Riccó, "Effect of channel geometries on FET output conductance in saturation," *IEEE Electron Device Lett.*, vol. 5, no. 9, pp. 353–356, Sept. 1984.
[13] C. C. Enz, "High precision CMOS micropower amplifiers," Ph.D. thesis no. 802, EPF-Lausanne, Switzerland, 1989.
[14] E. Vittoz, "Very low power circuit design: Fundamentals and limits," in *Proc. IEEE Int. Symp. Circuits and Syst.*, Chicago, IL, May 1993, pp. 1439–1442.

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