Switched-Current Memory Circuits for High-Precision Applications

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***Abstract*—We discuss circuit parameters that limit the precision of basic dynamic current-memory cells. In addition to analyzing current-copying errors caused by the finite output conductances of the current sources and by the clock-feedthrough (CFT) of the feedback switches, we analyze the noise performance of the basic memory cell. To reduce CFT and noise, we propose a novel circuit based on Miller capacitance-enhancement. Measurement results of memory cells integrated in a 1-μm CMOS process confirm the theoretical findings; with our CFT and noise reduction technique based on Miller enhanced capacitance and dummy switches, we achieve a dynamic range of 11 b at clock frequencies greater than 100 kHz.**

***Index Terms*— Current memory, switched-current circuits, clock-feedthrough, sampled-data noise, analog integrated circuits.**

I. Introduction

SWITCHED-current (SI) circuits [1], [2] have gained considerable interest for analog sampled-data signal processing. Low power consumption, low supply voltage, potential for high speed, and compatibility with standard CMOS processes are the major advantages of the SI technique over alternative analog-circuit principles. The precision of many SI circuits is, however, quite limited. The main sources of error are device matching and clock-feedthrough (CFT) [3] as well as the finite output impedances of the current sources used in the basic SI memory cells. Many proposals for remedying these nonidealities, mainly with respect to CFT, have been made, cf. [3]–[5].

Most CFT reduction studies consider the so-called current track-and-hold amplifier used extensively in SI-based filter circuits. The use of dummy switches and CFT cancellation techniques is described, for example, in [5]. Even if the CFT problems were completely solved, the precision of this type of SI circuit still suffers from the mismatch of the imbedded transistors, since during track mode the circuit performs as a static current mirror. The precision achievable in VLSI devices is barely sufficient for the building blocks of filter design and is too poor for high precision circuits such as A/D and D/A converters.

Although the approach of the present paper applies to the above-mentioned track-and-hold amplifiers, we concentrate here on a high-precision version of the basic current-memory cell in Fig. 1. Many SI circuits use this building block, which is sometimes called a "current copier" or "dynamic current mirror." Because the performance of the circuit in Fig. 1 does not depend on static element matching, it is potentially well-suited for high-precision applications. CFT and voltage dependence of the involved current sources, however, degrade its performance.

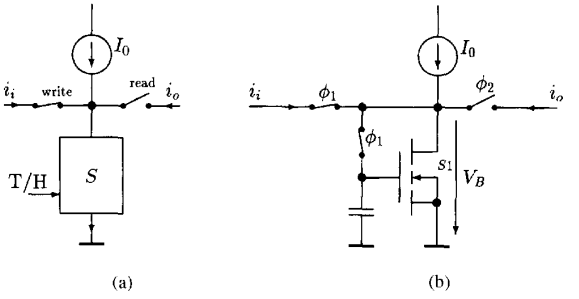

Fig. 1. Basic current-memory cell; (a) principle and symbol, (b) abstract realization. The abbreviation T/H in (a) means a toggle switch for "Track" and "Hold," respectively.

Many proposals exist for the reduction of errors due to the finite output conductance of current sources. Introducing a noninverting amplifier into the feedback path of the track mode, as proposed in [6]–[9], serves to keep the drain voltage of the memory transistor nearly constant in many applications. In some cases, however, a supply-voltage operation of 3 V or less may be precluded.

Several efforts to improve the precision of the basic circuit of Fig. 1 have been reported. Wegmann and Vittoz describe in [10] and [11] an accurate dynamic current mirror with continuous output-current. They eliminate the dependence of the copied current on the mismatch of the transistor pair and achieve a relative precision better than 100 ppm for currents in the range of approximately 0.3 μA. Because CFT still limits the achieved performance, their circuit uses additional gate-to-source capacitors of 5 pF and a relatively low switching slope, which limits the clock-frequency to about 1 KHz. Hughes *et al.* [12] propose a circuit, which they call S^2I, to reduce CFT and the influence of the current-source output resistances. The S^2I circuit exploits the fact that the current source I_0 of the circuit in Fig. 1 can be used, both as a bias source for the memory cell as in Fig. 1 and also as an auxiliary memory cell for error compensation. Toumazou *et al.* describe in [13] an alternative compensation method which uses two auxiliary memory cells and a six-phase clocking scheme. This circuit achieves considerable CFT reduction in simulations; however,

Manuscript received October 13, 1993; revised May 27, 1994. This work was supported in part by the Kwf Jessi-Project, 2302.1 Eureka sc Eu 127.

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IEEE Log Number 9404028.

we have no information about an implementation in silicon. An interesting high-precision copier cell was proposed by Groeneveld *et al.* [8]. They achieve a relative precision of 16 b between two copied samples of a reference current and use this copier cell in a high-precision D/A converter.

Differential circuits are an alternative solution for the reduction of errors due to output conductance and CFT. Noise is doubled in these circuits, however. An example is reported in [9].

Reduction of copying errors in the basic memory cells caused by CFT and sampled noise still remains a fundamental problem in high-precision circuits. In spite of the proposals to keep the output voltage constant, in many applications such as those where dc offsets are not tolerable and voltage drops in switches appear in the output, low output-conductances of the current sources are still required. Some of the cancellation techniques depend on matching of transistor characteristics or on stages with only approximate balancing properties. Low output conductances may be of great importance in these cases. Starting with reduced individual errors in compensating schemes leads to improved results.

The present paper deals with high-precision current copiers based on cascode current sources, error-correction stages, and electronically multiplied gate-source capacitances for CFT and noise reduction. We present experimental results for circuits integrated in a 1-μm CMOS process and compare measured results with simulated and calculated figures.

II. Errors Caused by Finite Output Conductances of Transistors

The output conductances of the MOS transistors used in the circuit of Fig. 1(b), both those of the transistors in the bias source I_0 as well as those of the storage transistor S_1, deteriorate the precision of the memory cell, when the track mode and the hold mode (or the read-out) operate at different bus-voltages V_B. For example, consider the simple delay cell of Fig. 2. Here a current is stored into the master-cell S_1 during clock-phase ϕ_1 and later copied into the slave-cell S_2 during clock-phase ϕ_2. During the *track* phase ϕ_1 when S_1 reads the input current i_i, the stored current i_1 and the actual bus voltage $V_B = V_{BT}$ become

$$i_1 = i_i + I_{01} \tag{1}$$

and

$$V_{BT} = \sqrt{(i_i + I_{01})/k_1} + V_{T1}, \tag{2}$$

respectively. During the *hold* phase ϕ_2, the current i_i is copied into S_2, and the output voltage of S_1 changes to $V_B = V_{BH}$ with

$$V_{BH} = \sqrt{(-i_i + I_{02})/k_2} + V_{T2}. \tag{3}$$

(2) and (3) assume the simple quadratic gate-voltage to drain-current characteristics of the involved MOS transistors S_1 and S_2, respectively; correspondingly, k_1, k_2 and V_{T1}, V_{T2} designate the slope factors and the threshold voltages, respectively. The transistor output-conductances of the master cell introduce

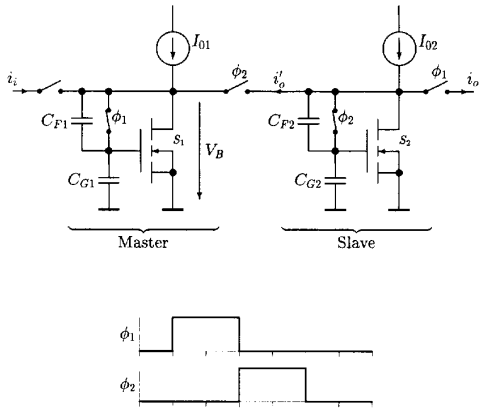

Fig. 2. Master–slave delay cell.

a total copying error-current, $\Delta i \triangleq i'_o - i_i$, between input i_i and output i'_o of the master cell given by:

$$\Delta i \approx g_{\text{eff}}(V_{BH} - V_{BT}),$$
$$g_{\text{eff}} \triangleq g_{0B} + g_{01} + g_{m1}\frac{C_{F1}}{C_{F1} + C_{G1}}, \tag{4}$$

where g_{0B} and g_{01} are the output conductances of the bias current source I_{01} and of the storage transistor S_1, respectively, g_{m1} is the transconductance of S_1 at current $i_1 = i_i + I_{01}$, C_{G1} is the gate capacitance of S_1, and C_{F1} is the coupling capacitance from the bus to the gate of S_1, cf. Fig. 2. The last term in the expression (4) for g_{eff} reflects the capacitive feedback from the master-cell output to the gate of S_1. This feedback induces a gate voltage $\Delta V_G = \Delta V_B C_{F1}/(C_{F1} + C_{G1})$ where $\Delta V_B \triangleq V_{BT} - V_{BH}$, which results in a drain error-current $g_{m1}\Delta V_G$ for S_1. The slave cell S_2 in Fig. 2 adds a supplementary error caused by its excursion from V_{BT} to V_{BH}.

We combat errors of the type just described by the addition of an auxiliary storage cell S'_1 as shown in Fig. 3. If such an auxiliary cell is coupled through a switch S' to the basic memory cell S_1 while S_1 is in hold phase and the signal source is still connected, then S'_1 reads the error current Δi of cell S_1. During the track phase of S'_1, the bus voltage V_B is[1]

$$V_{BR} = \sqrt{(\Delta i + I'_{01})/k'_1} + V'_{T1} \approx \sqrt{I'_{01}/k'_1} + V'_{T1}, \tag{5}$$

where k'_1 and V'_{T1} are the slope factor and the threshold voltage, respectively, of S'_1. Note that V_{BR} is nearly independent of the signal current i_i when the errors are small, i.e., when $\Delta i \ll I'_{01}$. After S'_1 has switched to hold, the current i_i is disconnected from the input and a current of magnitude i_i is mirrored to the output path. Because the current stored in S'_1 contains the error produced by S_1 and due to the voltage difference $V_{BT} - V_{BR}$, the sum of the currents in S_1 and S'_1 cancels Δi. Thus, *no* error appears in the output if both the input signal i_i and the output signal i_o are referenced to the

[1] We call the bus voltage realized in the described configuration the *reference* bus-voltage and measure errors with respect to that voltage. Although this reference voltage is not precisely defined because it varies from stage to stage, we use the approximation in (5) for the reference voltage.

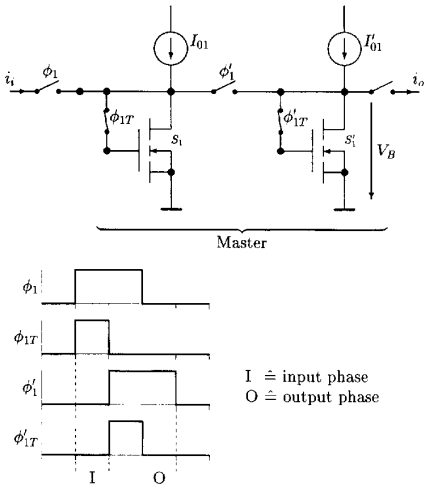

Fig. 3. Auxiliary storage cell to cancel errors caused by finite transistor output-conductances.

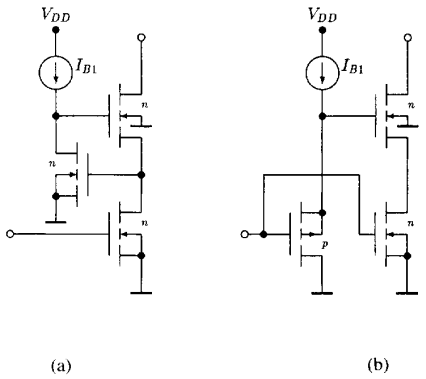

Fig. 4. Cascode circuits well-suited for the application in SI circuits. (a) Regulated cascode of Säckinger and Guggenbühl [14]. (b) Cascode of Guziński and Kulej [15].

voltage V_{BR}. Note that the auxiliary transistor can be operated with smaller transconductance and correspondingly smaller output conductance, which reduces the error according to (4).

The S^{2}I circuit proposed by Hughes *et al.* [12] follows a similar idea. Their method of compensating for V_B changes is as follows: In a first subcycle, the current source I_0 in Fig. 1(b) is a bias source; in a second subcycle, I_0 works as an auxiliary switched storage cell and compensates for the Δi error. The S^{2}I circuit involves fewer components than does our circuit of Fig. 3. However, our separation of biasing and compensation by the addition of a auxiliary cell leaves us more freedom for optimization with respect to CFT and noise.

The cancellation schemes described work well when the cell input and output currents are delivered and consumed at the reference voltage V_{BR}. This reference voltage is, according to (5), dependent on the characteristics of the auxiliary cell. Differences between the reference voltages of cascaded stages introduce residual copying errors. Such reference-voltage differences ΔV_{BR} arise from various sources such as

- differences between the individual reference bus-voltages V_{BR} specified by (5),
- voltage drops across internal resistances of *real* coupling switches between individual stages, and
- deviation of source and load voltages from the ideal reference bus-voltage V_{BR}.

Such ΔV_{BR} problems are important in high-precision circuits because they introduce errors analogous to the ΔV_B problem described by (4). With ΔV_{BR} denoting the difference between the effective reference voltages of the source cell and the load cell, the resulting equivalent copying current-error Δi_c is

$$\Delta i_c = g_{\text{eff}} \Delta V_{BR}, \tag{6}$$

i.e., it strongly depends on the effective conductance g_{eff} of the circuit feeding the load cell.

The signal-dependent portions of Δi_c in (6) are usually the most disturbing. One signal-dependent part of ΔV_{BR} and, in turn, of Δi_c arises from the residual ON-resistance R_i of the lateral switch connecting two cells. This resistance produces a voltage drop of $\Delta V_{BR} \approx R_i i_i$. Another signal-dependent contribution occurs when there are storage cells for which the condition $\Delta i \ll I_0$ is not fulfilled in (5).

Equation (4) and (6) show that we can reduce the described errors by keeping the conductance g_{eff} as small as possible. Using cascode circuits to replace simple transistors in the current-source circuits—in bias cells as well as in storage cells—is the solution to this problem because cascodes offer not only low ohmic output conductances but also low feedback capacitances from the output to the gate terminal. The classical cascode stage—a common-source stage followed by a constantly biased common-gate stage—suffers, however, from a low dynamic range since both stages have to operate in the saturation region. Because in an SI storage cell in track mode the gate is connected to the output terminal by a closed switch, the classical cascode is not suitable. The circuits proposed in [14], [15] solve the problem of dynamic range restriction. Proposal [14] is preferable since it obtains a $(g_0/g_m)^2$ reduction of its static output conduction; proposal [15] obtains only a $(g_0/g_m)^2$ reduction corresponding to a simple cascode. Toumazou *et al.* [16] also use cascode circuits of the type proposed in [14].

The following numerical examples illustrate the need of cascode circuits in high-precision SI applications. These examples apply to the 1-μm SACMOS process described in [17] that we used in our implementations. We consider an NMOS transistor with $W/L = 10$ μm/1 μm operated at a drain current of $I_0 = 70$ μA. The resulting transconductance g_m and output conductance g_0 are $g_m \approx 0.36$ mA/V and $g_0 \approx 10^{-5}$ A/V, respectively, whereas the gate capacitance C_G and the gate-drain capacitance C_F are $C_G \approx 16$ fF and $C_F \approx 4$ fF, respectively. The corresponding coefficient g_{eff} is $g_{\text{eff}} \approx 9.2 \cdot 10^{-5}$ AV. The voltage drop across a coupling switch with internal resistance $R_i = 1$ kΩ then gives, for $\Delta V_B \approx R_i i_i$, a relative current-error of $\Delta i_c / i_i \approx 9.2 \cdot 10^{-2}$ or $\Delta i_c / \Delta V_B \approx 92$ nA/mV for V_B changes.

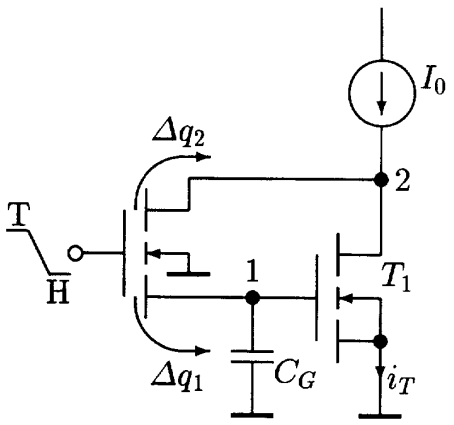

Fig. 5. Origins of clock-feedthrough. "T" indicates "Track"-mode," "H" indicates "Hold"-mode. Current source I_0 is realized according to the block *Bias Source* in Fig. 8. Transistor T_1 is realized as regulated cascode according to the block *Storage Transistor* in Fig. 8.

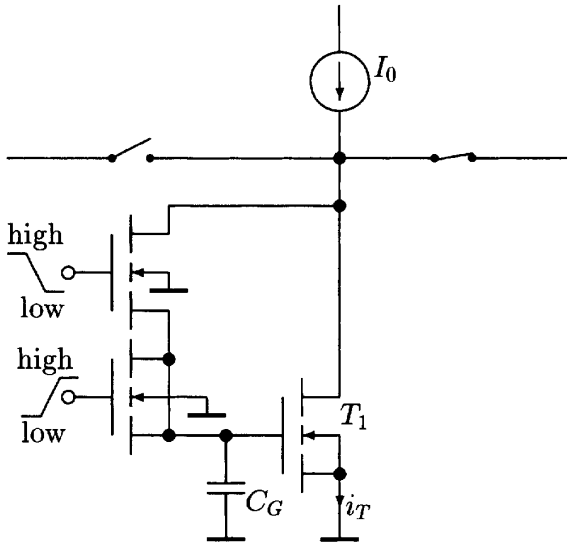

Fig. 6. Simple memory cell with dummy switch. Current source I_0 is realized according to the block *Bias Source* in Fig. 8. Transistor T_1 is realized as regulated cascode according to the block *Storage Transistor* in Fig. 8.

If we enhance the gate capacitance C_G with an external capacitor to 1 pF, we obtain $g_{\text{eff}} \approx 2.14 \cdot 10^{-5}$ A/V and a relative current-error of $\Delta i_c/i_i \approx 2.14 \cdot 10^{-2}$. With regulated-cascode circuits and with $C_F \approx 1$ fF and $C_G = 1$ pF, the coefficient g_{eff} reduces to $g_{\text{eff}} \approx 3.2 \cdot 10^{-7}$ A/V; the relative current-error becomes $\Delta i_c/i_i \approx 3.2 \cdot 10^{-4}$ or $\Delta i_c/\Delta V_B \approx 0.93$ nA/mV. These numbers illustrate the desirability of using cascode circuits—preferably regulated cascodes—to realize the various current sources in many applications.

III. Errors Caused by Clock-Feedthrough

Clock-feedthrough (CFT) is a major source of error in SI circuits. It originates from the charge injected from the channel and the overlap capacitances into the storage capacitor when the feedback switch-transistor in the basic memory cell opens to drive the cell from the track mode to the hold mode. As Fig. 5 illustrates, a portion Δq_1 of this charge is pushed into the gate capacitor C_G, and, in turn, changes the gate voltage by: $\Delta V_G = \Delta q_1/C_G$. This gate-voltage change results in a change of the drain current by:

$$\Delta i_{CF} \approx g_m \frac{\Delta q_1}{C_G}. \tag{7}$$

Several authors have investigated how the the total charge stored in the feedback switch is split into portions Δq_1 and Δq_2 that are injected to the adjacent circuit nodes during switching-off, [18], [19]. The charge Δq_1 injected into C_G depends on the switching speed, the source-to-substrate voltage, and the capacitance ratio between the node capacitances of the switching-transistor terminal nodes. Recommended remedies against CFT are

- a high value of C_G, which is achieved by an additional gate capacitor;
- a minimum-size feedback switch;
- compensation of Δq_1 by a dummy switch as illustrated in Fig. 6; and
- compensation schemes using auxiliary cells.

The first two remedies against CFT are obvious; the well-known [20] "dummy-switch compensation" has been treated in detail for voltage-mode sample-and-hold circuits [21]. As in the latter situation, we find here a complicated dependence on many circuit parameters including the time relation between the two gate-voltages driving the main switch and the dummy switch, respectively. Therefore, we do not attempt to determine the optimum size of the dummy transistors analytically for the considered SI cell, but instead, use on a sub-optimum size found by try-and-error simulations.[2] The result so obtained deviates from the "half-size rule" often found in the literature.

As mentioned in the introductory section, several CFT reduction schemes using auxiliary cells have been proposed. Our auxiliary cell S_1' shown in Fig. 3 also serves this purpose. The same mechanism that compensates for bus-voltage variations as shown in Section 2 can be used for CFT reduction. The cell S_1' stores the CFT error of cell S_1 and cancels it in the hold mode. If the current bias of S_1' is much larger than the CFT current of S_1, i.e., if $I_{01}' \gg i_{CF}$, then the remaining CFT error of the auxiliary cell is nearly independent of the signal current and is, therefore, tolerable in many applications. This property was also claimed by Hughes *et al.* [12] for their S^{2}I cell. If S_1' is designed with a lower transconductance than S_1, i.e. with $g_m' \ll g_m$—a solution which is not so easy to realize with the cell [12]—, the remaining CFT error of the auxiliary cell is considerably reduced according to (7). In some applications such as in master–slave delay cells, cf. Fig. 2, the remaining CFT error is further compensated in the following slave cell

[2] Although some SPICE models do not give reliable results for charge injection, we have found that the models used in ESPICE give good correspondences with experiments on integrated circuits. We used ESPICE, a version of SPICE developed by Philips Ag, because the chip was fabricated by Faselec Ag, a Philips company, in a 1-μm CMOS process for which ESPICE supplies adapted transistor models.

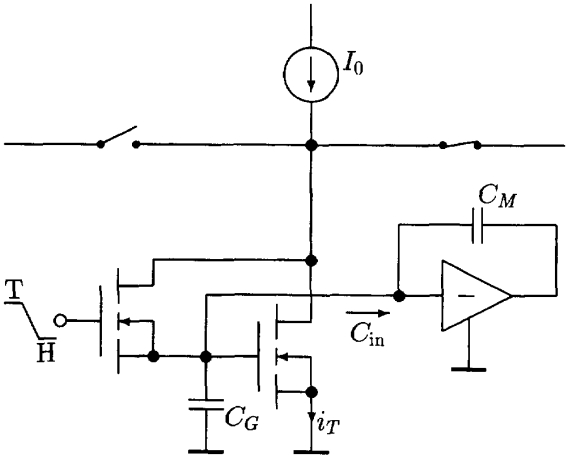

Fig. 7. Miller-enhanced memory cell. "T" indicates "Track"-mode, "H" indicates "Hold"-mode.

if both cells are equipped with auxiliary cells according to Fig. 3. Mismatch problems between master cell and slave cell have to be carefully considered and correspond to the voltage-difference problem mentioned in Section 2.

We present next a new method that allows us to greatly reduce CFT. In the present section we present the main idea of the technique, which we call "Miller enhancement method." In Section 5, we give experimental confirmation of the predicted improvements. To explain the method, we first observe that SI cells require gate capacitances that are neither precise nor linear and we note that *large* capacitances achieve low CFT. We can realize such a large capacitance by placing a (small) capacitor into the feedback loop of an amplifier and use the input port as the terminals for the resulting increased capacitance as illustrated schematically in Fig. 7. This effective capacitance C_{in} becomes

$$C_{\text{in}} \approx (A+1)C_M, \tag{8}$$

where A is the voltage gain of the amplifier and C_M is the capacitor in its feedback loop.

The simplest amplifier of this type is shown in Fig. 8. It consists of a single transistor stage T_3 with a feedback capacitor C_M between drain and gate. Connecting its input in parallel to the current memory cell adds a capacitance according to (8) to the gate of this cell. The bias current of this Miller amplifier tracks the current to be stored in the memory cell, since both gates are connected. A reasonably large range of stored currents combined with the fixed load resistance of the Miller amplifier would cause problems with the operating point. Therefore, we apply a dynamic load consisting of a p-type MOS transistor T_4 acting as a complementary dynamic memory cell. Transistor T_4 tracks the current forced into T_3 by the main memory cell as long as switch T_5 is closed. It switches to its high-impedance state when switch T_5 opens just before the track-to-hold transition of the main memory cell. It then presents a high-load resistance to T_3 as is required for a high gain A in (8) during the subsequent charge injection to the storage gate of T_1 of the main switch. Although this

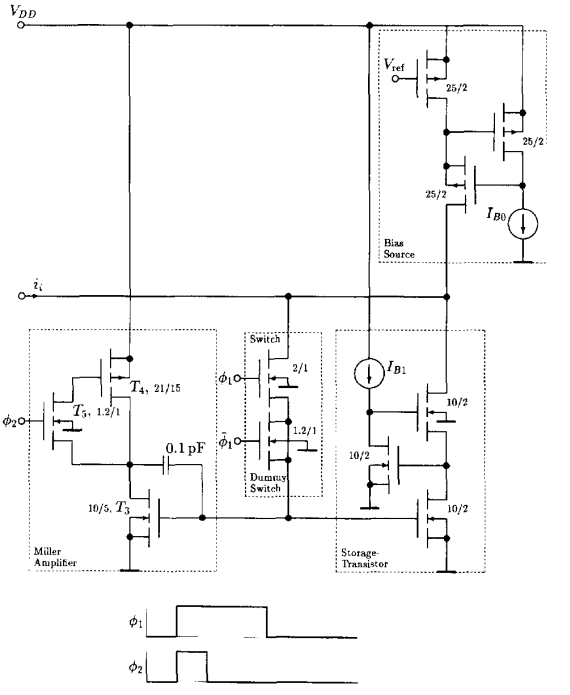

Fig. 8. Schematics of improved memory cell with dummy-switch compensation and Miller enhancement. The n- and p-channel current sources I_{B0} and I_{B1} are realized with classical one-to-one current mirrors using $10/2$ and $25/2$ transistors, respectively.

switching sequence introduces a speed penalty compared to the ordinary—the non-Miller—circuit, this speed degradation remains within reasonable limits.

As the experimental results presented in Section 5 confirm, we obtain the best results when we combine the *Miller-enhancement method* with *dummy-switch compensation.*

The reduction of CFT errors by combined dummy-switch/Miller enhancement appears to be very useful in many high-precision circuits for further reduction of compensated error, or for systems in which no cancellation exists.

IV. Noise in Switched–Current Memory Cells

Noise in SI memory cells can be analyzed by the methods of noise analysis for general sampled-data systems. Opening the feedback switch of the memory cell freezes the instantaneous noise voltage across the gate capacitor during the succeeding hold period. In addition to this sampled noise that is further processed as a sampled noise current, a continuous-time wideband noise current-signal appears in the output line of the cell. If the considered cell is coupled to a following SI cell, this continuous-time noise current is sampled in the next stage. Low-frequency noise such as flicker ($1/f$) noise usually accompanies the continuous-time wideband noise.

To describe the transformation of continuous-time noise into sampled-current noise, we calculate the noise-power spectral density of the voltage process across the gate capacitor for the track phase and determine the total noise power, which is

the variance of the frozen capacitor-voltage noise sample.[3] We base our computations on the noise-equivalent circuit shown in Fig. 9(b) and find the power-spectral density of the noise process across the gate capacitor C_G to be

$$S_{v_c}(\omega) \approx \frac{S_{n0}(\omega) + S_{ns}(\omega) + S_{ni}(\omega)}{g_{ms}^2 + \omega^2 C_G^2};$$

where $S_{n0}(\cdot)$, $S_{ns}(\cdot)$, and $S_{ni}(\cdot)$ are the noise power spectral densities of the bias source, the storage transistor, and the noise accompanying the input signal, respectively; g_{ms} and C_G denote the transconductance and the gate capacitance, respectively, of the storage transistor biased by $i_i + I_0$. The variance of the instantaneous noise voltage that is frozen on C_G when cell S goes from track to hold, $\sigma_{v_c}^2$, now becomes the integrated power spectral density. For wideband noise modeled as white noise with $S_{n0}(\omega) = S_{n0} = \text{const}$, $S_{ns}(\omega) = S_{ns} = \text{const}$, and $S_{ni}(\omega) = S_{ni} = \text{const}$, we obtain

$$\sigma_{v_c}^2 \approx \frac{1}{2\pi}\int_0^\infty S_{v_c}(\omega)d\omega \approx \frac{1}{4g_{ms}C_G}(S_{n0} + S_{ns} + S_{ni}).$$

The resulting variance $\sigma_{i_o}^2$ of the stored noise current is then

$$\sigma_{i_o}^2 \approx \frac{g_{ms}}{4C_G}(S_{n0} + S_{ns} + S_{ni}). \tag{9}$$

If we further assume a classical white noise power-spectral density for the MOS transistors, $S_{n0} = 8/3 \cdot kTg_{m0}$ and $S_{ns} = 8/3 \cdot kTg_{ms}$, we find

$$\sigma_{i_o}^2 \approx \frac{2}{3}\frac{kTg_{ms}^2}{C_G}\left(1 + \frac{g_{m0}}{g_{ms}}\right) + \frac{g_{ms}}{4C_G}S_{ni}. \tag{10}$$

For the first term of the sum in (10) and for the typical values of $C_G = 1\,\text{pF}$, $g_{ms} = 3 \cdot 10^{-4}\,\text{A/V}$, and $g_{m0} = g_{ms}$, we obtain for the standard deviation of the stored noise current

$$\sigma_{i_o} \approx 2.9 \cdot 10^{-8}\ \text{A} + \text{input-noise contribution}.$$

We have found that the Miller enhanced circuits perform even better than would be expected when C_G in (10) is enlarged by the Miller capacitance (8). The additional noise contribution of the Miller stage itself remains small. Omitting detailed explanations, we state that the variance of sampled output current-noise in a Miller-enhanced storage cell is smaller than

$$\sigma_{i_o}^2 < \frac{g_{ms}}{4C_{G\text{eff}}}\left(S_{n0} + S_{ns} + S_{ni} + \frac{S_{n3} + S_{n4}}{1 + g_{ms}/g_{m3}}\right), \tag{11}$$

where $C_{G\text{eff}} \approx C_G + (A+1)\,C_M$ and S_{n3} and S_{n4} denote the white-noise power spectral densities of the transistors T_3 and T_4, respectively, in the Miller amplifier in Fig. 8 and where g_{m3} is the transconductance of T_3. These findings have been confirmed by measurements.

To analyze the total noise of a cascaded system according to the circuit in Fig. 3, we note that the auxiliary cell not only compensates for the sampled noise of the main storage cell but also contributes itself to the total noise. Low transconductance auxiliary cells, as we proposed above to combat errors caused by finite output conductances and CFT errors, are preferable for good noise performance. We will treat this noise compensation problem and will give a detailed analysis of the noise performance of the Miller-enhanced circuit in a separate paper.

[3] We here assume that the continuous-time noise process has practically reached stationarity towards the end of the track period.

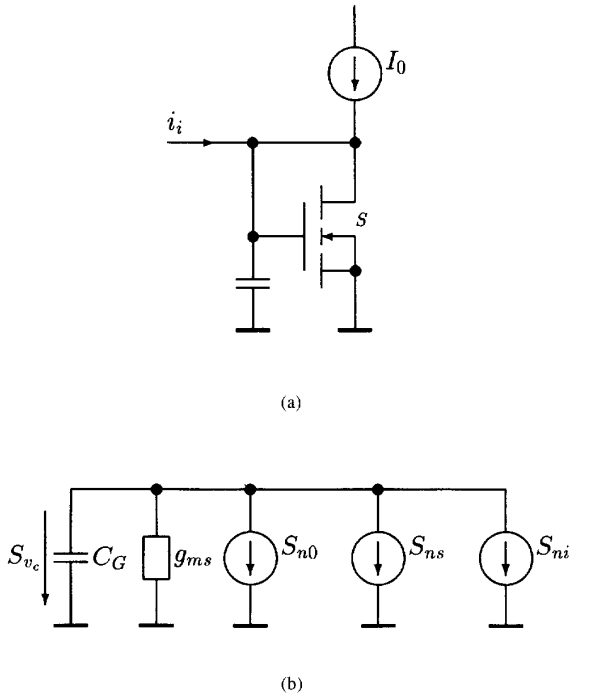

Fig. 9. Basic memory cell in track mode (a) and noise-equivalent circuit (b). The symbols S_{n0}, S_{ns} and S_{ni} denote the current-noise power spectral densities of the bias source, of the storage transistor and of the noise accompanying the input signal and S_{v_c} is the power spectral density of the voltage across the gate capacitance; all of these power spectral densities are, in general, frequency-dependent.

V. Experimental Results

We have designed, simulated, and integrated various configurations of dynamic current-memory cells. As mentioned, our implementations use the 1-μm SACMOS process described in [17]. Because our present interest is focused on CFT reduction techniques—especially on the Miller-enhancement method—we concentrate here on simple cells based on the generic structure shown in Fig. 1(a) and use these cells as test vehicles. All current sources have been realized with regulated-cascode structures according to Fig. 4(a), [22], to achieve the low output-voltage dependence of the current-copying factor that is necessary in many high-precision applications. The following circuit versions have been designed, simulated, integrated, and tested:

(i) A double cascode structure with (physical) capacitor $C_G = 1\,\text{pF}$ and a simple feedback-switch transistor with dimensions $W/L = 1.9\,\mu\text{m}/1\,\mu\text{m}$. We use this structure as a reference for comparison to better designs.

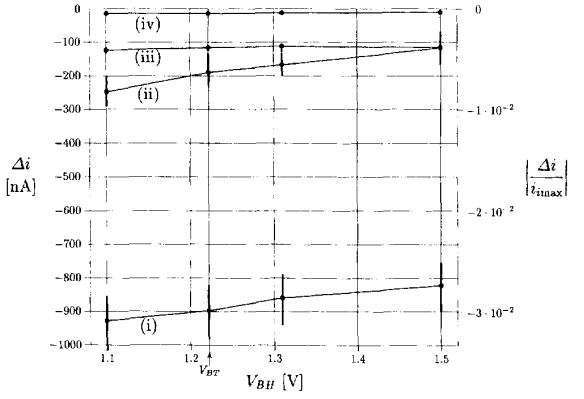

Fig. 10. Measured dependence of copying error on output voltage V_{BH} of the output circuit (bias current $I_0 = 70\ \mu$A, signal current $i_i = 30\ \mu$A, clock rate 100 kHz). The dots indicate the measured mean values and the rules show the differences between the measured minimum and maximum values in a sample of 19 chips. The curves are for (i) basic cell, (ii) basic cell with optimized dummy switch, (iii) Miller-enhanced cell and (iv) Miller-enhanced cell combined with optimized dummy switch.

(ii) As in (i) but with an experimentally optimized dummy transistor in series with the feedback-switch transistor.

(iii) As in (i) but with a gate capacitance that is realized by our novel Miller enhancement method.

(iv) As in (iii) but with an experimentally optimized dummy transistor in series with the feedback-switch transistor.

Our test results are summarized in Fig. 10 and show the dependence of the copying error $\Delta i \widehat{=} i_o - i_i$ on the voltage V_{BH} of the output circuit. This error can be split into an offset part, which is measured at the output- (hold-) voltage equal to the track voltage V_{BT} at which i_i was stored into the cell, and into a part that reflects the varying output- (hold-) voltage according to (4). The high offsets of the curves (i), (ii), and (iii) are caused by CFT, which is only optimally reduced in the combined dummy-switch/Miller-enhanced circuit, cf. curve (iv). The effective output conductance of the current sources—reflected in the voltage dependence of the Δi curves—is considerably improved in both Miller-enhanced circuits, cf. curves (iii) and (iv). Because the effective gate capacitance realized by the Miller-enhancement method is about an order of magnitude larger than the physical capacitor used in the circuits (i) and (ii), these observations confirm that capacitance feedback dominates the output conductance of the regulated cascodes according to (4). The curves in Fig. 10 were measured at maximum signal current $i_i = i_{i\max} = 30\ \mu$A. We have observed similar copying-error characteristics for the whole range of signal currents $[i_{i\min} = -30\ \mu$A, $i_{i\max} = 30\ \mu$A].

Fig. 11 shows the dependence of the copying error Δi on the signal current for the same circuit configuration on which Fig. 10 is based.[4] Again the dummy-switch/Miller-enhanced circuit is the best solution. In Fig. 12 we show the results for the two Miller versions (iii) and (iv) in an enlarged scale. We also show the minimum values and maximum values measured for a sample of 19 chips that confirm that our method is robust with respect to parameter variations for the individual transistors.

Summarizing the results for our dummy-switch/Miller-enhanced circuit, we achieve a maximum copying error of about 0.1% with respect to a maximum one-sided signal current $|i_{i\max} = 30\ \mu$A|. This corresponds to a dynamic

[4]The discontinuity in Fig. 11 for zero signal current is due to our measurement equipment, which used distinct current source and current sink circuits for positive and negative signals.

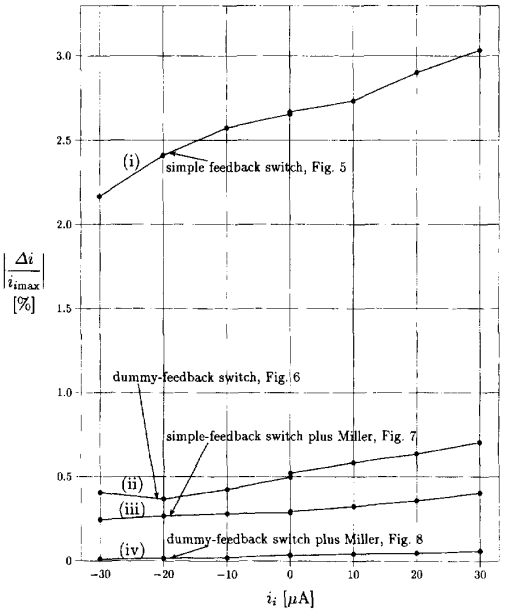

Fig. 11. Measured dependence of copying error on signal current i_i (bias current $I_0 = 70\ \mu$A, load voltage 1.24 V corresponding approximately to the reference voltage, clock rate 100 kHz). The dots indicate the measured mean values in a sample of 19 chips. The curves are for (i) basic cell, (ii) basic cell with optimized dummy switch, (iii) Miller-enhanced cell and (iv) Miller-enhanced cell combined with optimized dummy switch.

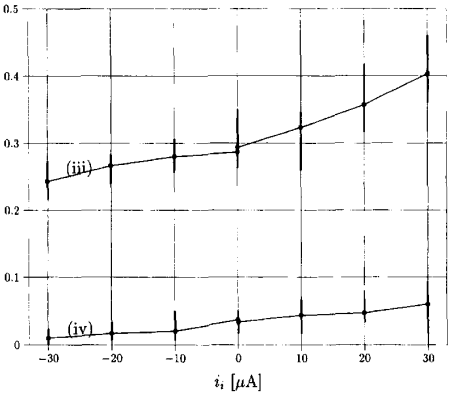

Fig. 12. Measured dependence of copying error on signal current i_i for the two Miller-enhanced versions (bias current $I_0 = 70\ \mu$A, load voltage 1.24 V corresponding approximately to the reference voltage, clock rate 100 kHz). The dots indicate the measured mean values and the rules show the differences between the measured minimum and maximum values in a sample of 19 chips. The curves are for (iii) Miller-enhanced cell and (iv) Miller-enhanced cell combined with optimized dummy switch.

range of 11 b for the bipolar signal range [$i_{\text{imin}} = -30$ μA, $i_{\text{imax}} = 30$ μA] in our circuits.[5] The experimental results achieved with the integrated circuits agree well with the theoretical predictions of Section 2 and Section 3 as well as with the results of simulations performed prior to the layout of the circuits.

Fig. 13 shows those parts of the microphotograph of the prototype chip containing the solutions (i)—the reference structure with a physical gate capacitor $C_G = 1$ pF—and the best solution (iv)—the combined dummy-switch/Miller-enhanced circuit. We see that the considerable improvements obtained with the Miller-enhancement method uses approximately the same silicon area as the more classical solution (i). If CFT-error currents equivalent to those in our combined dummy-switch/Miller-enhanced circuit have to be achieved with a physically large capacitor at the gate terminal, then a chip area four to five times larger would be needed.

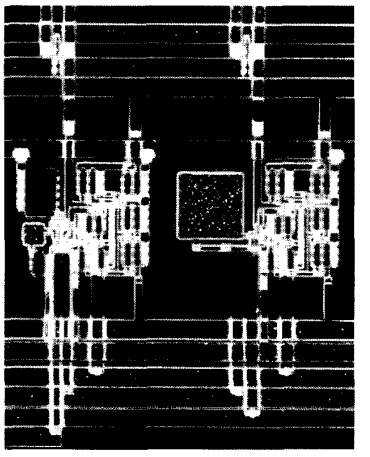

Fig. 13. Microphotograph of part of the prototype chip; on the left-hand side the combined dummy-switch/Miller-enhanced circuit (iv), on the right-hand side structure (i) with a physical gate capacitor $C_G = 1$ pF.

VI. Summary and Conclusion

We have investigated the limitations of high-precision dynamic current-memory cells and related these limitations to circuit-design parameters. One source of current copying-errors that often limits the use of the considered basic SI circuit blocks is the finite output conductance of the current sources imbedded as bias sources and as storage cells. These nonideal current sources produce errors proportional to the output-voltage steps when the transition from the track mode to the hold mode of the storage cell occurs. Additional auxiliary error-storage cells, which operate at a fixed reference or signal-return voltage, cancel these errors to the first order. For many applications, our quantitative estimates indicate that circuits with special cascode techniques will be needed to reduce the remaining copying errors.

Clock-feedthrough (CFT) is the most significant error source in SI circuits. The auxiliary cells introduced in the present paper can be designed to reduce CFT errors. Furthermore, a new way to reduce CFT error-currents has been proposed. It is based on an electronically enlarged gate capacitance and is realized by a switched-load Miller amplifier; the result is an area-efficient CFT reduction circuit. Although this CFT improvement degrades speed performance as do all circuits based on enlarged gate capacitances, we have built—with a combined dummy-switch/Miller enhancement CFT reduction—current copier circuits that achieve a dynamic range of about 11 b at a clock rate of more than 100 kHz.[6] The power dissipation of these circuits is 300 μW per cell.

Noise is another performance-limiting factor in SI circuits. Our analysis of the process for converting continuous-time wideband noise to sampled-data noise indicates a dynamic range limit similar to the limit set by CFT. Ideas for CFT reduction apply also to sampled-noise reduction.

We have integrated several memory-cell structures in a 1-μm CMOS process. Experimental results gained from these test structures confirm our theoretical predictions. Experiments with integrated A/D converter circuits are in preparation; their results will be described in a future paper.

[5] In the meantime, we have achieved with a new design similar results for clock frequencies up to 1 MHz.

[6] In the meantime we have achieved with a new design similar precisions for clock frequencies up to 1 MHz.

Acknowledgment

The authors would like to thank Jerzy B. Lont for valuable discussions and Prof. James L. Massey for a linguistic review of the manuscript. They also wish to thank the anonymous referees for their useful comments and suggestions.

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