A High-Slew Integrator for Switched-Capacitor Circuits

Andrew E. Stevens, *Student Member, IEEE*, and Gerald A. Miller, *Member, IEEE*

***Abstract*— A new method for improving the slew rate of a switched-capacitor integrator is introduced. A booster circuit is used to measure the integrator input voltage and then inject a proportionate amount of charge at the integrator output. The boosted integrator significantly reduces the settling time due to amplifier slewing. In addition, the booster has no adverse effect on the noise and stability performance of the integrator. The booster stage increases the total static integrator power by 36% and the total die area by 22%.**

I. Introduction

A COMMON requirement in switched-capacitor circuits is a fast settling time on the amplifiers. In addition, the amplifier in such a circuit may need to drive a large capacitive load in order to reduce the effects of thermal (kT/C) noise. A direct result of these requirements is that a large output drive current is necessary on the amplifier in order to quickly change the voltage on the large capacitive loads and subsequently settle to the final value. Often, the amplifier slew rate will severely limit the settling time of the circuit. Fig. 1(a) shows a typical noninverting switched-capacitor integrator with nonoverlapping clocks ϕ_1 and ϕ_2. The worst-case capacitive load on the amplifier occurs during ϕ_2 and depends predominantly on the input capacitor C_1, plus parasitics and loading effects of the next stage (collectively represented by C_L). The effect of the slewing is shown in Fig. 1(b), where the limited slew rate of the amplifier prevents the output voltage V_{OUT} from settling before the end of the ϕ_2 clock cycle.

Unfortunately, increasing the amplifier slew rate is often at odds with requirements for low power dissipation. The simplest method for increasing an amplifier slew rate is to increase the quiescent current in the input stage, thereby directly increasing the standby current in the entire amplifier. Other methods of enhancing the slew rate have involved dynamically boosting the input stage current [1], [2] or using a class AB input stage [3], though both methods can cause voltage swing problems inside the amplifier due to the large peak currents. Another method boosts the output stage current by monitoring the amplifier differential input voltage [4], but is limited by the frequency response of the booster circuit.

In this paper, a new method is introduced which boosts the slew rate of a noninverting switched-capacitor integrator. Since the integrator is an important building block in most switched-capacitor circuits, a complete high-slew integrator may be used to provide fast settling in lieu of using a high-slew amplifier. The new method boosts the current only at the output of the amplifier, and the extra current is only provided on an as-needed basis, thereby adding only a small amount to the total standby current of the circuit.

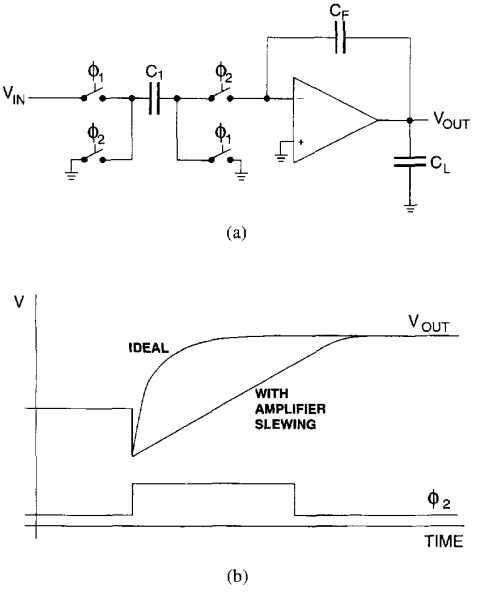

Fig. 1. (a) Switched-capacitor integrator and (b) the effect of slew rate on integrator transient response. If the slew rate is too low, the integrator will not settle before the end of the clock cycle.

II. Description of Boosted Integrator

A block diagram of the boosted integrator is shown in Fig. 2(a). This diagram shows a switched-capacitor integrator with an added external boost circuit which provides a dynamic current boost at the output of the amplifier. This is accomplished by measuring the input voltage and then injecting a proportionate amount of charge at the output of the integrator. The booster operates completely open loop with respect to the amplifier and reduces the amplifier to an error correction role. Thus, the requirements on the amplifier are relaxed because the boost stage does the bulk of the work. For example, if the booster circuit is 90% accurate, then the amplifier has only to settle the final 10% of the final value.

The booster circuit (Fig. 2(b)) contains four parts: a sampling capacitor C_2, a charge amplifier ($M1$–$M4$), a pair of current mirrors, and a shut-off switch. This sampling capacitor

Manuscript received November 19, 1993; revised June 1, 1994. This work was supported by the OYO Geospace Corp.

A. E. Stevens is with the Department of Electrical Engineering, Columbia University, New York, NY 10027 USA.

G. A. Miller is with Analog Devices, Inc., Wilmington, MA 01887 USA.

IEEE Log Number 9404026.

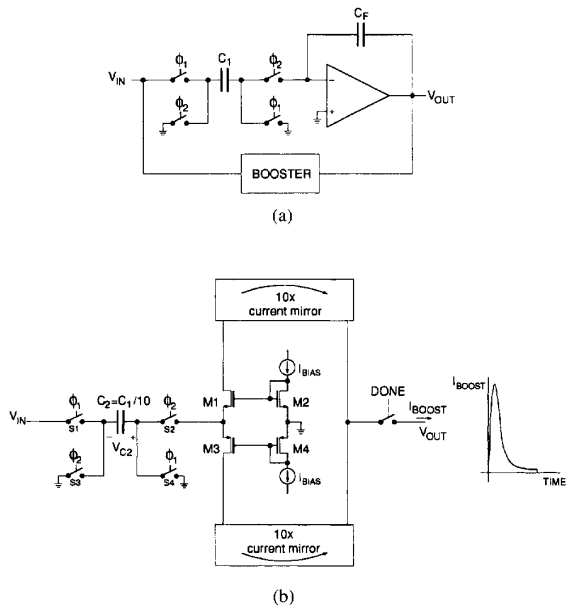

Fig. 2. (a) Slew booster is located external to integrator. (b) Schematic diagram of booster.

is ten times smaller than the sampling capacitor C_1 at the integrator amplifier input, which reduces the added input capacitance presented by the booster. The sampling capacitor is connected to the input devices $M1$ and $M3$ of the charge amplifier, whose input is at a virtual ground due to the biasing scheme (the sources of biasing transistors $M2$ and $M4$ are grounded). The current mirrors copy the charge amplifier output current to the booster output and also provide a gain of ten. The "DONE" switch is open during the quiescent state and prevents any undesirable loading effects on the integrator amplifier. The actual implementation of the "DONE" switch will be explained later.

A brief summary of the operation of the circuit is as follows: During the ϕ_1 clock phase, the input voltage $V_{\rm IN}$ is sampled onto capacitor C_2. At the beginning of ϕ_2, the "DONE" switch is closed. Assuming a positive input voltage, the voltage presented to the charge amplifier during ϕ_2 will be negative (because the input voltage is inverted by the switching of C_2). Thus, the source of $M1$ will be pulled down, $M3$ will turn off, and a large current will flow through $M1$. This current is mirrored and amplified by the top current mirror and then is dumped directly on the output of the integrator. This current will have some initial peak value, and will then continually decrease as C_2 is discharged and $V_{\rm GS1}$ drops. When the discharge of C_2 is complete, the circuit disconnects itself from the amplifier by opening the "DONE" switch. Note that depending on the polarity of $V_{\rm IN}$, only half of the circuit (top or bottom) will operate during boosting.

A time-domain solution for the current through $M1$ may be found assuming a positive input voltage $V_{\rm IN}$ so that only the top half of the circuit operates (a corresponding solution for the current through $M3$ may be found for negative $V_{\rm IN}$). Thus, a negative voltage is presented at the source of $M1$ during ϕ_2 via the negatively-charged C_2. Since the source of $M1$ is fed directly to C_2, the capacitor current may be equated to the drain current

$$I_{D1} = C_2 \frac{dV_{C2}}{dt} = \frac{\beta_1}{2}(V_{\rm GS2} - V_{C2} - V_{\rm Tn})^2 \qquad (1)$$

where I_{D1} is the drain current of $M1$, V_{C2} is the voltage across C_2, $\beta_1 = (\mu C_{\rm ox})(W/L)$ is the geometry factor of $M1$, $V_{\rm GS2}$ is the quiescent gate-source voltage of $M2$, and $V_{\rm Tn}$ is the threshold voltage of the n-channel device. Separating the variables and integrating yields

$$I_{D1}(t) = \frac{I_{D1,\rm peak}}{\left(1 + \frac{g_{m1,\rm peak}}{2C_2}t\right)^2} \qquad (2)$$

where $I_{D1,\rm peak} = (\beta_1/2)(V_{\rm GS2} + V_{\rm IN} - V_{\rm Tn})^2$ and $g_{m1,\rm peak} = \beta_1(V_{\rm GS2} + V_{\rm IN} - V_{\rm Tn})$ are the peak values for the drain current and the transconductance of $M1$ (at the beginning of the ϕ_2 clock phase). (2) is an exact solution for the drain current of $M1$, neglecting drain-source resistances and assuming that only the top half of the total circuit is working. As C_2 reaches the very end of its discharge, the charge amplifier will return to its symmetrical quiescent state as $M3$ turns back on and the remaining charge on C_2 is bled off. The boost current $I_{\rm BOOST}$ will approximate (2), limited by the finite frequency response of the current mirror and amplified by the current mirror gain.

For design purposes, it is useful to approximate the transient performance of the booster circuit with a single RC time constant $\tau_{\rm BOOST}$ determined by the resistance seen by C_2. By inspection, this resistance consists of the resistances of switches $S2$ and $S3$ (r_{s2} and r_{s3}, respectively), plus the resistance looking into the charge amplifier ($1/g_{m1}$ or $1/g_{m3}$, depending on which half of the circuit is working). Thus, a useful limit on the booster time constant $\tau_{\rm BOOST}$ can be represented by:

$$\tau_{\rm BOOST} < C_2(r_{s2} + r_{s3} + 1/g_{m,\rm worst\ case}) \qquad (3)$$

where $1/g_{m,\rm worst\ case}$ is the worst-case resistance looking into the input transistors $M1$ and $M3$ of the charge amplifier. The worst-case (largest) value for $1/g_{m1}$ will occur at minimum I_{D1} or I_{D3}, which, by inspection of (2), occurs at the end of the boost cycle (maximum t). Thus, $1/g_{m,\rm worst\ case} = \max(1/g_{m1,\rm quiescent}, 1/g_{m3,\rm quiescent})$.

The control for the "DONE" switch is generated by sensing an "off" condition at either current mirror. Thus, if either current mirror is conducting zero current (indicating a half circuit shutdown during a boost), the DONE switch is closed and the boost current is conducted to the output of the integrator. When the boost is complete, both mirrors conduct a small standby current, and the DONE is switch opened, thereby disconnecting the booster from the integrator. The integrator amplifier then completes the charge transfer to high accuracy. In addition, since the booster is separated

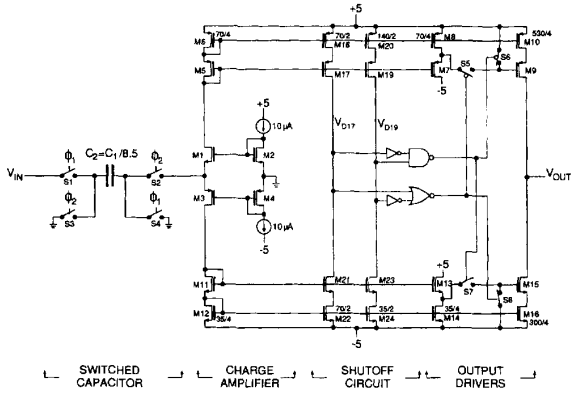

Fig. 3. Circuit diagram of booster circuit.

from the integrator by open switches, it does not affect the noise performance and stability of the complete integrator.

III. Circuit Design

A complete design for the booster circuit is shown in Fig. 3. The charge amplifier is formed by $M1$–$M4$. The two current mirrors are formed by $M5$–$M10$ and $M11$–$M16$. These cascode current mirrors contain a source follower between the input and output in order to extend the output swing [5]. The ratio between sampling capacitors C_1/C_2 is 8.5 (instead of ten) in order to ease the layout.

Transistors $M17$–$M24$, switches $S5$–$S8$, and the four logic gates form a shutoff circuit in order to perform the "DONE" function. Although conceptually modeled by a single switch in Fig. 2(b), this circuit actually works by operating four switches inside the current mirrors, thus avoiding any IR drop in the "DONE" switch. The quiescent power is also reduced because the output transistors $M9$–$M10$ and $M15$–$M16$ are off during the quiescent state. The circuit works as follows: both legs of the shutoff circuit (transistors $M17$–$M20$ and $M21$–$M24$) nominally carry a current of 20 μA. However, transistors $M19$–$M20$ and $M21$–$M22$ are sized to carry twice as much current as their counterparts on the opposite rail. Thus, in the quiescent state, $V_{D17} = -5$ and $V_{D19} = +5$. The outputs of the logic gates then drive switches $S5$–$S8$ in order to enable/disable the booster output transistors. In Fig. 3, the switches are shown in their quiescent position, thereby turning off transistors $M9$ and $M15$ and effectively disconnecting the booster from the integrator. During booster operation, half of the circuit (top or bottom) will turn off, and the remaining 20 μA current source will charge its output node to its own rail. This change in the logic level (either V_{D17} or V_{D19} will change levels, depending on whether the top or bottom half shuts off) will subsequently close $S5$ and $S7$ and open $S6$ and $S8$, which will turn on mirror outputs $M9$–$M10$ and $M15$–$M16$ and thus connect the booster to the integrator. When boosting is complete, both halves of the circuit will be on, and the switches will return to their quiescent state.

TABLE I
Circuit Characteristics

Power supplies	±5 V
Amplifier 3 dB bandwidth	3.6 MHz
Amplifier phase margin	72°
Amplifier slew rate	1.8 V/μs
Booster slew rate	14 V/μs
Value of C_1	85 pF
Value of C_F	155 pF
Value of C_2	10 pF
Die area	2200 μm × 2250 μm
Technology	2 μm CMOS double-poly

The implementation of Fig. 3 has several limitations due to the speed of the shutoff circuit and the finite bandwidth of the current mirrors. In particular, if the shutoff circuit is late turning on the output devices at the beginning of the clock cycle, a significant amount of charge may be lost at the output of the booster. The booster is particularly sensitive to this effect because the peak boost current occurs at the beginning of the cycle. Similarly, bandwidth limitations in the current mirror may cause the shutoff circuit to activate before the charge at the output is completely transferred. These effects were accounted for by adjusting the sizes of the output devices of the current mirrors in an attempt to optimize the overall performance. This was done at the simulation level. In addition, performance differences between the n-channel and p-channel transistors led to different gains in the two current mirrors (7.6× and 8.6×).

For small input voltages, the offset mismatch between the integrator amplifier and the booster may cause the booster to overcompensate and subsequently provide too much boost current. However, any added settling time due to overcompensation has no appreciable effect when compared to the longer settling time for larger input voltages (i.e., at input voltage magnitudes much larger than the offset voltage).

IV. Test Results

Characteristics of the test chip are shown in Table I. The integrator amplifier is a single-stage folded-cascode design. For comparison purposes, the test chip contains an identical integrator without the boost circuit. As seen in Fig. 4, the booster adds about 22% more area to the total integrator as compared to the unboosted integrator.

Fig. 5 shows the performance of the unboosted and boosted integrators. In the unboosted case, amplifier slewing at 1.8 V/μs dominates the settling time. In the boosted case, the slew rate is increased to 14 V/μs during the boost (7.8× improvement), but the booster only provides about 70% of the total necessary charge. Thus, the amplifier must settle the final 30%, which includes a short period of slewing at 1.8 V/μs. We believe that this performance could be improved by a better design of the "DONE" shutoff circuit in the booster. Table II shows the settling times to 1% accuracy.

By comparison, if the 200 μA idle current in the booster was instead applied directly to the amplifier, then the amplifier tail current would be increased by roughly 100 μA (for a folded-

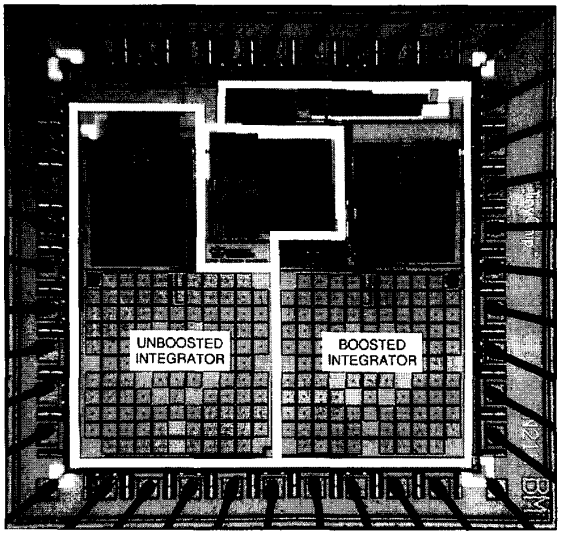

Fig. 4. Die photograph. The chip contains both boosted and unboosted integrators for comparison purposes.

TABLE II
SUMMARY OF RESULTS

	unboosted	boosted
Settling time of integrator (1% accuracy, $V_{IN}=-3.5$V)	2100 ns	600 ns
Settling time of integrator (1% accuracy, $V_{IN}=+3.5$V)	2000 ns	750 ns
Die area of integrator	1.35 mm^2	1.65 mm^2
Static power of integrator	5.5 mW	7.5 mW

cascode amplifier). This would only increase the amplifier slew rate by approximately 50% in an unboosted integrator configuration.

V. CONCLUSION

A new method has been introduced for boosting the slew rate of a switched-capacitor integrator by boosting the integrator as a whole, thereby avoiding any redesign of the amplifier. In addition, since the booster circuit is disconnected from the integrator after boosting, there are no added noise or loading effects. The circuit is particularly useful in low-power and low-noise applications such as Σ-Δ modulators, data converters, and switched-capacitor filters.

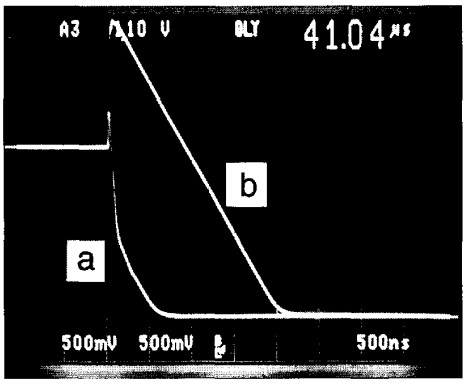

Fig. 5. Oscilloscope photograph showing the settling time of the boosted integratord (*trace a*). An unboosted integrator is shown for comparison (d*trace b*). Horizontal scale: 500 ns/div. Vertical scale: 0.5 V/div.

ACKNOWLEDGMENT

The authors gratefully thank P. Ju, D. Vallancourt, W. Lee and P. Ferguson.

REFERENCES

[1] M. G. Degrauwe, J. Rijmenants, E. A. Vittoz, and H. J. De Man, "Adaptive biasing CMOS amplifiers," *IEEE J. Solid-State Circuits*, vol. 17, no. 3, pp. 522–528, June 1982.
[2] J. Hosticka, "Dynamic CMOS amplifiers," *IEEE J. Solid-State Circuits*, vol. 15, no. 5, pp. 887–894, Oct. 1980.
[3] R. Castello and P. R. Gray, "A high-performance micropower switched-capacitor filter," *IEEE J. Solid-State Circuits*, vol. 20, no. 6, pp. 1122–1132, Dec. 1985.
[4] K. Nagaraj, "CMOS amplifiers incorporating a novel slew rate enhancement technique," in *Proc. IEEE 1990 Custom Integrated Circuits Conf.*, May 1990, pp. 11.6.1–11.6.5.
[5] P. R. Gray and R. G. Meyer, *Analysis and Design of Analog Integrated Circuits*, 2nd Ed. New York: Wiley, 1984.