A Voltage Compensated Series-Gate Bipolar Circuit Operating at Sub-2 V

Hisayasu Sato, Kimio Ueda, Nagisa Sasaki, Tatsuhiko Ikeda, and Koichiro Mashiko, *Member, IEEE*

***Abstract*— A low-voltage series-gate (LSG) bipolar circuit is proposed. A lower-input transistor of the series-gate circuit acts as a current source transistor. The lower-input is driven by VEE-Traced buffer (VTB). The dc characteristics of the VTB output trace the change in a power supply voltage VEE. The switching current of the series-gate circuit is stable while VEE changes. The design of VTB also takes the temperature variation into consideration. A 4-b counter using this circuit technology is fabricated with 0.8-μm double polysilicon self-align process. The maximum operating frequency of 640 MHz is obtained at -2.0 V and 25°C. The power dissipation of the 4-b counter is 3.3 mW. The circuit operates at over 500 MHz with the supply voltage of -1.6 V. The variation of VEE or temperature has a small effect on the circuit operation.**

I. Introduction

THE improvement of silicon bipolar technology has extended its application to GHz level data communication systems in which GaAs devices had dominated in the past. In these applications, especially in handheld wireless communication equipments and fiberoptic transceivers connecting EWS's, low-power operation is one of the most important issues. Also, as the operating voltage of CMOS circuits continues to decrease from 3.3 V to 2.5 V or even lower, while the operating frequency of microprocessors continues to increase from 100 MHz to 200 MHz or even higher, the I/O interfaces among microprocessor and memories and peripheral controllers become a critical path for the signal propagation. Silicon bipolar technology is a promising candidate for this area because of its high-speed operation and large driving capability.

Bipolar circuits can be integrated into these paths by applying MCM (multichip module) or BiCMOS technologies. Therefore, bipolar circuits should have low supply voltage to coexist with CMOS circuits on the same chip or the same board. However, reduction of the supply voltage has been difficult because of the saturation of bipolar transistors.

To meet this requirement, some low voltage techniques, which operate at 2.2 V, 2.5 V, and 1.5 V have been presented [1]–[3]. However, these circuits do not improve the speed performance and/or power dissipation because they cannot implement a series-gate circuit. Also these circuits are not sufficiently insensitive to power supply variations, so the amount of switching current varies as VEE fluctuates. This leads to deep saturation or degradation of noise margin. This becomes serious especially when a power supply voltage gets lower.

This paper describes series-gate bipolar circuits operating at a supply voltage of sub-2 V. In the following sections, we show the concept of the low-voltage series-gate (LSG) circuit and the VEE-Traced Buffer (VTB), some examples of the circuits, and their application to a 4-b counter. Finally its experimental results are given.

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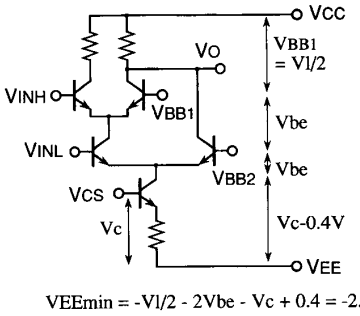


Fig. 1. LCML gate.

II. Circuit Design

A. Low-Voltage Series-Gate Circuit (LSG)

Fig. 1 shows an example of conventional Low-Level Current Mode Logic (LCML). The circuit diagram shows a 2-level series-gate circuit. In bipolar circuits, the range of the supply voltage is restricted by base-collector saturation. In Fig. 1, $VBB1$ is a threshold voltage for upper inputs. It is equal to half of voltage swing $V1$. Threshold voltage for lower inputs $VBB2$ is set to 1 Vbe below $VBB1$. We designed the circuit to operate in the light saturation mode with the base-collector forward bias of up to 0.4 V. The voltage between a collector node of a current source transistor and VEE becomes $(Vc - 0.4)$ V. Here, Vc is 1.1 V, which is equal to the output of a bandgap reference circuit. Therefore, the minimum power supply voltage, VEE min, is a sum of these values. It is represented as:

$$VEE\,\min = -V1/2 - Vbe - Vbe - Vc + 0.4V. \quad (1)$$

When $V1 = 0.4$ V, $Vbe = 0.8$ V, and Vc is 1.1 V, VEE min becomes -2.5 V in this circuit. Considering the operating margin of the circuit, the practical power supply

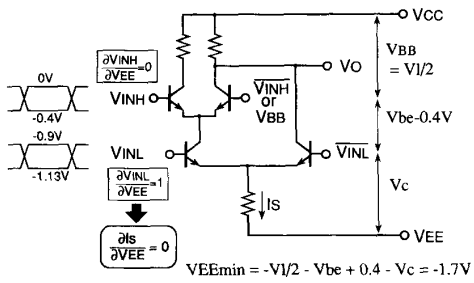


Fig. 2. Low-voltage Series-Gate (LSG).

should be around 3.0 V for 2-level series-gate circuits [4]. $VEE\,\min$ may depend on the circuit design. For example, when one needs an emitter follower, one Vbe should be added to this value.

The simplest solution for voltage lowering is to use a resistor, a MOSFET, and a current mirror, for a current source circuit. However, in these cases, it is difficult to control the switching current.

To reduce the power supply voltage, we merged a lower-input transistor of a series-gate circuit and a current source transistor, as shown in Fig. 2. It is basically similar to a 2-level series gate circuit with a resistor type current source. $VEE\,\min$ is described as:

$$VEE\,\min = -Vl/2 - Vbe + 0.4V - Vc. \tag{2}$$

This becomes -1.7 V. In addition, the circuit is modified in the following way. The lower-input voltage $VINL$ is usually set to 1 Vbe below the upper-input voltage ($VINL = VINH - Vbe$) in conventional LCML gates. Because it is independent of the power supply voltage $VEE\,(\partial VINL/\partial VEE = 0)$, the switching current and the logic swing change with VEE. Accordingly, the lower-input requires a special gate whose output characteristics correspond to a reference voltage Vcs used for a constant current source. The output of the special gate VTB (VEE-Traced Buffer) traces VEE variation ($\partial VINL/\partial VEE = 1$). This keeps the voltage between the high level of the lower-input and VEE constant. Also, the switching current is constant regardless of VEE. The typical high level of $VINL$ is -0.9 V and the low level is -1.13 V.

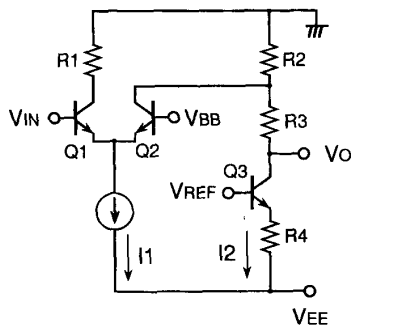
B. VEE-Traced Buffer (VTB)

Fig. 3(a) shows a basic circuit of VTB. The characteristics of the output voltage Vo should be the same as that of the reference voltage Vcs. It traces the power supply voltage VEE. When the input voltage Vin is "high," the transistor $Q2$ cuts off. Then the output voltage at high level VOH is presented as the following equation:

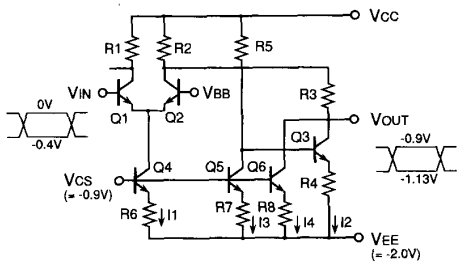
$$VOH = VCC - (R2 + R3) \cdot I2, \tag{3}$$

where

$$I2 = (VREF - VBE - VEE)/R4. \tag{4}$$



(a)



(b)

Fig. 3. VEE-Traced Buffer (VTB).

VOH is set to the same voltage as the reference voltage Vcs. As both sides of (3) are differentiated by VEE, the VEE-dependence of Vo is given by the following equation:

$$\frac{\partial VOH}{\partial VEE} = -\frac{(R2 + R3)}{R4}\left(\frac{\partial VREF}{\partial VEE} - 1\right). \tag{5}$$

This value becomes 1, if $\partial VREF/\partial VEE = 0$ and $R2 + R3 = R4$.

Since the dc characteristics of VOH are equal to Vcs and the output Vo only goes to the lower-input of the gate in the next stage, the switching current of the gate keeps constant regardless of VEE change.

When the input voltage is "low," the transistor $Q2$ turns on. Therefore, the output voltage VOL is represented as:

$$VOL = VCC - R2 \cdot (I1 + I2) - R3 \cdot I2. \tag{6}$$

Since, as mentioned above, the switching current $I1$ has no VEE dependence and $I2$ is independent of VEE,

$$\frac{\partial VOL}{\partial VEE} = 1. \tag{7}$$

(5) and (7) show that the output voltage swing is not affected by the power supply voltage.

A full schematic of VEE-Traced buffer is shown in Fig. 3(b). The VEE dependence of the base voltage of $Q3(VREF)$ is equal to 0, because Vcs traces VEE, and $I3$ is constant. $Q6$ and $R8$ are added to satisfy the condition $R2 + R3 = R4$. Vo at "high" level is determined by:

$$VOH = VCC - (R2 + R3)(I2 + I4), \tag{8}$$

where,

$$I2 = -(VCS - VEE - Vbe)R5/(R4 \cdot R7) - (VEE + Vbe)/R4, \quad (9)$$

$$I4 = (VCS - VEE - Vbe)R8. \quad (10)$$

Then the relation between VEE and VOH is given by:

$$\frac{\partial VOH}{\partial VEE} = \left(\frac{R5 \cdot (R2 + R3)}{R4 \cdot R7} - \frac{R2 + R3}{R8}\right)\left(\frac{\partial VCS}{\partial VEE} - 1\right) + \frac{R2 + R3}{R4} \quad (11)$$

where $Vcc = 0\,V$ and $\partial Vbe/\partial VEE \cong 0$.

The first term of the right side of the equation becomes zero because $\partial VCS/\partial VEE = 1$. Then (11) is simplified by:

$$\frac{\partial VOH}{\partial VEE} = \frac{R2 + R3}{R4}. \quad (12)$$

It should be noted that $R8$ has no influence on the $VEE - VOH$ relation. The usage of the transistor $Q6$ and the resistor $R8$ can adjust $R2 + R3$ to be the same as $R4$. Then $\partial VOH/\partial VEE$ becomes one. Thus, switching current on the following gate is stable while the power supply fluctuates.

When the input voltage is at "low" level, the transistor $Q2$ turns on and the output voltage Vo goes down by $I1 \cdot R2$. The logic swing of Vo is designed to be 230 mV. In the same way as VOH, the relation $\partial VOL/\partial VEE$ also becomes one.

The effect of temperature on Vo is obtained as follows. As both sides of (8) are differentiated by temperature T, the relation between temperature and VOH is given by

$$\frac{\partial VOH}{\partial T} = \frac{\partial}{\partial T}\left[-\frac{(R2 + R3)}{R4} \cdot \left\{\left(\frac{R4}{R8} - \frac{R5}{R7}\right)(Vcs - Vbe) - Vbe\right\}\right]. \quad (13)$$

Because the temperature coefficient of the resistor is almost constant regardless of resistant value, (13) becomes

$$\frac{\partial VOH}{\partial T} = -\frac{(R2 + R3)}{R4}\left\{\left(\frac{R4}{R8} - \frac{R5}{R7}\right) \cdot \left(\frac{\partial Vcs}{\partial T} - \frac{\partial Vbe}{\partial T}\right) - \frac{\partial Vbe}{\partial T}\right\}. \quad (14)$$

Since $R2 + R3 = R4$ and $\partial Vcs/\partial T$ is made equal to $\partial Vbe/\partial T$ in order to keep the switching current constant, (14) is represented as:

$$\frac{\partial VOH}{\partial T} = \frac{\partial Vbe}{\partial t} = \frac{\partial Vcs}{\partial T}. \quad (15)$$

Consequently, VEE and temperature dependence of the output voltage VOH of the VEE-traced buffer is the same as that of the reference voltage Vcs. VTB converts the input voltage with LCML level (VIH = 0 V, VIL = −0.4 V) to the output voltage (VOH = −0.9 V, VOL = −1.13 V). The output voltage traces VEE.

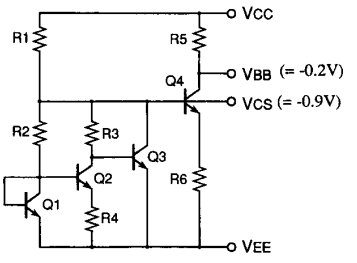


Fig. 4. Reference voltage generator.

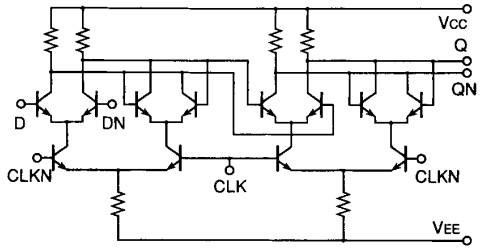


Fig. 5. LSG flip–flop.

C. Reference Circuit

We designed the reference voltage generator by using a bandgap reference circuit [5]. The circuit is optimized for the low-voltage operation. The reference circuit shown in Fig. 4 provides the threshold voltage VBB and the voltage Vcs for the constant-current source. These voltages are counterbalanced against the variations of the supply voltage and temperature. VBB is set to −0.2 V, which is used for upper inputs. Vcs is typically set to −0.9 V.

D. Master–Slave Flip–Flop

Fig. 5 shows a circuit diagram of the Master–slave flip–flop as an example of LSG. It adopts a two-level series-gate circuit and a resistor type current source. The data input D, DN, and the data outputs Q, QN, have a CML level (VH = 0 V and VL = −0.4 V). The clock inputs CLK and $CLKN$, which are the lower inputs of the series-gate, are driven by VTB. Consequently the switching current keeps constant with fluctuations in supply voltage and temperature. The typical switching current is 87 μA. The power dissipation of the flip–flop is 348 μW at a power supply voltage of 2 V.

III. Process Technology

The circuits are designed with 0.8-μm double-polysilicon self-aligned technology (DPSA) with trench isolation filled with HTO (High Temperature Oxide). The cross-sectional view of a transistor and a resistor is shown in Fig. 6. Device isolation and field isolation are achieved by using HTO deposition. The trench width and depth are 0.8 μm and 5 μm, respectively. The p+ polysilicon resistor and the base electrode are fabricated at the same process step. The sheet resistances

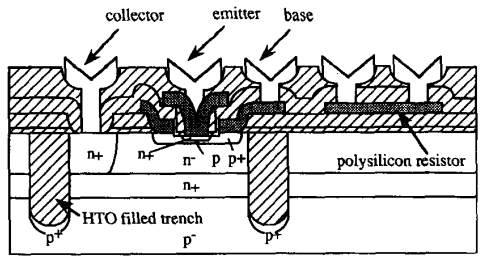


Fig. 6. Cross-sectional view of transistor.

TABLE I
TRANSISTOR PARAMETERS

0.8 μ m Double-Polysilicon Self-Aligned Technology with Trench Isolation	
Minimum Emitter Size	0.4 x 0.9 μ m^2
Breakdown voltage	BVceo > 7 V
Current gain	hFE = 100
Base-Collector Cap.	CTC = 4.0 fF
Base-Emitter Cap.	CTE = 3.8 fF
Collector-Sub. Cap.	CTS = 5.0 fF
Cut-off Frequency	fT = 12 GHz

of the polysilicon resistors are 300 Ω/square and 800 Ω/square, and the coefficients of temperature are 0 ppm and −400 ppm, respectively.

Table I summarizes the transistor parameters. The minimum emitter size is $0.4 \times 0.9\,\mu\mathrm{m}^2$. The emitter-collector breakdown voltage $BVceo$ is greater than 7 V. Dc current gain hFE is 100. The cut-off frequency fT is 12 GHz.

In order to compare the transistor performance fairly, we evaluated the conventional ECL gate fabricated on the same wafer. An intrinsic gate delay is 59 ps at 240 μA switching current for a conventional ECL gate. The power dissipation of the gate is 1.4 mW at $VEE = -4.0$ V with $0.5 \times 1.7\,\mu\mathrm{m}^2$ effective emitter size. An LCML gate delay is 69 ps at $VEE = -3.0$ V and a power dissipation of 0.72 mW. A toggle frequency of 5 GHz is obtained for an LCML flip–flop with a power dissipation of 3.04 mW.

IV. EXPERIMENTAL RESULTS

Fig. 7 shows a micrograph photo of a test chip to evaluate the LSG circuits. The chip size is 1.25 by 0.95 mm^2. The chip includes the block to measure the dc characteristics and the block to evaluate the speed performance.

A. Dc Characteristics

The supply voltage dependence of the output voltage of the reference circuit and VTB is shown in Fig. 8(a). The horizontal axis represents the power supply voltage VEE, and the vertical axis denotes the output voltage. The white circle shows the threshold voltage VBB, and black one is the reference voltage for a current source. The triangle shows the output voltage of VTB at "high" level. The $\partial VBB/\partial VEE$ is 0.074 V/V. This means the fluctuation of VBB is 22 mV when VEE swings between $-2.0\,\mathrm{V} \pm 15\%$. The relations $\partial VCS/\partial VEE$ and $\partial \mathrm{VOUT}/\partial VEE$ at "high" level are 0.892 V/V and 0.999 V/V, respectively. These are nearly equal to 1. This indicates that both Vcs and $Vout$ trace VEE well.

Fig. 8(b) shows the temperature dependence of VBB, Vcs, and Vout at "high" level. Vcs and Vout are designed to have negative dependence on temperature to keep the switching current constant.

As can be seen in these figures, the behavior of Vout is quite similar to that of Vcs.

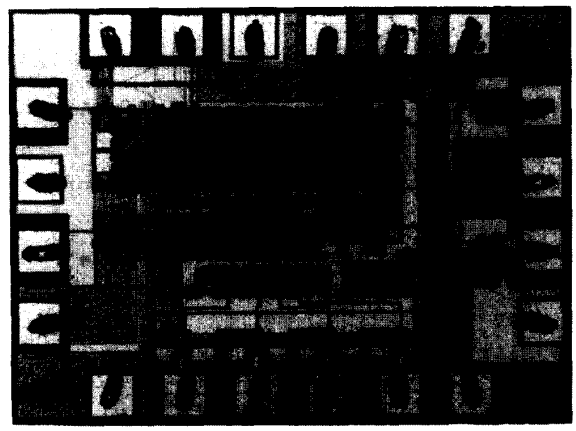
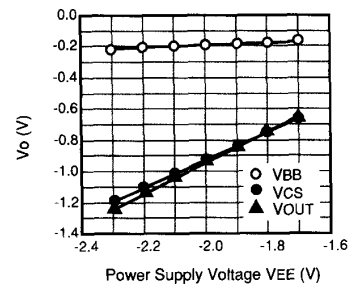
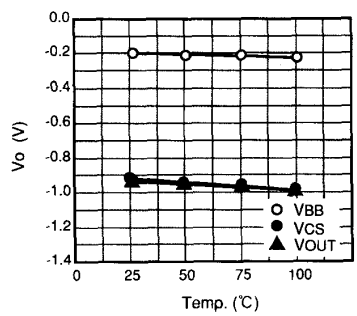


Fig. 7. Micrograph photo of test chip.



(a)



(b)

Fig. 8. Dc characteristics of Vcs and VTB.

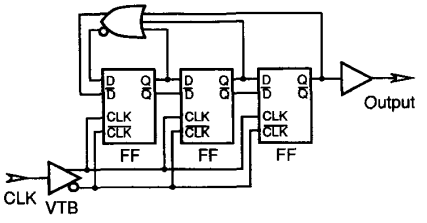


Fig. 9. 4-b counter block diagram.

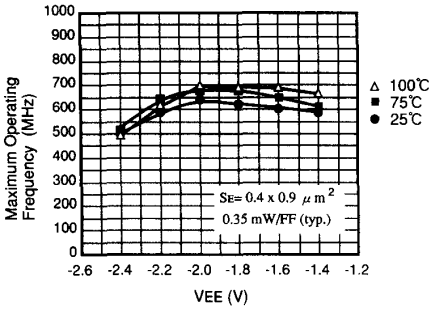


Fig. 10. Operating frequency variation of 4-b counter versus VEE.

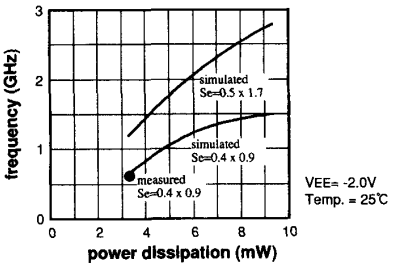


Fig. 11. Maximum operating frequency of 4-b counter.

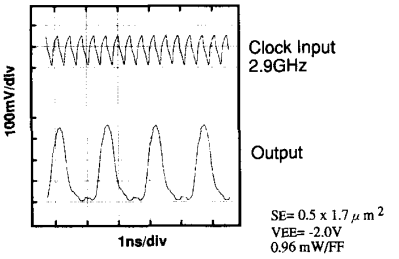


Fig. 12. Simulated wave form of 4-b counter.

B. Speed Performance

A 4-b counter, as shown in the block diagram in Fig. 9, is implemented on the chip to evaluate the speed performance. Three master–slave flip–flops are implemented using the low-voltage series-gate circuits while 3-input OR/NOR gate is conventional LCML circuit. The VEE-traced buffer, which has differential outputs, acts as a clock driver.

Fig. 10 shows the measured maximum operating frequency of the 4-b counter. These three curves indicate the measurement data at 25, 75, and 100°C. The circuit is realized using transistors with minimum emitter size of $0.4 \times 0.9\,\mu\mathrm{m}^2$. The maximum operating frequency of 640 MHz is obtained under the condition of $VEE = -2.0$ V and the temperature = 25°C. The power dissipation of the 4-b counter is 3.3 mW at -2.0 V (excluding output buffers and reference circuits). The circuit operation at over 500 MHz covers the wide range of the supply voltage from -2.4 V to -1.4 V. However, the voltage swing becomes small at -1.4 V because of the saturation of the lower input transistor. Furthermore, it does not work at -1.3 V. The lower limitation for practical use is -1.6 V. The measurement data shows stable operation with both VEE and temperature fluctuation.

In Fig. 11, the lower curve indicates the simulated data with the emitter size of $0.4 \times 0.9\,\mu\mathrm{m}^2$ and the higher one is that with the emitter size of $0.5 \times 1.7\,\mu\mathrm{m}^2$. The black point is the measured data (640 MHz with 3.3 mW; this work). The simulation result shows the 4-b counter operates at 2.9 GHz. Fig. 12 shows the simulated output wave form of the 4-b counter with the emitter size of $0.5 \times 1.7\,\mu\mathrm{m}^2$. The power dissipation of the 4-b counter and a flip–flop are 9.3 mW and 0.96 mW, respectively.

V. Conclusion

The low-voltage series-gate bipolar circuit (LSG) and the VEE-traced buffer (VTB) have been described. The dc characteristics of the VTB output remain stable while a power supply voltage or temperature deviates. A 4-b counter is fabricated with 0.8-μm double polysilicon self-align process to evaluate this circuit technology. The 4-b counter operates at 640 MHz with the power dissipation of 3.3 mW. It proves stable operation at -1.6 V. The circuit covers a wide range of VEE. It is scarcely affected by fluctuations in VEE or temperature. According to the simulation data, the 4-b counter operates at 2.9 GHz with 9.3 mW power dissipation. These results indicate that the circuit is suitable for low-voltage, high-speed applications.

Acknowledgment

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References

[1] Y. Horiba *et al.*, "A bipolar 2500-gate subnanosecond masterslice LSI," *IEEE ISSCC Dig. Tech. Papers,* pp. 228–229, Feb. 1981.
[2] C. L. Chen, "2.5 V bipolar/CMOS circuits for 0.25 μm BiCMOS technology," *Symp. on VLSI Circuits, Dig. of Tech. Papers,* pp. 121–122, May 1991.
[3] B. Razavi *et al.*, "Low voltage techniques for high speed digital bipolar circuits," *Symp. on VLSI Circuits, Dig. of Tech. Papers,* pp. 31–32, May 1993.
[4] M. Suzuki *et al.*, "43-ps 5.2-GHz macrocell array LSI's," *IEEE J. Solid-State Circuits,* vol. 23, no. 5, pp. 1182–1188, Oct. 1988.
[5] R. J. Widlar, "New developments in IC voltage regulators," *IEEE J. Solid-State Circuits,* vol. 6, no. 1, pp. 2–7, Feb. 1971.

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