A Figure of Merit for the High-Frequency Noise Behavior of Bipolar Transistors

L. C. N. de Vreede, H. C. de Graaff, G. A. M. Hurkx, J. L. Tauritz, and R. G. F. Baets

Abstract—**In this paper a new Figure of Merit for high frequency noise behavior for use in the evaluation and development of bipolar silicon process technology is introduced. Basic low noise design rules for optimum transistor biasing and emitter scaling are proposed.**

I. Introduction

In ANALOG signal processing the noise behavior of the electronic circuits is of paramount importance, especially at higher frequencies, where the noise factor increases significantly. In this paper a new Figure of Merit (FOM) for the high-frequency noise behavior of a bipolar transistor, driven by a purely resistive source, is defined. This FOM (which should not be confused with the noise factor, sometimes also called noise figure) is shown to be convenient for assessing silicon technological development with respect to high-frequency noise behavior. In conclusion, a comparison with capacitive sources is carried out illustrating the applicability of the FOM in practical situations where the applied sources are non-ohmic.

We start from a simple Ebers-Moll model but take into account the base resistance and the influence of the emitter resistance and derive an expression for the noise factor as function of frequency, bias current and device geometry [1]. The Figure of Merit proposed, is defined as follows:

$f_{FC(\mathrm{dB})}$ = the *frequency* at which the noise factor F, optimized with respect to bias current and device geometry, has increased to a specified value (e.g., $F = 1.5$ or 2.0 dB).

This optimization relates the proposed Figure of Merit to technological processes rather than to devices. Using the formulas to be presented, insight can be gained in the high-frequency noise behavior of a given process, thereby obviating the need for full transistor characterization and extensive computations.

II. The Noise Model of the First Stage Transistor

As starting point for our noise study, we use the circuit shown in Fig. 1. In this figure, the basic bipolar transistor equivalent circuit is given with its dominant noise sources and ohmic input circuit. The $1/f$ noise of the base current and the shot noise of the collector leakage current are neglected. All noise sources are assumed to be white and uncorrelated. The resulting noise power spectral components are:

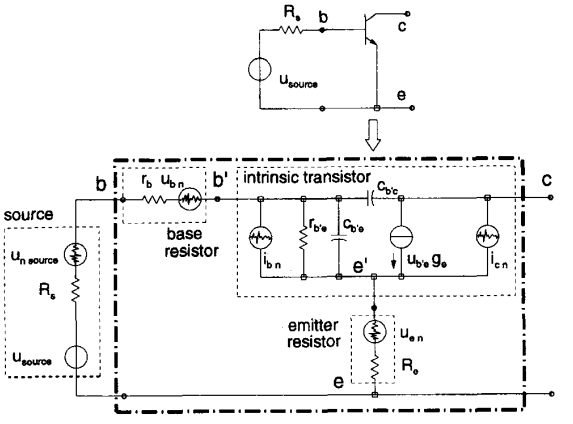

Fig. 1. Ebers-Moll noise model of a bipolar transistor with base and emitter resistance.

Power spectrum	Thermal equivalent	
$S(i_c) = 2.q.I_c$	$= 2.k.T.g_e$	(1)
$S(i_b) = 2.q.I_b = 2.q.\frac{I_c}{h_{FE}}$	$= 2.k.T.\frac{g_e}{h_{FE}}$	(2)
$S(u_b)$	$= 4.k.T.r_b$	(3)
$S(u_e)$	$= 4.k.T.R_e$	(4)

with:

$$g_e = \frac{1}{r_e} = \frac{q.I_c}{k.T} \tag{5}$$

III. The Derivation of the Noise Factor F for a Purely Ohmic Source

The source impedance R_s is considered to be purely ohmic with its own noise source $u_{n\ \mathrm{source}}$. The calculation of the noise factor F is now straightforward and is defined as the ratio of the total available noise to the noise of the source impedance at room temperature (290°K) [2].

$$F = \frac{\overline{u^2_{n\ \mathrm{source}}} + \overline{u^2_{n\ \mathrm{network}}}}{\overline{u^2_{n\ \mathrm{source}}}}$$

For the calculation of $u_{n\ \mathrm{network}}$ the remaining noise sources of the transistor should be transformed to one single source

Manuscript received January 31, 1994.

L. C. N. de Vreede, H. C. de Graaff, J. L. Tauritz, and R. G. F. Baets are with the Delft University of Technology, Dept. of Electrical Engineering, Laboratory for Telecommunication and Remote Sensing Technology, 2600 GA Delft, the Netherlands.

G. A. M. Hurkx is with Philips Research Laboratories, 5600 J. A. Eindhoven, the Netherlands.

IEEE Log Number 9404520.

0018-9200/94$04.00 © 1994 IEEE

using a Thevenin representation. A straightforward approach for calculating $u_{n\ \text{network}}$ for the circuit of Fig. 1 using noise correlation matrices [3], [4] leads to very cumbersome equations, difficult to handle and masking insight. A more fruitful approach is to simplify the circuit of Fig. 1 by eliminating the emitter resistance R_e while taking into account its noise contribution.

In effect, we neglect the influence of R_e on the ac signal transfer and transfer R_e's associated thermal noise source to the input. The influence of the emitter resistor R_e can be investigated by studying a chain parameter description of the intrinsic transistor combined with the emitter resistance. The chain parameters, which relate the output directly to the input quantities, are defined as follows:

$$\begin{bmatrix} U_1 \\ I_1 \end{bmatrix} = \begin{bmatrix} A & B \\ C & D \end{bmatrix} \cdot \begin{bmatrix} U_2 \\ I_2 \end{bmatrix}.$$

Based on the equivalent small signal circuit of a bipolar transistor with its parasitic resistors r_b and R_e in Fig. 1, we can (using Kirchof's Voltage Law) carry out a Blakesley transformation or e-shift [5] leading us to the situation of Fig. 2. The resulting voltage noise source in the collector branch can be neglected. The noise source due to the emitter resistance in the base branch can be directly combined with the one due to the base resistance by replacing these with a single source of value $4kT(r_b+R_e)$. Consequently, for the remainder of this paper the noise contribution of the emitter resistance is modeled simply by adding its numerical value to the base resistance r_b and ignoring the existence of R_e in the rest of our calculations. This simplifies our calculations considerably and (as has been numerically verified) gives a good approximation of the ac signal transfer as long as $R_e.g_e \ll 1$. Following this simplification a chain matrix transformation [6], [7] for the collector shot noise source is applied yielding the situation of Fig. 3. The relevant chain matrix parameters of the intrinsic bipolar transistor are given below:

$$B_{\text{tr}} = \frac{-1}{g_e - j\omega C_{b'c}} \qquad D_{\text{tr}} = -\left[\frac{\frac{1+j\omega r_{b'e}C_{b'e}}{r_{b'e}} + j\omega C_{b'c}}{g_e - j\omega C_{b'c}}\right].$$

For the condition that $\omega.r_e.C_{b'c} \ll 1$ these expressions can be simplified to:

$$B_{\text{tr}} = -r_e \qquad D_{\text{tr}} = -\left[\frac{1}{\beta} + j\frac{f}{f_T}\right] \tag{6}$$

with current gain and cut-off frequency given by:

$$\beta = g_e.r_{b'e}, \quad f_T = \frac{g_e}{2\pi(C_{b'e} + C_{b'c})}. \tag{7}$$

$C_{b'e}$ is the sum of the emitter diffusion and depletion capacitances $(ge.\tau_0 + c_{TE})$, in which τ_0 is the base transit time. In forward operation $C_{b'c}$ is equal to the collector depletion capacitance c_{TC}, so that the cutoff frequency may be written as:

$$f_T = \frac{1}{2\pi(r_e(c_{TE} + c_{TC}) + \tau_0)}. \tag{8}$$

This expression takes into account the emitter geometry. Based on Fig. 3 the noise voltage $u_{n\ \text{network}}$, expressed in terms of

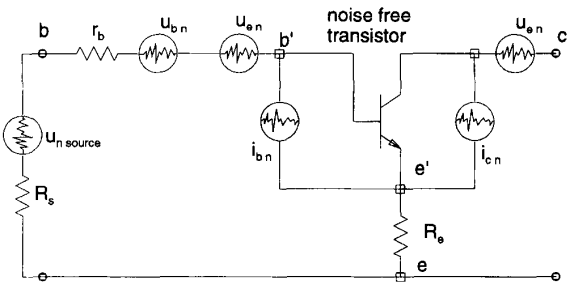

Fig. 2. Blackwell or e-shift of the emitter resistance noise source.

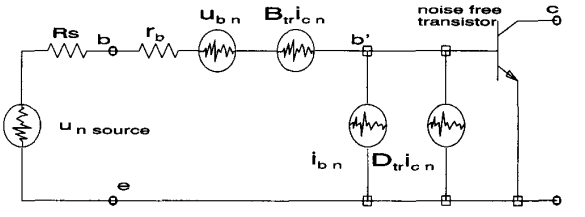

Fig. 3. Transformation of the noise sources to the input using a chain matrix representation.

the chain parameters of the transistor, is on inspection:

$$u_{n\ \text{network}} = u_{bn} + (R_s + r_b)i_{bn} + (B_{\text{tr}} + D_{\text{tr}}(R_s + r_b))i_{cn}$$

Using the simplified expressions for the chain matrix parameters of (6) we obtain for the noise factor:

$$F = 1 + \frac{1}{R_s}\left[r_b + \frac{r_e}{2} + \frac{(r_b + R_s)(r_b + R_s + 2r_e)}{2r_e\beta} + \frac{(r_b + R_s)^2}{2r_e\beta^2} + \frac{(r_b + R_s)^2}{2r_e} \cdot \left[\frac{f}{f_T}\right]^2\right]$$

In the dc limit when f approaches zero it can be shown that this is exactly equivalent to the result of van der Ziel [2]. If we assume $\beta \gg 1$ and $\omega r_e C_{b'c} \ll 1$ we can further simplify our calculations, without introducing serious error, to the formulation for the noise factor given in [7]:

$$F \approx 1 + \frac{1}{R_s}\left[r_b + \frac{r_e}{2} + \frac{(r_b + R_s)^2}{2\beta r_e} + \frac{(r_b + R_s)^2}{2r_e} \cdot \left(\frac{f}{f_T}\right)^2\right]. \tag{9}$$

This expression for the noise factor takes into account the current gain β, the base resistance r_b, the delay time τ_0 and the depletion capacitances c_{TE} and c_{TC}. This is in contrast with the noise analysis of Hawkins [8] and van der Ziel [2] which neglect the base collector capacitance $C_{b'c}(\approx c_{TC})$. In the analysis of [2] however, the correlation between collector and base shot noise sources (which occurs at high frequencies) has been included. This is an effect which manifests itself most clearly when determining the optimum noise reflection parameter (which is needed to achieve the minimum noise factor) for devices with an extremely low base resistance. This correlation is a second order effect which would unnecessarily complicate our equations and has thus been ignored.

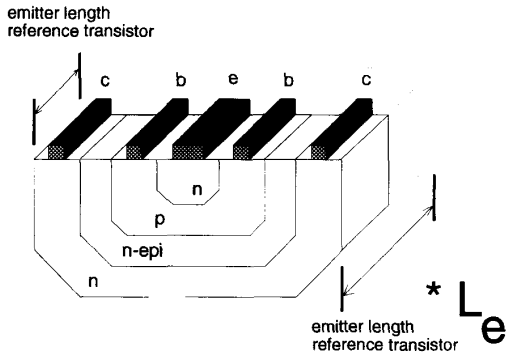

Fig. 4. Scaling the emitter length of the reference device.

IV. Introduction of Normalization and Scaling

To obtain a noise FOM independent of the source impedance level, normalization and scaling of the device under consideration have proven useful. In the remainder of this paper we introduce a reference transistor that is representative for a particular process. This reference transistor is described by the parameters τ_0, β, r_b, c_{TE} and c_{TC}; the parameters τ_0 and β are mainly process dependent, r_b, c_{TE} and c_{TC} are also dependent on geometry. For optimization purposes, we introduce the emitter length multiplication factor L_e (see Fig. 4), being the *ratio* of the emitter length of the transistor under consideration and the reference transistor. We assume that the depletion capacitances are linearly proportional to the multiplication factor L_e and that the base resistance is inversely proportional to L_e. So for a transistor with an arbitrary multiplication factor (9) becomes:

$$F \approx 1 + \frac{1}{R_s} \times \left[\frac{r_b}{L_e} + \frac{r_e}{2} + \frac{\left(\frac{r_b}{L_e} + R_s\right)^2}{2\beta r_e} + \frac{\left(\frac{r_b}{L_e} + R_s\right)^2}{2r_e} \cdot \left(\frac{f}{f'_T}\right)^2 \right] \tag{10}$$

where f'_T is:

$$f'_T = \frac{1}{2\pi . r_e . L_e (c_{TE} + c_{TC}) + \tau_0}.$$

Normalization results in the following:

$$F = 1 + \frac{1}{s} + \frac{1}{2}r + \frac{\left(1 + \frac{1}{s}\right)^2}{2\beta r} + \frac{\left(1 + \frac{1}{s}\right)^2}{2r}(\tau + sr)^2\Omega^2 \tag{11}$$

where:

$$r = \frac{r_e}{R_s}, \qquad s = \frac{R_s}{r_b} \cdot L_e$$
$$\tau = \frac{\tau_0}{r_b(c_{TE}+c_{TC})} \qquad \Omega = 2\pi r_b (c_{TE} + c_{TC}) f.$$

The normalized quantities r, τ and Ω are geometry-independent; τ is the ratio of the time constant determined by $r_b(c_{TE} + c_{TC})$ and the transit time τ_0.

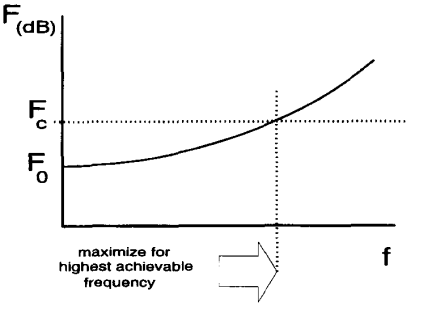

Fig. 5. Maximization of the bandwidth by optimizing for the scale.

V. Optimization for Bias and Device Geometry

Noting that r_e and thus r are current-dependent, the noise factor can be optimized with respect to the bias condition. We assume that τ_0, c_{TE}, c_{TC} and r_b are current-independent. The optimization is carried out by solving for the minimum in the noise factor function:

$$\frac{dF}{dr} = 0 \Rightarrow r_{\text{opt}} = \left(1 + \frac{1}{s}\right)\sqrt{\frac{\frac{1}{\beta} + \Omega^2\tau^2}{1 + (1+s)^2\Omega^2}}. \tag{12}$$

Substituting in (11) yields:

$$F_{\text{ropt}}(s) = 1 + \frac{1}{s} + \left(1 + \frac{1}{s}\right)^2 s\tau\Omega^2 + \left(1 + \frac{1}{s}\right) \times \sqrt{\left(\frac{1}{\beta} + \Omega^2\tau^2\right)(1 + (s+1)^2\Omega^2)}. \tag{13}$$

This is a function of the normalized frequency Ω and normalized scaling factor s. Determination of an optimum value for s is not straightforward. In particular at low frequencies ($F = F_0$) there is no distinct optimum for s. This problem may be circumvented by setting the noise factor to a constant arbitrary value $F_c > F_0$ (e.g., 2 or 3 dB) and maximizing the corresponding frequency (see Fig. 5) by differentiating $\tau\Omega^2$ with respect to s. Replacing $F_{\text{ropt}}(s)$ by the constant F_c and writing the frequency-dependent parameters explicitly we obtain:

$$\tau\Omega^2 = \frac{\left(\frac{sF_c}{1+s} - 1\right)^2 - \frac{1}{\beta}}{2s(F_c - 1) - 2 + \tau + \frac{1}{\beta\tau}(1+s)^2}. \tag{14}$$

Putting $d(\tau\Omega^2)/d(s) = 0$ and neglecting minor terms (assuming large β) leads to:

$$s_{\text{opt}} \approx \frac{1}{2} \cdot \frac{2 + F_c + \sqrt{F_c}\sqrt{F_c + 4\tau}}{F_c - 1}. \tag{15}$$

Substituting s_{opt} in (14) and using the definitions of Ω and τ we solve for our Figure of Merit, namely; the frequency f_{Fc} for which the noise factor reaches the value F_c.

$$f_{F_c} = \sqrt{\frac{\max(\tau\Omega^2)}{4\pi^2\tau_0 . r_b (c_{TE} + c_{TC})}} \tag{16}$$

Here $\max(\tau\Omega^2)$ is the right-hand side of (14) for $s = s_{\text{opt}}$.

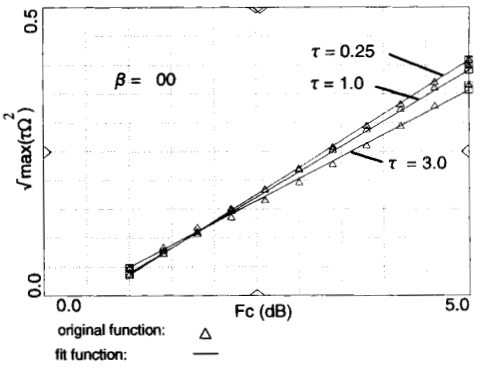

Fig. 6. The function $\sqrt{\max(\tau\gamma^2)}$ with its fit function for = 100.

This defines our Figure of Merit with respect to the high-frequency noise behavior of the bipolar transistor. The function $\sqrt{\max(\tau\Omega^2)}$ complicates the use of (16). We have found it expedient to replace the function $\sqrt{\max(\tau\Omega^2)}$ by a fit function. In Fig. 6 $\sqrt{\max(\tau\Omega^2)}$ is plotted as function of F_c (in dB's) with τ as parameter.

$$f_{Fc\ (\mathrm{dB})} \approx \frac{0.011\tau - 0.05 - \frac{1}{\beta} + \frac{F_{c\ (\mathrm{dB})}}{0.842\tau + 10.53}}{\sqrt{4\pi^2\tau_0 r_b(c_{TE} + c_{TC})}}. \tag{17}$$

Alternatively, the fit function may be used to compute the optimized noise factor corresponding to a given bandwidth and process parameters:

$$F_{c(\mathrm{dB})} \approx (0.842\tau + 10.53) \times \left(f_{Fc\ (\mathrm{dB})}\sqrt{4\pi^2\tau_0 r_b(c_{TE} + c_{TC})} - 0.011\tau + 0.05 + \frac{1}{\beta}\right). \tag{18}$$

VI. Choice of the Parameter Values

The capacitances c_{TE} and c_{TC}, although slightly bias dependent, have been treated as constant in the optimization process. Realistic values for c_{TE} and c_{TC}, corresponding to the normal forward bias condition must be employed. To avoid overly optimistic results we take $c_{TE} = 2.C_{je}$ (twice the zero bias emitter-base depletion capacitance) and $c_{TC} = C_{jc}$ (the zero bias collector-base depletion capacitance).

We also assume r_b to be independent of the bias current, but we take the width modulation of the neutral base into account by lowering the base resistance under the emitter, using [9]:

$$r_b = R_{BC} + \frac{R_{BV}}{1 + \frac{C_{je}V_{DE}}{Q_{BO}}} \tag{19}$$

in which:

R_{BC} the constant part of the base resistance,
R_{BV} maximum of the variable part of the base resistance,
V_{DE} emitter-base diffusion voltage, and
Q_{B0} the base charge at zero bias.

We have chosen $\beta \approx h_{FE\ \max}$; τ_0 is obtained by extrapolating from the f_T characteristic at $V_{bc} = 0$.

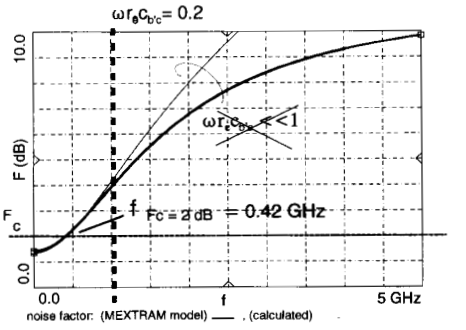

Fig. 7. The computed noise factor for the optimized device of process A.

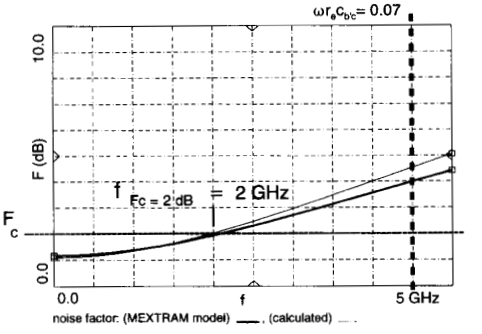

Fig. 8. The computed noise factor for the optimized device of process B.

VII. Results

In order to test the validity of our calculations and approximations the accurate compact transistor model MEXTRAM [9] as implemented at the TU-Delft in Hewlett-Packard's Microwave Design System (MDS) has also been used to calculate the noise factor. The MEXTRAM model combines the benefits of a compact circuit model with the accuracy and insight of a physical device model.

The transistors were optimized in scale and bias to maximize the frequency at which the noise factor reaches the value of 2 dB (F_c = 2 dB). The optimized multiplication factor for the length of the emitter becomes:

$$L_{e\ \mathrm{opt}} = s_{\mathrm{opt}} \cdot \frac{r_b}{R_s}. \tag{20}$$

We have treated three different processes, namely: a conventional oxide-isolated process (A), a modern production process [10] (B) and an advanced experimental process [11] (C). The calculated noise factor as function of frequency is plotted in Fig. 7, 8 and 9 for these three processes using the previously developed equations and the complete MEXTRAM model. It is clear from these figures that for frequencies where $\omega r_e C_{b'c} \ll 1$ both curves fit tightly. The results are summarized in Table I.

In these figures the analytical calculations neglect the emitter resistance R_e. This can be noted in Fig. 9 which is related to a modern device with a relatively high emitter resistance. Here, the constant difference in level between the two calculated noise factors is caused by the absence of R_e

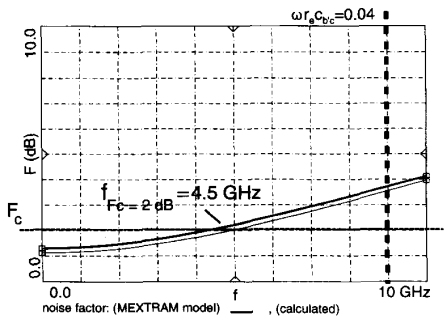

Fig. 9. The computed noise factor for the optimized device of process C.

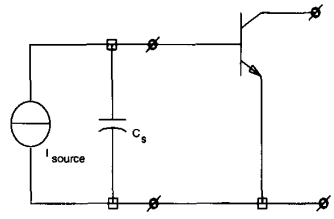

Fig. 10. A bipolar transistor with a capacitive source impedance.

TABLE I
OVERVIEW CALCULATION f_2 dB AND Lopt.

Process	A	B	C
$f_{Fc=2\,dB}$ num. optimized (GHz)	0.41	2.1	4.37
$f_{Fc=2\,dB}$ (eq. (16)) (GHz)	0.423	1.97	4.92
$f_{Fc=2\,dB}$ (eq. (17)) (GHz)	0.446	1.9	4.65
$L_{e\,opt}$ num. optimized	54.56	53.5	32.6
s_{opt} (eq.(15))	4.76	6.46	6.08
$L_{e\,opt}$ (eq. (20)) using s_{opt} (eq. (15))	60	57.3	30.4

in our equations. If we, however, modify the value of the base resistance by adding the emitter resistance R_e to it, the resulting curve will coincide with the numerical simulation.

VIII. FURTHER JUSTIFICATION OF THE USE OF THIS FIGURE OF MERIT

It is interesting to know if this Figure of Merit is also valid for silicon process comparison in the event that the source impedance is not purely ohmic. We consider further a signal source that is purely capacitive (see Fig. 10). This situation can be found in the case of a photodiode or capacitive sensor as signal source. With a capacitive source the use of the noise factor F is no longer convenient; it is more logical to transform the noise sources of the bipolar transistor to one single equivalent current noise source at the input. The value

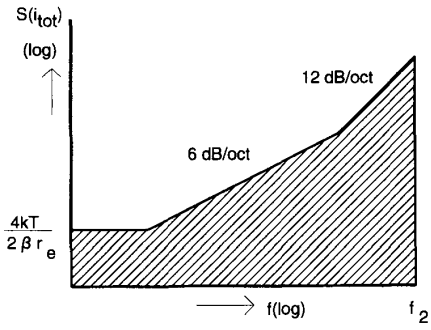

Fig. 11. Spectrum of $S_{(itot)}$ of a bipolar transistor with a capacitive source.

of this current noise source is given by:

$$i_{\rm tot} = u_{bn}Y_s + i_{bn}(r_bY_s + 1) + i_{cn}(B_{\rm tr}Y_s + D_{\rm tr}(r_bY_s + 1))$$

with:

$$Y_s = j\omega C_s.$$

Using the description of the first stage transistor as given in Section 3 and ignoring some minor terms, the following noise spectrum of the equivalent noise current at the input may be found:

$$S(i_{\rm tot}) = 4kT\left[\left(r_b + \frac{r_e}{2}\right)\omega^2C_s^2 + \frac{\omega^2C_s}{\omega_T} + \frac{1}{2r_e}\left(\frac{1}{\beta} + \frac{\omega^2}{\omega_T^2}\right)(1 + \omega^2C_s^2r_b^2)\right]. \quad (21)$$

In wide-band amplifiers one is interested in the equivalent noise current at the input for a given bandwidth f_2 and source capacitance C_s. To obtain the equivalent noise current we integrate the noise spectrum over the bandwidth f_2, yielding:

$$\overline{i_{\rm tot}^2} = 4kTf_2\left[\frac{1}{3}\left(r_b + \frac{r_e}{2}\right)\omega_2^2C_s^2 + \frac{1}{3}\frac{\omega_2^2Cs}{\omega_T} + \frac{1}{2\beta r_e}\left(1 + \frac{1}{3}\omega_2^2r_b^2C_s^2\right) + \frac{\omega_2^2}{2r_e\omega_T^2}\left(\frac{1}{3} + \frac{1}{5}\omega_2^2C_s^2r_b^2\right)\right]. \quad (22)$$

The noise spectrum of (21) is plotted in Fig. 11; the shaded area below the curve is a measure of $\overline{i_{\rm tot}^2}$. Restricting ourselves to the dominant terms for the linear and quadratic region of the noise spectrum as depicted in Fig. 11 (which is usually valid in the case of wide band amplifiers) and scaling with respect to the emitter length using: $r_b \Rightarrow r_b/L_e$ and $\omega_T = 1/(r_e \cdot L_e \cdot C_T + \tau_0)$ where $C_T = c_{TE} + c_{TC}$ we can reduce (22) to:

$$\frac{\overline{i_{\rm tot}^2}}{4kTf_2} = g_1 + g_2^2r_e + \frac{h}{r_e}$$

$$g_1 \approx \frac{1}{3}\omega_2^2C_s^2\left[\frac{r_b}{L_e} + \frac{\tau_0}{C_s} + \frac{L_e\tau_0C_T}{C_s^2}\right],$$

$$g_2^2 \approx \frac{1}{6}\omega_2^2C_s^2\left[1 + \frac{L_eC_T}{C_s}\right]^2,$$

$$h \approx \frac{1}{2}\left[\frac{1}{\beta} + \frac{1}{3}\omega_2^2\tau_0^2\right]. \quad (23)$$

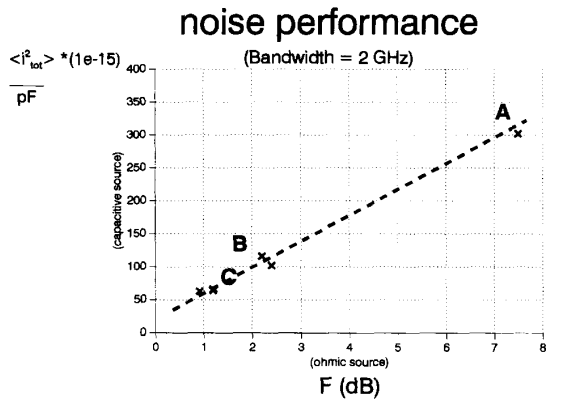

Fig. 12. Correlation in noise performance for optimized devices of different processes using a capacitive as well an ohmic souce impedance for a bandwidth of 2 GHz.

Optimizing $\overline{i_{\text{tot}}^2}$ with respect to the bias condition (r_e) and the scaling factor (L_e) we obtain (see Appendix A):

$$\frac{\overline{i_{\text{tot}}^2}}{4kTf_2} \approx \frac{1}{3}\omega_2^2 C_s \left[\tau_0\left(1+\sqrt{1+\frac{3}{\beta\omega_2^2\tau_0^2}}\right)+2 \times\sqrt{r_b C_T \tau_0\left(1+\sqrt{1+\frac{3}{\beta\omega_2^2\tau_0^2}}\right)}\right]. \quad (24)$$

Equation (24) gives the equivalent noise current for a bipolar input stage with a capacitive source impedance optimized both for bias and geometry. Note that the expression found allows us to normalize for the capacitance, so that it is possible to define the equivalent noise current per pF for a given bandwidth. The equivalence noise current per pF for a bandwidth of 2 GHz has been calculated for a number of processes using (24) and plotted in relation to the results found for an ohmic source using (18) (see Fig. 12). From this we can conclude that the Figure of Merit as proposed is a real measure of quality for a given silicon process even when the source impedances are capacitive.

For inductive sources a similar approach can be used. In this case, however, optimization of the emitter length with respect to the noise behavior will tend to give a resonant solution for the input circuit, consisting of the source inductance and the depletion capacitances c_{TE} and c_{TC}. This resonance, although useful in reducing the noise level will, in general, significantly deteriorate the transfer characteristic of the amplifier. For this reason we find that a device optimized in bias and geometry for a purely inductive source is of limited interest for the wide band amplifier case. A more detailed treatment is beyond the scope of this paper.

IX. Conclusion

A new Figure of Merit for the high-frequency noise behavior of a bipolar transistor with optimum bias and emitter length has been presented. We have kept the expressions as compact as possible while taking into account all dominant parameters with respect to noise. Using the results, process technologies may be rated with respect to their high-frequency noise behavior, without requiring full transistor parameter sets. This Figure of Merit for high-frequency noise behavior can be useful to process developers and designers in assessing competing technologies.

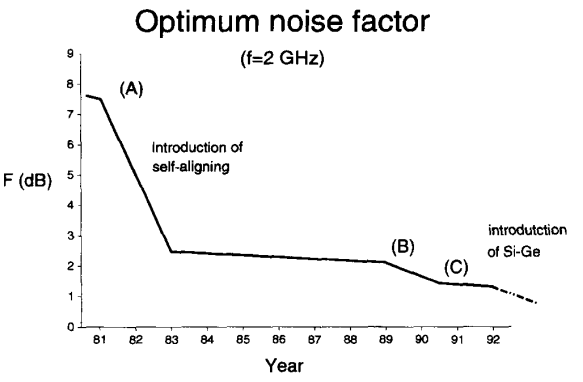

Fig. 13. High frequency noise behavior of silicon IC technology.

TABLE II
Recent Processes with Their Noise Performance

	Hitachi [11]	Siemens [14]	Toshiba [12]
$f_{Fc=2\,dB}$ (GHz)	4.5	4.65	5.38
$F_{c\,(2\,GHz)}$ (dB)	1.2	1.19	0.91

As a final illustration progress in silicon process technology with respect to high-frequency noise behavior is reviewed in Fig. 13. $F_{cf\,=\,2\,\text{GHz}}$ has been plotted for processes from 1981 to the present. The introduction around 1982 of self-aligned bipolar process technology [15] resulted in a substantial decrease in the lowest achievable noise factor for a given bandwidth. Self-aligning, which facilitates the use of smaller geometries in combination with other technological improvements, has led to large reductions in base resistance and depletion capacitances due to the smaller lateral dimension and the availability of very shallow junctions leads to a reduction of the delay time τ_0. For the moment, performance is relatively stable, yielding a noise factor of approximately 1 dB at 2 GHz. Results for a number of recently described processes are listed in Table II. We anticipate that the further maturation of silicon-germanium IC processes will lead to significant reductions in the noise factor.

X. Appendix A: Optimization for the Bias Condition and Geometry for a Capacitive Source Impedance

Optimizing $\overline{i_{\text{tot}}^2}$ of (23) with respect to the bias condition (r_e) we find for $r_{e\ \text{opt}}$:

$$r_{e\ \text{opt}} = \frac{\sqrt{h}}{g_2}; \quad (A.1)$$

substitution of $r_{e\ \mathrm{opt}}$ in (23) yields:

$$\frac{\overline{i_{\mathrm{tot}}^2}}{4kTf_2} = \frac{1}{3}\omega_2^2 C_s^2 \left[\frac{\tau_0}{C_s}\left(1+\sqrt{1+\frac{3}{\beta\omega_2^2\tau_0^2}}\right) + \frac{r_b}{L_e} + L_e \frac{C_T\tau_0}{C_s^2}\left(1+\sqrt{1+\frac{3}{\beta\omega_2^2\tau_0^2}}\right)\right], \quad \text{(A.2)}$$

which leads in turn to the following optimum for $L_{e\ \mathrm{opt}}$:

$$L_{e\ \mathrm{opt}} = \frac{C_s}{C_T}\sqrt{\frac{r_b C_T}{\tau_0\left(1+\sqrt{1+\frac{3}{\beta\omega_2^2\tau_0^2}}\right)}}. \quad \text{(A.3)}$$

Substitution of $L_{e\ \mathrm{opt}}$ in (A.2) results in (24).

REFERENCES

[1] Original idea of A. Jongepier of Philips Research Lab, Eindhoven.

[2] A. V. D. Ziel, *Noise in Solid State Devices and Circuits*. New York: Wiley, 1986.

[3] H. A. Haus and R. B. Adler, *Circuit Theory of Linear Noisy Networks*. New York: Wiley, 1959.

[4] H. Hillbrand and P. H. Russer, "An efficient method for computer aided noise analysis of linear amplifier networks," *IEEE Trans. Circuits and Syst.*, vol. 23, pp. 235–238, April 1976.

[5] S. Seshu and N. Balabanian, *Linear Network Analysis*. New York, Wiley, 1957, pp. 96–97.

[6] H. Rothe and W. Dahlke, *Proc. IRE*, 1956, vol. 44, pp. 204–213.

[7] E. H. Nordholdt, *Design of High-Performance Negative Feedback Amplifiers*. Amsterdam: Elsevier Scientific, 1983.

[8] R. J. Hawkins, "Limitations of Nielsen's and related noise equations applied to microwave bipolar transistors, and a new expression for the frequency an current dependent noise figure," *Solid State Electron.*, vol. 20, pp. 191–196, 1977.

[9] H. C. de Graaff, F. M. Klaassen, *Compact Transistor Modelling for Circuit Design*. New York: Springer-Verlag, 1990.

[10] J. de Jong, R. Lane, B. van Schravendijk and G. Conner, "Single polysilicon-layer advanced super high speed BiCMOS technology," in *Proc. BCTM*, Minneapolis, MN, 1989.

[11] Toshiro Hiramoto *et al.*, "A 27 GHz double polysilicon bipolar technology on bonded SOI with embedded 58 μm^2 CMOS memory cells for ECL-CMOS SRAM applications," *IEEE-IEDM Tech. Dig.*, pp. 39–42, 1992.

[12] Y. Katsumata, N. Itoh, H. Nakajima, K. Inou, T. Iinuma, S. Matsuda, C. Yoshino, Y. Tsuboi and H. Iwai, "Sub-20 ps ECL bipolar technology with high breakdown voltage," in *Proc. ESSDERC 93*, pp. 133–13.

[13] J. Hauenschild, A. Felder, M. Kerber, H.-M, Rein and L. Schmidt, "A 22 Gb/s decision circuit and a 32 Gb/s regenerating demultiplexer IC fabricated in silicon bipolar technology," in *Proc. BCTM*, Minneapolis, MN, 1992, pp. 151–154.

[14] T. F Meister, R. Stengl, A. Felder, H.-M. Rein and L. Treitinger, "Selective epitaxial bipolar technology for 25 to 40 Gb/s ICs," in *Proc. ESSDERC 93*, pp. 203–210.

[15] See e.g., Oh Chi, A. Kayanuma, K. Asano, H. Hayaski and M. Noda, *IEEE IEDM Techn. Digest.*, Washington, 1983, p. 55.

Leo C. N. de Vreede was born in Delft, the Netherlands, in 1965. He received the B.S. degree in electrical engineering from the Hague Polytechnic in 1988.

In the summer of 1988, he joined the Microwave Component Group of the Laboratory of Telecommunication and Remote Sensing Technoloyg of the Department of Electrical Engineering, Delft University of Technology. From 1988 to 1990, he worked on the characterization and modeling of CMC capacitors. He is currently carrying out Ph.D. research on the hierarchical design of silicon MMIC's.

Henk C. de Graaff was born in Rotterdam, the Netherlands, in 1933. He received the M.Sc. degree in electrical engineering from Delft University of Technology, Delft, the Netherlands, in 1956, and the Ph.D. degree from the Eindhoven University of Technology, Eindhoven, the Netherlands, in 1975.

He joined Philips Research Laboratories, Eindhoven, in 1964, and has been working on thin-film transistors, MOST, bipolar devices and materials research on polycrystalline silicon. His present field of interest is device modeling for circuit simulation. Since his retirement from Philips Research (November 1991), he has been a consultant to the Delft University of Technology and the University of Twente, the Netherlands.

Fred Hurkx (M'92) was born in Best, the Netherlands, on September 24, 1956. He received the M.Sc. degree in engineering physics from the Eindhoven University of Technology, the Netherlands, in 1985. In 1990, he received the Ph.D. degree from the Eindhoven University of Technology for a thesis concerning the modeling of downscaled bipolar transistors.

In 1979, he joined the Philips Research Laboratories, Eindhoven, where he has been working in the field of semiconductor research since 1983. His present field of interest is the modeling and simulation of silicon devices, especially bipolar transistors.

Joseph L. Tauritz (S'60-M'63) was born in Brooklyn, NY, in 1942. He received the B.E.E. degree from New York University, New York, in 1963 and the M.S.E. degree in electrical engineering from the University of Michigan, in 1968. He was a research fellow at the Delft University of Technology, Delft, the Netherlands, from 1970 to 1971.

He first became acquainted with microwaves while working as a junior engineer on circularly polarized antennas at Wheeler Laboratories in the summer of 1962. From 1963 to 1970, he worked as a technical specialist attached to the R.F. department of the Conduction Corporation, where he designed innovative microwave, VHF, and video circuitry for use in high-resolution radar systems. In 1970, he joined the scientific staff of the Laboratory of the Telecommunication and Remote Sensing Technology, where he is presently an assistant professor. Since 1976, he has headed the Microwave Component Group, where he is principally concerned with the systemetic application of computer-aided design techniques in research and education. His interests include the modeling of high-frequency components for use in the design of MIC's and MMIC's, filter synthesis and planar superconducting microwave components.

Mr. Tauritz is a member of Eta Kappa Nu and the Royal Dutch Institute of Engineers.

Roel G. F. Baets (M'88) received the degree in electrical engineering from the University of Gent, Belgium, in 1980. He received the M.Sc. degree in electrical engineering from Stanford University, Stanford, CA, in 1981, and the Ph.D. degree from the University of Gent in 1984.

Since 1981, he has been with the Department of Information Technology of the University of Gent. In 1989, he was appointed Professor in the engineering faculty of the University of Gent and in 1990, he received a part-time appointment at the Delft University of Technology, the Netherlands, as well. He has worked in the field of *III–V* devices for optoelectronic systems. With over 100 publications and conference papers he has made contributions to the modeling of semiconductor laser diodes, passive guided wave devices and to the design and fabrication of OEIC's. His main interests are now in the modeling, design, and testing of optoelectronic devices, circuits and systems for optical communication and optical interconnects.

Dr. Baets is a member of the Optical Society of America, and the Flemish Engineers Association. He has served as member of the program committee of the ESSDERC conference of the IEEE International Laser Conference and of the ECOC conference.