Special Brief Paper

High-Speed Dynamic Reference Voltage (DRV) CMOS/ECL Interface Circuits

R. X. Gu and M. I. Elmasry

Abstract—**This paper introduces a circuit technique to increase the operating speed of CMOS/ECL interface circuits. The technique is based on shifting the reference voltage dynamically to follow the ECL input signal. HSPICE simulation results based on a 0.8-μm BiCMOS technology show the advantages of DRV CMOS/ECL in terms of speed and noise margins. An analytical delay model which fits HSPICE simulation results is addressed. The error between the model and the circuit simulator is within 4%.**

I. Introduction

HIGH-SPEED ECL circuits play an important role in high performance VLSI systems [1]. The existence of large-swing (CMOS type) and low-swing (ECL type) circuits in a single chip requires that both types communicate to each other via interface circuits. In this brief paper, novel CMOS/ECL interface circuits are proposed. The novel circuits shift the reference voltage of CML dynamically to follow the output of the CMOS stage. Thus, the signal transfer delay from the CMOS based input stage to a bipolar CML based output stage is greatly reduced [2].

The conventional circuit and the new circuits as well as their operation principles are addressed in Section II. In Section III, the dc characteristics and the noise margins are discussed. In Section IV, an analytical delay model for the proposed circuits is described. Results and design considerations are discussed in Section V.

II. Operation Principle of Dynamic ECL Reference Voltage (DRV) CMOS/ECL Interface Circuits

The conventional CMOS/ECL interface circuit is shown in Fig. 1 ([3]). The disadvantage of this circuit is that the delay of the signal transferring from the CMOS inverter stage to the CML stage is long. This is caused by the reference voltage V_r being fixed at the midpoint of supply voltage. The proposed circuit solution ($DRV1$ CMOS/ECL) to accelerate the switching of CMOS/ECL interface circuits is to change the reference voltage V_r dynamically with the input as shown in Fig. 2. Another version of the interface circuit ($DRV2$ CMOS/ECL) is illustrated in Fig. 3. The resistors in Fig. 2 are substituted by MOS transistors. The $DRV2$ CMOS/ECL converter is more suitable for VLSI fabrication at a marginal cost in speed. The circuit principle can be explained by the transient waveforms of Fig. 4, which are from HSPICE results using 0.8-μm BiCMOS technology parameters as shown in Fig. 5.

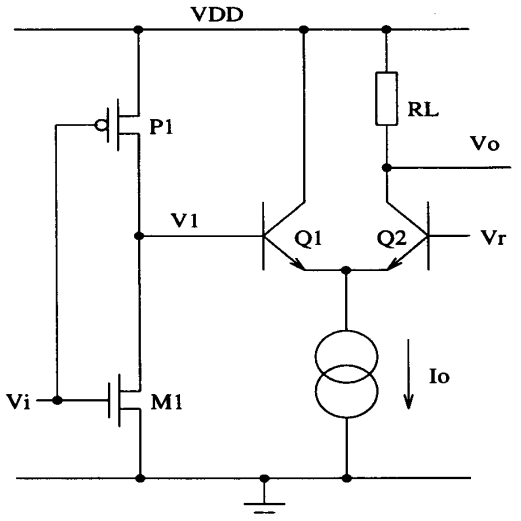

Fig. 1. Circuit schematic of the conventional CMOS/ECL interface.

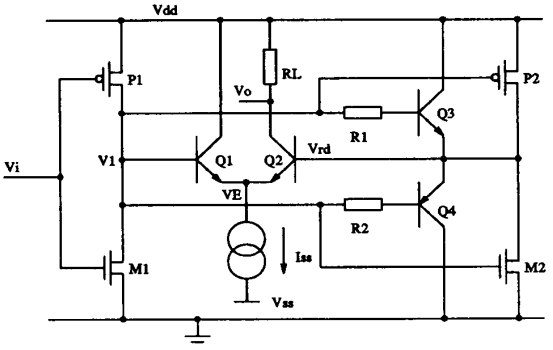

Fig. 2. A circuit schematic of the $DRV1$ CMOS/ECL interface circuit.

The operation principle of $DRV1$ CMOS/ECL and $DRV2$ CMOS/ECL converters is similar and is briefly described as follows: When the input V_i is HIGH (V_{DD}), V_1 is grounded, $Q3$ is off, $P2$ is on and $M2$ is off. The current supplied by the $P2$ branch is injected into the base of $Q2$ and the emitter

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The authors are with the VLSI Research Group, the Department of Electrical and Computer Engineering, University of Waterloo, Waterloo, Ontario, Canada N21 3G1.

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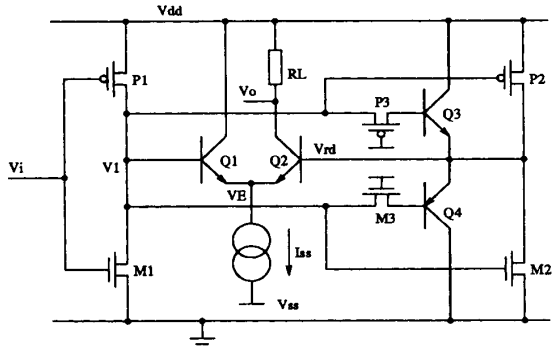

Fig. 3. A circuit schematic of the $DRV2$ CMOS/ECL interface circuit.

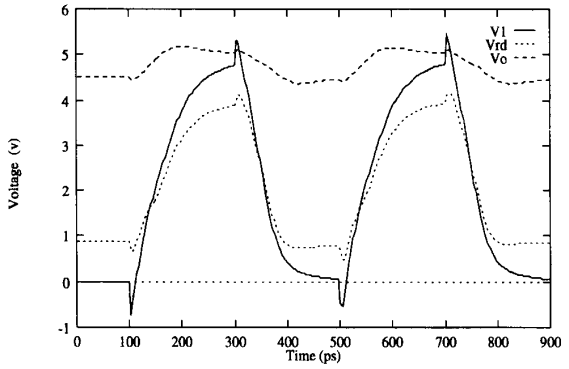

Fig. 4. Node waveforms of the $DRV1$ CMOS/ECL interface circuit.

of $Q4$. This in turn causes $Q4$ to turn on and $V_{rd} = V_{be}$. In this case, $Q1$ is turned off, $Q2$ is turned on and the output $V_o = V_{DD} - I_{ss}R_L$.

When the input V_i falls from HIGH to LOW, V_1 rises and turns Q_4 off. When V_1 rises above $V_{rd} = V_{be}, Q1$ is turned on and $Q2$ is turned off and therefore the output of the circuit immediately rises to HIGH. Since V_{rd} is close to $V_{TN}, M2$ is turned on simultaneously and the current from the $M2$ branch sinks the base charge of $Q2$. When V_1 reaches $2V_{be}, Q3$ is turned on and restricts the V_{rd} to remain lower than V_1 by V_{be} when V_1 continues to rise. The resistor $R1$ of Fig. 2 is adjusted to introduce a proper delay to switch V_{rd} after V_1 rises above V_{be}. The function of PMOS $P3$ of Fig. 3 is to force V_{rd} to switch after V_1 rises above V_{be}. The difference is that no current is supplied to the base of $Q3$ until V_1 reaches V_{be} for the DRV2 CMOS/ECL converter. When V_1 reaches $V_{DD} - V_{TP}$, PMOS $P2$ is turned off. The static biasing current flows from $Q3$ to $M2$. Compared with the conventional CMOS/ECL converter, the DRV-CMOS/ECL converters use $P2$ and $M2$ as a build-in current source instead of a voltage source at the base of $Q2$.

III. DC Characteristics and Noise Margins

The dc input and output voltage transfer characteristics are shown in Fig. 6. Maximum LOW input voltage $V_{il,\max}$ is defined as the low input voltage which causes the output V_o

NPN	Value	PNP	Value
Gain	98	Gain	38
Emitter resistance (Re)	9 Ω	Emitter resistance (Re)	23 Ω
Base Resistance (Rb)	167 Ω	Base Resistance (Rb)	220 Ω
Collector Resiistance (Rc)	57 Ω	Collector Resiistance (Rc)	266 Ω
Base-Emitter Cap. (Ce)	29 fF	Base-Emitter Cap. (Ce)	10fF
Base-Collector Cap. (Cc)	38 fF	Base-Collector Cap. (Cc)	19fF
Base-Substrate Cap. (Cs)	56fF	Base-Substrate Cap. (Cs)	50fF
Ft	10GHz	Ft	4.5GHz
NMOS		**PMOS**	
Vtn	0.78 V	Vtp	-0.88 V
Gate Oxide Thickness	175 Å	Gate Oxide Thickness	175 Å
U0	502 $cm^2 V^{-1} sec^{-1}$	Uo	165 $cm^2 V^{-1} sec^{-1}$
Cgso	273P F/m	Cgso	215P F/m
Cgdo	273P F/m	Cgdo	215P F/m
Cj	250U F/m	Cj	450U F/m
Cjsw	205P F/m	Cjsw	212P F/m

Fig. 5. 0.8-μm BiCMOS technology parameters.

to switch. Under this condition, V_1 drops by one V_{be}, PMOS $P1$ operates in the linear region and NMOS $N1$ is in the saturation region. Assuming $W_P = 2W_n$, the current passing through the CMOS inverter is given by:

$$\begin{aligned} I &= k((V_{dd} - V_T - V_{il,\max})V_{be} - 0.5V_{be}^2) \\ &= 0.5k(V_{il,\max} - V_T)^2. \end{aligned} \tag{1}$$

Assuming $V_T = V_{be}$ and solving the above equation:

$$V_{il,\max} = (2V_{dd}V_T - 4V_T^2)^{0.5}. \tag{2}$$

Due to the symmetry, minimum HIGH input voltage $V_{ih,\min} = V_{dd} - V_{il,\max}$. If $V_{dd} = 5$ V, then, $V_{il,\max} = 2.4$ V and $V_{ih,\min} = 2.6$ V. As shown in Fig. 6, $V_{il,\max}$ and $V_{ih,\min}$ are equal to 2.4 V and 2.5 V respectively, resulting in the transfer characteristics of DRV CMOS/ECL circuits switching abruptly. The noise margins are given by [4]:

$$NM_L = |V_{il,\max} - V_{ol,\max}| \tag{3}$$

$$NM_H = |V_{oh,\min} - V_{ih,\min}| \tag{4}$$

where $V_{ol,\max}$ is the maximum LOW output voltage and $V_{oh,\min}$ is the minimum HIGH output voltage. From the above equations, the noise margin of DRV CMOS/ECL circuits is 2.4 V which is very close to $V_{dd}/2$. The transfer characteristics of the conventional CMOS/ECL circuit (Fig. 1) operated at maximum speed with $C_L = 0.1$ PF is as shown in Fig. 6. Properly choosing the reference voltage can minimize the circuit delay. As the reference voltage shifts up towards V_{dd}, the rise time is increasing and the fall time is decreasing

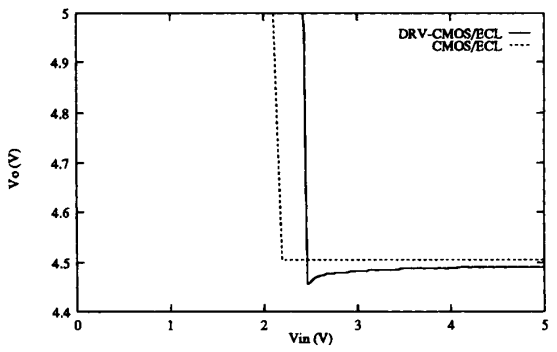

Fig. 6. DC transfer characteristics.

and vice versa. In order to achieve symmetrical fall and rise times, V_{ref} is set to 3 V causing the output transfer voltage to shift down to less than 2.5 V. Thus, the noise margin is reduced. The CMOS/ECL circuit trades noise margins for speed with the adjusting of the reference voltage [5]. Due to one V_{be} advantage at the output of the CMOS inverter V_1, the DRV CMOS/ECL circuits have larger $V_{il,\max}$ and $V_{ih,\min}$ than a CMOS inverter. The noise margin of DRV CMOS/ECL circuits is better than the CMOS/ECL converter and the CMOS inverter.

IV. Transient Analysis

Transient analysis of the conventional NMOS/ECL interface circuit has been reported by Embabi *et al.* [6]. In this section, the fall and rise time analysis of the $DRV2$ CMOS/ECL interface circuit is described. The equivalent circuits using the Ebers-Moll large-signal model for calculating the fall and rise time delays are shown in Fig. 7 and 8. In the case of the DRV CMOS/ECL circuits, V_E swings by 4 V as shown in Fig. 4. This implies that the parasitic capacitance at the common emitter node V_E sinks and sources considerable current during transitions. It is suggested that an MOS current source with smaller parasitic capacitance be used. The total parasitic capacitance C_E at the common emitter node V_E is included in the model analysis as shown in Fig. 7 and 8. The following circuit modeling is based on the $DRV2$ CMOS/ECL circuit. The transistors Q_3 and Q_4 are modeled as two clamped diodes. Their parasitic capacitors are contributed to C_{eq}. Modeling of the $DRV1$ CMOS/ECL circuit is very complicated due to its direct coupling of the bipolar transistors $Q3$ and $Q4$. Since p-n-p $Q4$ acts only as a diode, a lateral p-n-p can be used instead of a vertical p-n-p to achieve similar results. Thus, the proposed circuits still can operate at high speed without increasing the process complexity.

A. The Fall Time Delay t_f

The fall time delay is divided into two parts: (1) t_{f1}, the time required for $Q2$ to turn on and (2) t_{f2}, the time elapsed between the turning on of $Q2$ and the output voltage reaching the $V_{50\%}$.

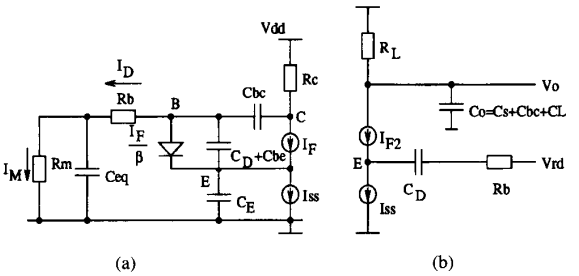

Fig. 7. The equivalent circuit for calculation of (a) t_{f1} and (b) t_{f2}.

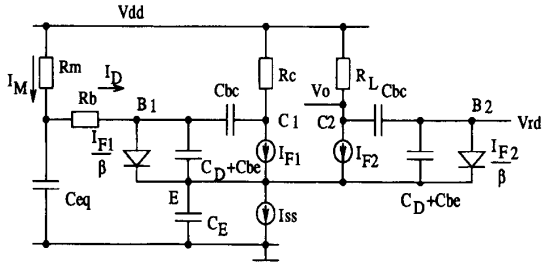

Fig. 8. The equivalent circuit for calculation of t_{r1} and t_{r2}.

1) Calculation of t_{f1}: From the equivalent circuit as shown in Fig. 7(a), the KCL nodal equations at the base and the common emitter are written as:

$$I_D + \tau_F \frac{dI_{F1}}{dt} + I_{F1}/\beta + C_{be}\frac{V_{BE}}{dt} + C_{bc}\frac{d}{dt}(V_B - V_{DD} + I_{c1}R_c) = 0 \tag{5}$$

$$(1 + 1/\beta)I_{F1} + \tau_F \frac{dI_{F1}}{dt} + C_{be}\frac{dV_{BE}}{dt} = I_{ss} + C_E\frac{dV_E}{dt} \tag{6}$$

where $I_D = (C_{bc} + C_{be}/C_{eq})I_M$ is the current extracted from $Q1$ by NMOS $N1$. It is understood that the collect current can be written in terms of V_{BE}:

$$\frac{dV_{BE}}{dt} = \frac{VT}{I_{F1}}\frac{dI_{F1}}{dt} \tag{7}$$

where $V_{BE} = V_B - V_E$. Eliminating V_B and V_E, the differential equation of I_{F1} is given by:

$$C_2 I_2 + C_{bc} I_{F1} + (C_0^2 V_T/I_{F1} + C_1\tau_1)\frac{dI_{F1}}{dt} = 0 \tag{8}$$

where $C_0^2 = C_E C_{bc} + C_E C_{be} + C_{bc}C_{be}, C_1\tau_1 = \tau_F(C_{bc} + C_E) + R_c C_{bc} C_E$ and $C_2 I_2 = C_E I_{F1} - C_{bc} I_{ss}$.

From Fig. 5, we find that $C_1\tau_1$ is much larger than $C_0^2 V_T/I_{F1}$ with I_{F1} around 1 mA. Thus, the $C_0^2 V_T/I_{F1}$ term in (8) is neglected. By using the initial condition $I_{F1}(0) = I_{ss}$, the solution of (8) is:

$$I_{F1} = \frac{C_E}{C_{bc}} I_D \exp\left(-\frac{t}{t_2}\right) + I_{ss} - \frac{C_E}{C_{bc}} I_D \tag{9}$$

where $t_2 = \tau_F(1 + C_E/C_{bc})$. The relation of I_{F1} and V_E is derived by eliminating V_B from (5) to (7):

$$I_D + I_{ss} - I_{F1} + C_{bc}\left(R_c + \frac{V_T}{I_{F1}}\right)\frac{dI_{F1}}{dt} + (C_E + C_{bc})\frac{dV_E}{dt} = 0. \quad (10)$$

Introducing (9) into (10), we obtain

$$\left(1 + \frac{C_E}{C_{bc}}\right)I_D - I_D\left(\frac{C_E}{C_{bc}} + \frac{R_cC_{bc}}{t_2}\right)\exp\left(-\frac{t}{t_2}\right) - \frac{C_{bc}V_T}{t_2}\left(1 + \frac{C_EI_D}{C_{bc}I_{F1}} - \frac{I_{ss}}{I_{F1}}\right) + (C_E + C_{bc})\frac{dV_E}{dt} = 0. \quad (11)$$

In real applications, I_D has a range from 1 mA to 4 mA and $C_{bc}V_T/t_2 = 0.05$ mA according to the technology parameters. Thus, the terms including $C_{bc}V_T/t_2$ are negligible. Separating the variables and integrating (11) and noting that the time period t_{f1} required for Q_2 to turn on is the time to enable the common emitter V_E to drop by $V_{be,on}$. Thus, t_{f1} is given by:

$$t_{f1} = \frac{(C_Et_2 + R_cC_{bc}^2)}{C_E + C_{bc}} + \frac{V_{be,on}C_{bc}}{I_D}. \quad (12)$$

2) Calculation of t_{f2}: During t_{f2}, $Q1$ is off. The equivalent circuit can be simplified to include $Q2$ only as shown in Fig. 7(b). When $Q2$ begins to turn on, p-n-p $Q4$ is still off due to the delay of the switch of NMOS $M3$. V_{rd} remains quasi-constant, causing V_E to remain quasi-constant. Hence, C_E is not included in the emitter of the model. From Fig. 7(b), I_{F2} is given by:

$$I_{F2} = I_{ss}\left(1 - \exp\left(-\frac{t}{\tau_F}\right)\right). \quad (13)$$

The output nodal equation is written as:

$$I_{F2} = \frac{V_{dd} - V_o}{R_L} - C_o\frac{dV_o}{dt}. \quad (14)$$

Combining (13) and (14) and solving the differential equation, yields the following result:

$$V_o(t) = V_{dd} - I_{ss}R_L + \frac{I_{ss}R_L}{\tau_F - \tau_L}\cdot\left(\tau_F\exp\left(-\frac{t}{\tau_F}\right) - \tau_L\exp\left(-\frac{t}{\tau_L}\right)\right) \quad (15)$$

where $\tau_L = R_LC_o$. For small load C_L, τ_F is close to τ_L. The exponential terms can be expressed as a second order Taylor series. Solving the above equation with the condition $V_o(t_{f2}) = V_{dd} - I_{ss}R_L/2$, yields the following expression:

$$t_{f2} = (\tau_F\tau_L)^{0.5}. \quad (16)$$

The fall time delay is given by:

$$t_f = t_{f1} + t_{f2} = \frac{C_Et_2 + R_cC_{bc}^2}{C_E + C_{bc}} + \frac{V_{be,on}C_{bc}}{I_D} + (\tau_F\tau_L)^{0.5}. \quad (17)$$

B. The Rise Time Delay t_r

The rise time delay is divided into two parts: (1) t_{r1}, the time required for $Q1$ to turn on and (2) t_{r2}, the time elapsed between the turning on of $Q1$ and the output voltage reaching the $V_{50\%}$.

1) Calculation of t_{r1}: The initial delay for turning on $Q1$ is derived as ([7]):

$$t_{r1} = (R_{CH} + R_b)C_{eq}\frac{V_{be,on}}{V_{dd} - V_T} \quad (18)$$

where $R_{CH} = 2/g_{m,sat}$ is the equivalent channel resistance of PMOS $P1$ operating in the saturation region.

2) Calculation of t_{r2}: From the equivalent circuit shown in Fig. 8, the KCL nodal equation at the base of $Q1$ and the common emitter are given by:

$$\tau_F\frac{dI_{F1}}{dt} + I_{F1}/\beta + C_{be}\left(\frac{dV_{B1}}{dt} - \frac{dV_E}{dt}\right) + C_{bc}\frac{d}{dt}(V_B - V_{DD} + I_{c1}R_c) = I_D \quad (19)$$

$$I_{F1} + I_{F2} + \tau_F\frac{dI_{F1}}{dt} + \tau_F\frac{dI_{F2}}{dt} + C_{be}\left(\frac{dV_{B1}}{dt} - \frac{dV_E}{dt}\right) + C_{be}\left(-\frac{dV_E}{dt}\right) + I_{F1}/\beta + I_{F2}/\beta = C_E\frac{dV_E}{dt} + I_{ss} \quad (20)$$

and the relation of bipolar transistors:

$$\frac{dV_{B1}}{dt} - \frac{dV_E}{dt} = \frac{V_T}{I_{F1}}\frac{dI_{F1}}{dt} \quad (21)$$

$$-\frac{dV_E}{dt} = \frac{V_T}{I_{F2}}\frac{dI_{F2}}{dt}. \quad (22)$$

In (22), $dV_{Vrd}/dt = 0$. The R_cC_{bc} term is negligible since it is much smaller than τ_F. The above two equations do not have an analytical solution. An approximation is introduced: Assuming that C_D of $Q1$ is much smaller than C_{eq}, i.e., the current sunk by C_D is negligible, hence, the current I_M from PMOS $P1$ charges C_{eq} only, i.e., $dV_{B1}/dt = I_M/C_{eq}$. The HSPICE simulation result shows that the input of ECL V_1 has a good linear relation with respect to time. Combining the equations, yields the following relation:

$$\left(\tau_F + \frac{C_{be}V_T}{I_{F1}}\right)\frac{dI_{F1}}{dt} = I_M^* \quad (23)$$

where $I_M^* = (C_{be}/C_{eq})I_M$. The above equation shows that I_{F1} rises exponentially to $C_{be}V_T/\tau_F = 0.07$ mA in a very short time interval. With the increase of the I_{F1}, τ_F becomes the dominate term. Assuming $C_{be}V_T/I_{F1}$ is constant and small, we introduce the average value. Solving the above differential equation, yields the following expression:

$$I_{F1} = I_M^*\frac{\tau_{F1}}{t} \quad (24)$$

where $\tau_{F1} = \tau_F + \overline{C_{be}V_T/I_{F1}}$ and $\overline{C_{be}V_T/I_{F1}}$ is the average contribution from I_{F1}. The above equation is correct with $t < I_{ss}\tau_F/I_M^*$. Thus, I_{F2} is given by:

$$I_{F2} + \tau_{F2}\frac{dI_{F2}}{dt} = I_{ss} - I_M^* - \frac{I_M^*}{\tau_{F2}}t \quad (25)$$

where $\tau_{F2} = \tau_F + \overline{(C_E + C_{be})V_T/I_{F2}}$. In order to simplify mathematical manipulations, it is reasonable to assume that $\tau_{F1} = \tau_{F2} = \tau_F + a((C_E + C_{be})V_T/I_{ss})$ because of $\overline{1/I_{F1}} > \overline{1/I_{F2}}$ during t_{r2}. We choose $a = 2$ for our simulations. Solving (25) with the initial condition $I_{F2}(0) = I_{ss}$, I_{F2} is given by:

$$I_{F2} = -\frac{I_M^*}{\tau_{F1}}t + I_{ss}. \tag{26}$$

From Fig. 8, solving the nodal equation at the output which is the same as (14), V_o is given by:

$$V_o(t) = V_{dd} - I_m^* R_L + \frac{I_M^* R_L \tau_L}{\tau_{F1}} \exp\left(-\frac{t}{\tau_L}\right) + \frac{R_L I_M^*}{\tau_{F1}}(t - \tau_L). \tag{27}$$

For small load C_L, (27) is treated the same as (15). Expressing the exponential term as a second order Taylor series, yields the following result:

$$t_{r2} = \left(\frac{I_{ss}}{I_M^*}\tau_{F1}\tau_L\right)^{0.5}. \tag{28}$$

The rise time delay is therefore given by:

$$t_r = t_{r1} + t_{r2} = (R_{CH} + R_b)C_{eq}\frac{V_{be,on}}{V_{dd} - V_T} + \left(\frac{I_{ss}}{I_M^*}\tau_{F1}\tau_L\right)^{0.5}. \tag{29}$$

V. Results and Design Considerations

In order to verify the correctness of the model, comparisons between the model and the HSPICE simulator are carried out. Assuming that every parasitic capacitance is constant during a transition, the average value for each parasitic capacitance is calculated using the parameters listed in Fig. 5. The comparison between the fall time delay model and the HSPICE simulation result is shown in Fig. 9. It is interesting to note that the fall time delay is inversely proportional to the square root of the current source of ECL and is insensitive if I_{ss} is larger than 0.8 mA. The error between the delay model and the HSPICE result is within 3%. The comparison between the rise time delay and the HSPICE simulation result is shown in Fig. 10. The rise time delay weakly depends on I_{ss}. The error between the delay model and the HSPICE result is shown within 4%.

Both the fall and rise time delay models show that the operating speed is inversely proportional to the size of the CMOS inverter. The delay becomes insensitive to the size of CMOS inverter beyond a certain point due to the constant terms. Usually, the fall time delay is longer than the rise time delay according to the technology parameters. The fall time delay limits the operating speed. If the load capacitance is large, τ_L dominates over the other time constants, both the fall time and rise time are proportional to τ_L and inversely proportional to I_{ss}.

The time delay versus supply voltage is shown in Fig. 11 and reveals that both DRV CMOS/ECL circuits are still faster than the conventional CMOS/ECL circuit with V_{DD} scaled down to 3 V. Fig. 11 also indicates that the $DRV1$ CMOS/ECL circuit is faster than the $DRV2$ CMOS/ECL circuit. This is mainly due to direct coupling of $Q3$ and $Q4$ and smaller C_{eq} causing V_1 to switch faster.

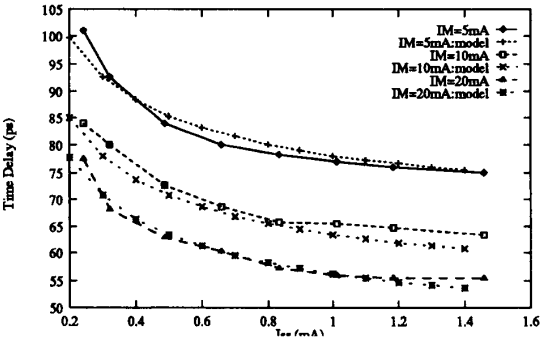

Fig. 9. A comparison for the fall time delay versus I_{ss} with $C_o = 0.1$ pF.

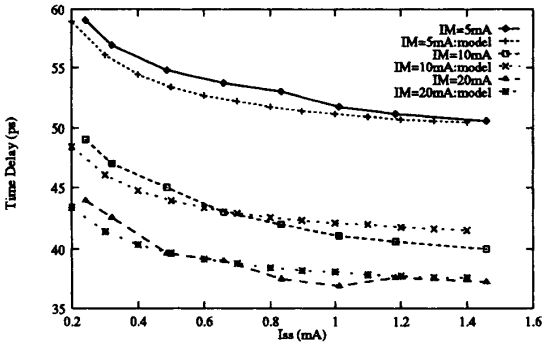

Fig. 10. A comparison for the rise time delay versus I_{ss} with $C_o = 0.1$ pF.

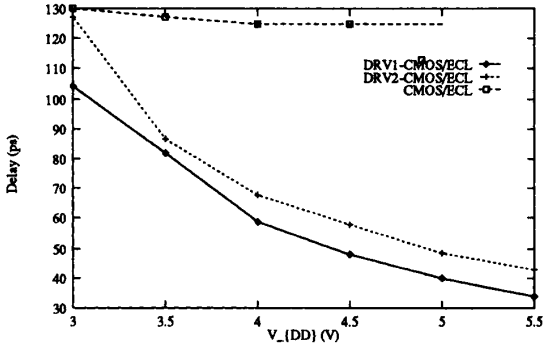

Fig. 11. Time delay versus supply voltage.

VI. Conclusions

Novel high speed CMOS/ECL interface circuits using a dynamic reference voltage technique are reported. Circuit simulation results show superior performance of speed and noise margin over conventional designs. An analytical delay model for small output loads fits HSPICE simulation results.

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