# Optimum Degeneration for Minimum Mismatch in Bipolar Current Sources

Morteza Vadipour

*Abstract*— **Statistical analysis of mismatch in bipolar degenerated current sources reveals the existence of an optimum degeneration for minimum mismatch. Extra degeneration does not improve matching but degrades it and forces unnecessary dc restrictions on the circuit.**

## I. Introduction

BIPOLAR degenerated current sources are used widely in linear and nonlinear circuits such as analog blocks, D/A and A/D converters, timers, multipliers, and so on. It is well-known that degeneration improves current matching between two similar current sources. However, the effectiveness of the technique is somewhat obscured and the common thought is that more degeneration results in more matching. In this work degeneration is considered from the statistical point of view and some useful results are derived which are helpful in the design of matched current sources.

Throughout the text the simple current mirror of Fig. 1 will be considered. For other current mirrors such as Wilson and cascode, the situation is the same. The reason is that the amount of matching in these current sources directly depends on the matching of the mirror transistors and for good matching they are usually degenerated.

A simple method of mismatch and offset calculation will be presented in Section IV. This method considerably simplifies such calculations, specially for complex circuits.

## II. Mismatch in Degenerated Current Sources

In Fig. 1, a pair of simple degenerated n-p-n current sources is shown. In many applications the "equality" or matching of output currents is of great importance. The mismatch in the output currents results from $Is, \beta$ and $R$ mismatches in the two branches.

To evaluate the effect of the latter mismatches on the former, we use the method described in Section IV.

Using the circuit of Fig. 2 for calculation of $\Delta I_c$ and noting that

$$G_m = \frac{g_m}{1 + \frac{g_m R}{\alpha}}$$

$$r_e = \frac{\alpha}{g_m}$$

$$I_B \frac{\Delta\beta}{\beta} = \frac{I_c}{\alpha}\frac{\Delta\alpha}{\alpha},$$

Manuscript received November 19, 1993; revised May 9, 1994.
The author is with ZAG Chemie Company, Tehran 14346, Iran.
IEEE Log Number 9404521.

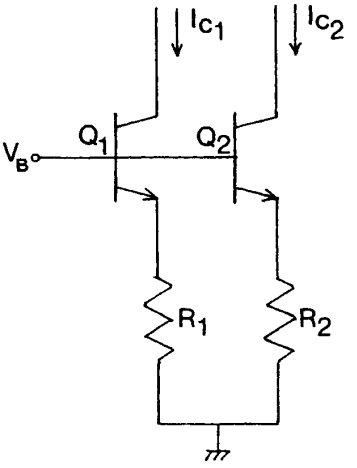


Fig. 1. A pair of simple n-p-n degenerated current sources.

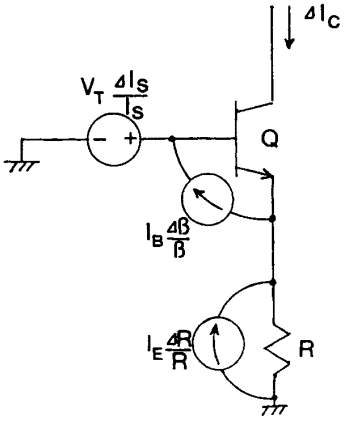


Fig. 2. A model for mismatch calculation.

it is readily found that

$$\frac{\Delta I_c}{I_c} = \left(\frac{1}{1 + \frac{g_m R}{\alpha}}\right)\frac{\Delta I_s}{I_s} + \left(\frac{\frac{g_m R}{\alpha}}{1 + \frac{g_m R}{\alpha}}\right) \cdot \left(\frac{\Delta\alpha}{\alpha} - \frac{\Delta R}{R}\right). \quad (1)$$

This is the same as given in [1] obtained classically.

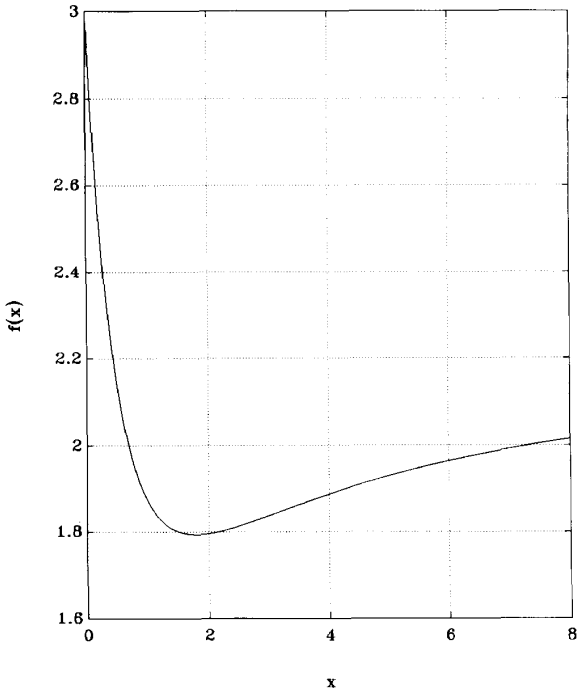


Fig. 3. Graph of function (3) for $K = 3, L = 2$.

Electrical device parameters are, in general, statistical random variables [2]. Mismatch components $(\Delta I_s/I_s, \Delta\alpha/\alpha, \Delta R/R)$ in the right side of (1) are also statistical random variables. In the design of matched current sources, care is taken to reduce these mismatches by defining large and equal size features for the elements. Common centroid geometries are also used for this purpose [1]. These strategies result in zero mean and low standard deviation for parameter mismatches [1], the variance of $(\Delta I_c/I_c)$ with the assumption of independence between right side mismatches [1] can be written [3].

$$\sigma^2_{\Delta I_c/I_c} = \left(\frac{1}{1+\frac{g_m R}{\alpha}}\right)^2 \sigma^2_{\Delta I_s/I_s} + \left(\frac{\frac{g_m R}{\alpha}}{1+\frac{g_m R}{\alpha}}\right)^2 \cdot (\sigma^2_{\Delta\alpha/\alpha} + \sigma^2_{\Delta R/R}). \quad (2)$$

It is seen that for a known set of $\sigma_{\Delta I_s/I_s}, \sigma_{\Delta\alpha/\alpha}$ and $\sigma_{\Delta R/R}$ (which are usually given for various processes and geometrical sizes) $\sigma_{\Delta I_c}$ is a function of degeneration $g_m R$.

## III. Optimum Degeneration for Minimum Mismatch

Relation (2) is of the form

$$f(x) = \frac{K}{(1+x)^2} + \left(\frac{x}{1+x}\right)^2 L$$
$$x = \frac{g_m R}{\alpha}, \quad K = \sigma^2_{\Delta I_s/I_s}, \quad L = \sigma^2_{\Delta\alpha/\alpha} + \sigma^2_{\Delta R/R}. \quad (3)$$

To illustrate the properties of this function, it is depicted in Fig. 3 for (arbitrary) $K = 3, L = 2$.

It is evident that $f(0) = K, f(\infty) = L$ and in amidst there is a minimum.

It can be shown that the minimum occurs for $x_{\min} = K/L$ and $f(x_{\min}) = K \parallel L (K \parallel L = KL/K + L)$.

In the original relation (2), as degeneration $g_m R$ is increased from zero to large values, $\sigma^2_{\Delta I_c/I_c}$, at first, decreases from $\sigma^2_{\Delta I_s/I_s}$ to its minimum value $(\sigma^2_{\Delta I_s/I_s}) \parallel (\sigma^2_{\Delta\alpha/\alpha} + \sigma^2_{\Delta R/R})$ at $g_m R = \frac{\sigma^2_{\Delta I_s/I_s}}{\sigma^2_{\Delta\alpha/\alpha}+\sigma^2_{\Delta R/R}}$, then it increases to the value $(\sigma^2_{\Delta\alpha/\alpha} + \sigma^2_{\Delta R/R})$ for large $g_m R$.

This analysis shows that there is an optimum degeneration that minimizes mismatch. Further degeneration increases mismatch and causes unnecessary dc restriction for the current source.

Fig. 4 shows the effect of degeneration for typical n-p-n and p-n-p integrated circuit current sources. The devices are junction isolated, 44 V, 17 $\mu$ epi and 100 $\Omega/\square$ base diffusion [1]. Emitter size for n-p-n transistors is $20\,\mu \times 25\,\mu$ and $30\,\mu \times 30\,\mu$ for p-n-p's. Degeneration resistors $R_1$ and $R_2$ are base diffusion with 8 $\mu$ width. Parameter mismatches are as follows [1].

For n-p-n transistors: $\sigma_{\Delta I_s/I_s} = 5\%, \sigma_{\Delta\alpha/\alpha} = .1\%, \& \sigma_{\Delta R/R} = 1\%$.

For p-n-p transistors: $\sigma_{\Delta I_s/I_s} = 5\%, \sigma_{\Delta\alpha/\alpha} = 1\% \& \sigma_{\Delta R/R} = 1\%$.

In Fig. 4(a) and (b) degeneration is expressed in terms of voltage drop on $R\,(g_m R/\alpha = I_E R/V_T)$.

For these typical current sources, the standard deviation of mismatch, after reaching the minimum, increases very slightly. This is because of the large difference between $\sigma^2_{\Delta I_s/I_s}$ and $(\sigma^2_{\Delta\alpha/\alpha} + \sigma^2_{\Delta R/R})$. However, no better matching is available than for $(g_m R)_{opt}$ and further degeneration imposes a dc restriction for the current source. The amount of optimum degeneration for minimum mismatch is also reasonable and practical (.64 V for n-p-n and .325 V for p-n-p).

As an example, in the commercial 741 (assuming parameter mismatches:

$$\sigma_{\Delta I_s/I_s} = 5\% \sigma_{\Delta R/R} = 1\%, \sigma_{\Delta\beta/\beta} = 10\%$$

for n-p-n and p-n-p transistors.

The amount of degeneration in the first stage current mirror is less than optimum and good improvement can be achieved by some more degeneration. Choosing 6 K resistors instead of 1 K (which are simply and economically realizable) input offset voltage reduces from 2.6 mV to 1.9 mV.

## IV. A Simple Method for Offset and Mismatch Calculation

Classical methods of offset and mismatch calculation [1], [4] are rather tedious and are only practical for simple circuits. In this part a concise method will be described that greatly simplifies such calculations. This method is based on proper circuit models which transform offset and mismatch calculation to simple ac analysis of the circuits. The basis of these models is that the effect of small variations in the device

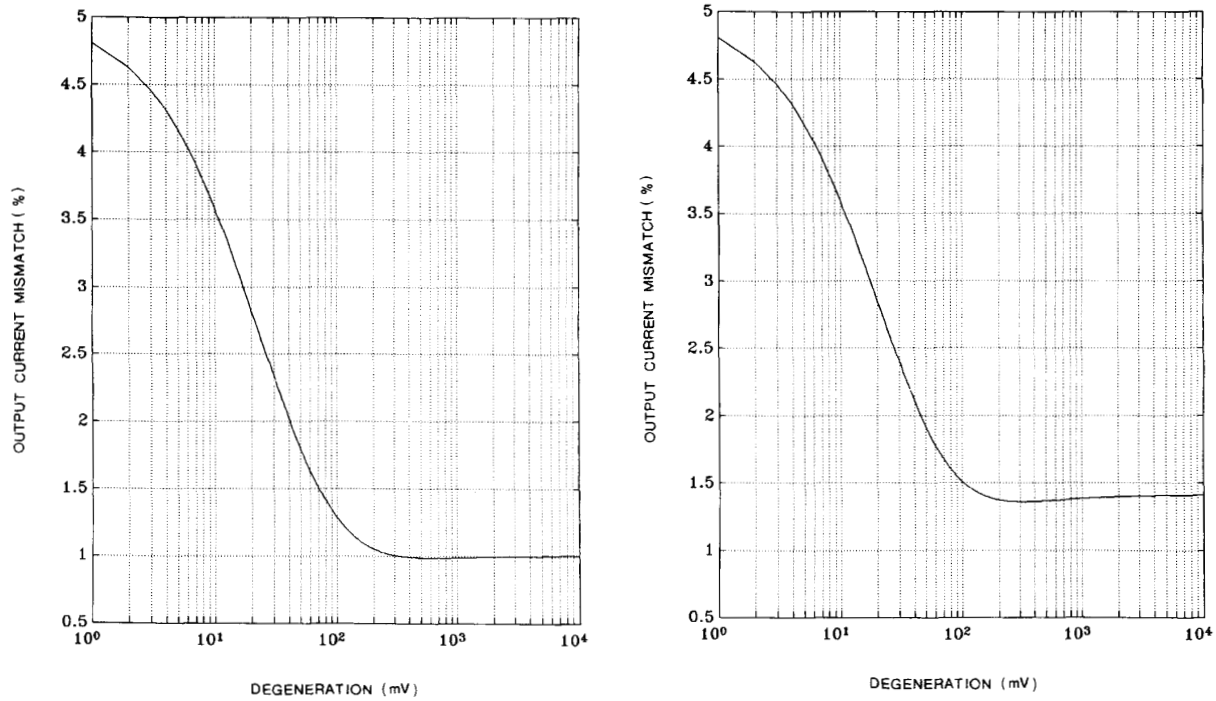


Fig. 4. (a) Effect of degeneration on mismatch for a pair of typical n-p-n integrated circuit current sources ($\sigma_{\Delta I_s/I_s} = 5\%$, $\sigma_{\Delta\alpha/\alpha} = .1\%, \sigma_{\Delta R/R} = 1\%$ [1]). (b) Effect of degeneration on mismatch for a pair of typical p-n-p integrated circuit current sources ($\sigma_{\Delta I_s/I_s} = 5\%, \sigma_{\Delta\alpha/\alpha} = 1\%, \sigma_{\Delta R/R} = 1\%$[1]).

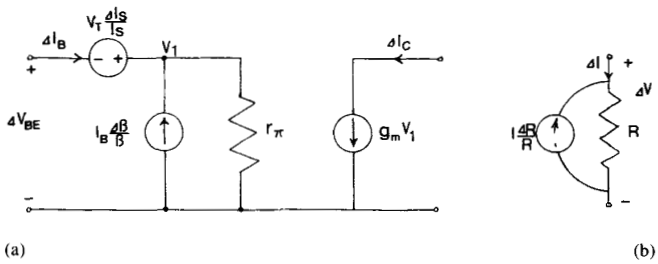


Fig. 5. Mismatch model for (a) transistor (b) resistor.

parameters (such as $Is, \beta, R$) are incorporated in the original ac models.

### A. Bipolar Transistors

Two basic equations define a bipolar transistor in the active mode operation

$$V_{BE} = V_T ln \frac{I_c}{I_s} \tag{4}$$

$$I_B = \frac{I_c}{\beta}. \tag{5}$$

Consider two similar transistors in similar conditions, having small differences in $Is$ and $\beta$ that are:

$$\beta' = \beta + \Delta\beta \tag{6}$$

$$I_s' = I_s + \Delta I_s. \tag{7}$$

These differences result in variations in $V_{BE}, I_c$, and $I_B$ of the two transistors. From (4) we have:

$$V_{BE} = V_T ln \frac{I_c}{I_s}$$

$$V_{BE}' = V_T ln \frac{I_c + \Delta I_c}{I_s + \Delta I_s}.$$

It is easily found that for small variations

$$\Delta V_{BE} = V_T \left( \frac{\Delta I_c}{I_c} - \frac{\Delta I_s}{I_s} \right). \tag{8}$$

A similar argument for (5) results in

$$\Delta I_B = \frac{\Delta I_c}{\beta} - I_B \left( \frac{\Delta\beta}{\beta} \right). \tag{9}$$

Merging (8) and (9) we obtain

$$\Delta V_{BE} + V_T \frac{\Delta I_s}{I_s} = \frac{1}{g_m} \Delta I_c \tag{10}$$

$$\Delta I_B = \frac{1}{r_n}\left(\Delta V_{BE} + V_T \frac{\Delta I_s}{I_s}\right) - I_B\left(\frac{\Delta \beta}{\beta}\right). \tag{11}$$

It is easy to verify that model in Fig. 5(a) satisfies (10) and (11).

### B. Resistors

From Ohm's law $I = V/R$, we have

$$\Delta I = \frac{\Delta V}{R} - I\frac{\Delta R}{R}. \tag{12}$$

The model in Fig. 5(b) clearly satisfies (12).

## V. Conclusion

The concept of optimum degeneration of this paper seems useful in the design of matched current sources and prevents unintended over- or under-degeneration which degrade the circuit performance. The technique of mismatch and offset calculation of this paper allows a simple and general method for the purpose and gives a more comprehensive view of the mismatch performance of the circuit.

## References

[1] P. R. Gray and R. G. Meyer, *Analysis and Design of Analog Integrated Circuits*. New York: Wiley, 1984.

[2] R. W. Dutton *et al.*, "Correlation of fabrication process and electrical device parameter variations," *IEEE J. Solid-State Circuits*, vol. 12, no. 4, Aug. 1977.

[3] W. B. Davenport, Jr., *Probability and Random Processes*. New York: McGraw-Hill, 1970.

[4] A. B. Grebene, *Bipolar and MOS Analog Integrated Circuit Design*. New York: Wiley, 1984.