High-Speed, Low-Switching Noise CMOS Memory Data Output Buffer

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***Abstract*—This paper describes a data output buffer for high-speed CMOS integrated memories with a high data output pin count. The buffer minimizes the switching noise induced on supply lines while achieving very fast output transitions by combining output presetting techniques together with adequate driving of the output pull-up and pull-down transistors. Tristate operation and zero static power consumption are also provided. The buffer was integrated in a 16-Mb EPROM device. It occupies 0.06 mm^2 and ensures a better than 15 ns output transition time with a load capacitor of 100 pF.**

I. Introduction

A DATA output buffer for high-speed memories must provide very fast output transitions. To this end, the output current i_O should be capable of charging and discharging the output capacitive load C_L to a predetermined voltage level within a specified time interval. In the presence of large capacitive loads, nonnegligible voltage bumps are induced on the device power supply lines (ground and V_{DD}). These are due mainly to the parasitic inductance L of the power buses (particularly of bonding wires and package pin leads), which gives rise to Ldi/dt noise (inductive or switching noise or ground/V_{DD} bounce) [1]–[7] (Fig. 1). This noise creates spurious signals, and can lead to false switching if its magnitude exceeds the noise tolerance of the device logic circuitry. The problem is particularly severe in memory chips with a wide-word organization, as simultaneous switching of several outputs [8]–[10] can occur. In the case of simultaneous switching, an efficient solution is advanced packaging and assembly technology, nevertheless suitable design techniques also help to alleviate the problem. The key target of these techniques is to keep the peak value of di_O/dt as low as possible to limit inductive noise to a minimum, while still meeting the switching speed specifications required of the device.

A popular approach uses, for a single output buffer, pull-up and pull-down structures made of a number of transistors placed in parallel [11], [12]. When performing an output transition, suitable delays are introduced while driving the different elements: the peak contributions of the switching noise do not occur at the same instant, and therefore the overall peak noise is reduced. A similar principle can be adopted for the switching of several outputs. Suitable delays in switching on different output buffers ("staggered" output drive approach) reduce the inductive noise as well. The effectiveness of the above solutions depends on careful design and layout. Moreover, their performance relies heavily on the wafer fabrication process. For these reasons, noise control becomes rather difficult and needs very accurate implementation. Therefore, more reliable design techniques are necessary.

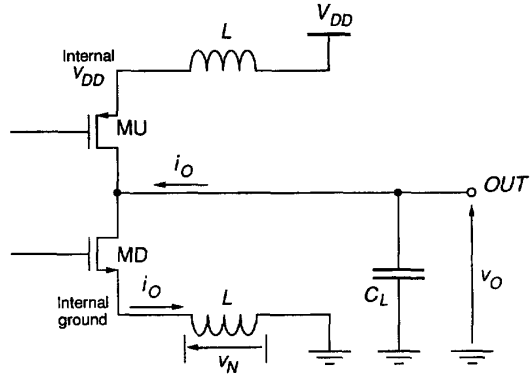

Fig. 1. Generation of inductive noise $v_N = Ldi_O/dt$ on the ground line. The output pull-down transistor MD is assumed to be activated.

Better results are achieved by employing a suitable control of the gate of the output pull-up and pull-down transistors. The waveforms used should produce the required control of the output current, limiting its time derivative. Several methods [3], [4], [13]–[19] have been proposed to generate the desired driving waveforms, and good results have been reported. However, for large output voltage swings, these techniques lead to unacceptable output transition time.

Alternatively, the output node can be preset to a determined level $V_{O,pr}$, intermediate between V_{DD} and ground, when the request for a read operation is detected [20]–[25]. The preset operation is carried out during the period in which memory cells are addressed and their content is sensed ("sensing period"). Therefore, it does not contribute to the access time. The preset operation reduces the output voltage swing in the following phase ("output transition period"). Hence a lower value of di_O/dt for a given output transition time will result. However, we have the problem of controlling the current when the output node approaches the specified middle output level.

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This paper describes a new circuit solution for a data output buffer. It uses a suitable combination of the output presetting technique together with adequate driving of the output pull-up and pull-down transistors. Zero power consumption is provided during stand-by and static conditions.

In Section II, considerations on switching noise minimization are discussed and design guidelines are given. The circuit diagram and the operation of the proposed buffer are described in detail in Section III. Finally, silicon implementation is presented in Section IV together with measurements results.

II. Minimizing Switching Noise

Before entering into the details of the method used, we shall first analyze the origin of switching noise. For this, let us consider an output voltage swing ΔV_O carried out in a time interval $\bar{t}$. If the output capacitive load is C_L and the output current is i_O we have

$$\int_0^{\bar{t}} i_O d\tau = C_L |\Delta V_O|. \tag{1}$$

The best waveform that minimizes the peak value of di_O/dt is a triangular shape with equal rising and falling edges [3]:

$$\left|\frac{di_O}{dt}\right| = K. \tag{2}$$

From (1) and (2), the output voltage swing in each half of the triangular current waveform (time length $\bar{t}/2$) is $\frac{1}{2}\frac{K}{C_L}(\frac{\bar{t}}{2})^2$; therefore, the total output voltage swing ΔV_O is given by:

$$|\Delta V_O| = \frac{1}{4}\frac{K}{C_L}\bar{t}^2. \tag{3}$$

The value of K must allow the required output voltage swing within the available time interval t_o:

$$K \geq \frac{4|\Delta V_O| C_L}{(t_o)^2}. \tag{4}$$

The switching noise due to the supply line inductance L results:

$$|v_N| = L\left|\frac{di_O}{dt}\right| = KL. \tag{5}$$

From (4) and (5) we have that for a given output swing the noise is kept unchanged by increasing the switching time as the square root of the capacitive load.

We have already mentioned in the introduction that the best trade-off between switching time and noise is the use of the presetting technique. In this case the best output current waveform will be the one shown in Fig. 2(a). During the preset phase the output voltage, assumed equal to V_{DD}, is reduced to $V_{O,pr}$ (Fig. 2(b)). The output current has an isosceles-triangular shape and the switching noise is kept to a defined level (Fig. 2(c)). During the output transition phase, the read datum, assumed to be low, leads the output voltage to zero. Again, the shape of the output current is triangular. The slope is the same as in the previous phase, and therefore the noise does not exceed the predefined limit. In the ideal case, the

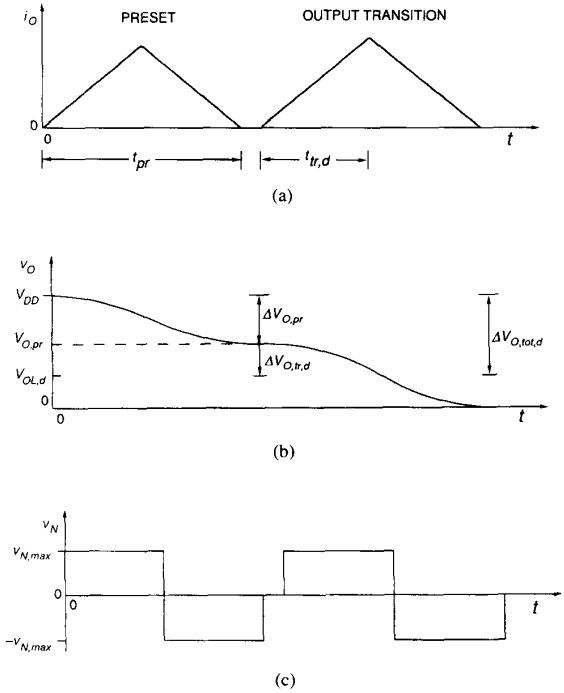

Fig. 2. Ideal waveform of the output current i_O (a) used to minimize switching noise v_N when adopting the presetting technique (c). The resulting output voltage waveform v_O is also shown in (b) (output transition $1 \rightarrow 0$). The static output current is assumed equal to zero.

specified dynamic output logic level ($V_{OL,d}$) is reached before the output current slope reverses.

A critical point concerns the choice of the preset voltage $V_{O,pr}$. Its optimal value depends on the largest required total dynamic output voltage swing $\Delta V_{O,tot,d}$ (output preset plus transition periods) as well as on the available times for the preset and the output transition phases (t_{pr} and $t_{tr,d}$, respectively). $\Delta V_{O,tot,d}$ in turn, is a function of the specified static and dynamic output logic levels, which are generally different.

From the above equations, the output voltage swing in the preset phase, $\Delta V_{O,pr}$, should be set equal to:

$$|\Delta V_{O,pr}| = \frac{|\Delta V_{O,tot,d}|}{\left[1 + 2(t_{tr,d}/t_{pr})^2\right]}. \tag{6}$$

We generally have the largest value of $\Delta V_{O,tot,d}$ for an output transition $1 \rightarrow 0$, when the output node is driven from a starting value $V_{O,i} = V_{DD}$ to the dynamic low output level $V_{OL,d}$. Setting $\Delta V_{O,tot,d} = V_{DD} - V_{OL,d}$ and $\Delta V_{O,pr} = V_{DD} - V_{O,pr}$ in (6), we obtain:

$$V_{O,pr} = \frac{2(t_{tr,d}/t_{pr})^2}{2(t_{tr,d}/t_{pr})^2 + 1} V_{DD} + \\ + \frac{1}{2(t_{tr,d}/t_{pr})^2 + 1} V_{OL,d}. \tag{7}$$

In practical cases, the value $V_{OL,d}$ is generally reached after the inversion in the output current slope, and hence some corrections should be made with respect to (7).

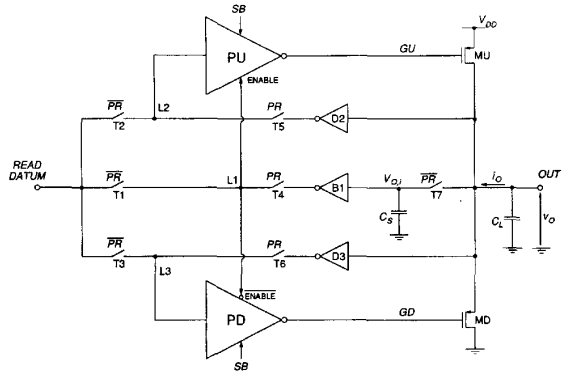

Fig. 3. Block diagram of the proposed output buffer.

By contrast, the largest $\Delta V_{O,tot,d}$ for the complementary transition $0 \rightarrow 1$ equals the dynamic high output level $V_{OH,d}$. Since it is small, the preset level is not a critical parameter.

III. Description of the Output Buffer

The block diagram of the proposed buffer is shown in Fig. 3. The inverting blocks PU and PD control the pull-up (MU) and the pull-down (MD) transistor, respectively. The voltage discriminators $D2$ and $D3$ decide when the slope of the output current must be reversed in the preset phase [26].

We can distinguish three operating phases, which are controlled by signals SB (stand-by) and PR (preset). We have:

—stand-by SB = 1 PR = 0
—preset SB = 0 PR = 1
—data output SB = 0 PR = 0.

During stand-by, the driving blocks PU and PD are disabled: both output transistors MU and MD are forced to the off state.

Out of stand-by conditions, the operation of PU and PD is controlled by the line $L1$: depending on its logic level (high or low), only one of the two blocks (PU or PD, respectively) is enabled. The enabled block allows the corresponding output transistor to be controlled by its respective driving line ($L2$ or $L3$). The signal PR decides if the system is in the preset phase or not.

During the preset period, transfer gates $T1$, $T2$, and $T3$ are kept off, thus disabling the control by the read datum. $T4, T5$, and $T6$ are switched on, while $T7$ is off: the output voltage at the beginning of the preset period, $V_{O,i}$, is stored on capacitor C_S, and drives line $L1$ through the inverting buffer $B1$. The two discriminators $D2$ and $D3$ sense the instantaneous output voltage $v_O(t)$, and control the lines $L2$ and $L3$. The enabled driving block (PU or PD) activates the corresponding output transistor, thereby charging or discharging the capacitive load C_L. The driving used ensures a constant slope in the output current. The relative discriminator defines when the output current slope must reverse. After the slope inversion, the output current is driven back to zero smoothly. The output voltage is brought to a suitable level $V_{O,pr}$ between V_{DD} and ground.

At the end of the preset phase, the read datum is made available, and takes the conrol of lines $L1, L2$, and $L3$. Again, one of the two blocks PD and PU is enabled, and drives the corresponding output transistor with a suitable control of the output current. During this phase it is no longer necessary to use the voltage discriminators $D2$ and $D3$: when the drain-to-source voltage of the activated output transistor is driven low enough, it enters the triode region, and therefore we have a naturally smooth reduction of the output current until its steady-state value is reached [27].

In our memory chip, the preset cycle is triggered by address transition detection. The entire read operation consists of the following successive steps: new address selection; address transition detection; output preset (during memory sensing) and data output transition. Of course, the output data is not valid during the output preset period. This determines the data hold time.

As preset is carried out during the memory sensing period, the precharge takes place even when consecutive 0's or 1's are read. This result in power consumption even when the read data does not change.

A. Pull-Down and Pull-Up Sections

The circuit schematic of the buffer is shown in Fig. 4. We describe the operation of the pull-down section ($V_{O,i}$ high, read datum low). The operation of the pull-up section is symmetrical.

During preset, as well as during the first part of the output transition, MD works in saturation. In a first approximation the output current i_O has a quadratic dependence on its overdrive voltage $v_{GS,D} - V_{TH}$:

$$i_O = k'_D \frac{W_D}{L_D}(v_{GS,D} - V_{TH})^2, \tag{8}$$

the symbols having an obvious meaning. To obtain a nearly linear output current ramp, the gate of the pull-down transistor (line GD) should be charged with a decreasing current [15]. In the preset period, this is achieved by means of the combined action of $M2A, M3A$ and $M5A$. $M2A$ behaves as an ideally constant current source. $M5A$ acts as a diode-connected transistor placed in series to the current source $M3A$. This series combination drains a current which decreases as the voltage on GD increases, since $M3A$ is forced to work in the triode region with a decreasing drain-to-source voltage. With suitable device sizing, we obtain the desired time dependence for $v_{GS,D}$ and, hence, for i_O.

When the output reaches the threshold voltage V_{T3} of the discriminator $D3$, the line $L3$ is switched high and begins to discharge GD. The output current then decreases, in accordance with the ideal waveform shown in Fig. 2. By careful sizing of $M9A$, we obtain a suitable time constant for the discharge of GD, thus achieving the desired falling edge of i_O.

When the preset phase is over, the read datum takes the control of the buffer. If it is low, block PD is enabled to charge the gate of MD. Again, the gate capacitance is charged with a decreasing current, so that the output current waveform approximates a linear ramp as long as MD works in saturation.

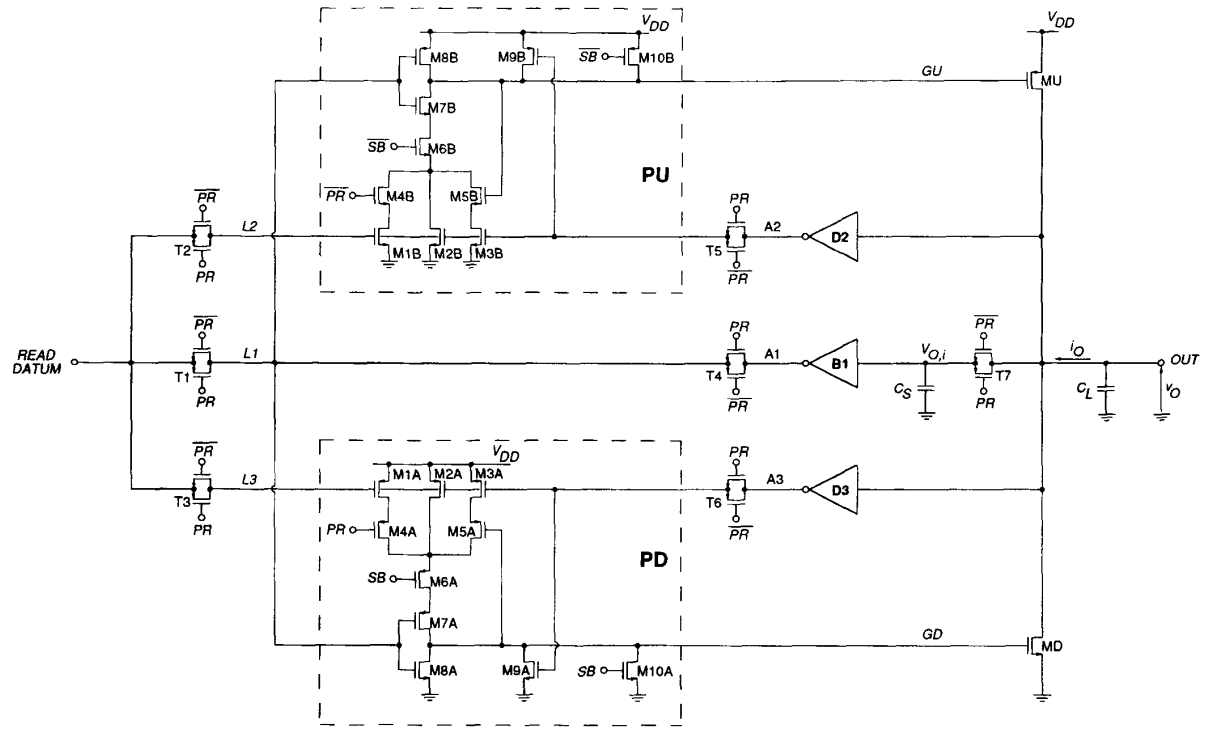

Fig. 4. Circuit diagram of the output buffer.

The main difference with respect to the preset operation is that switch $M4A$ is on. This provides an additional current contribution (source $M1A$) to the charging of line GD in order to compensate for the lower drain-to-source voltage of MD, thus obtaining a similar value for di_O/dt. As explained above, the falling edge of the output current waveform is obtained naturally after MD enters the triode region.

In static conditions, when the buffer has to continuously deliver a given output logic level, the enabled output transistor is driven with the maximum gate-to-source voltage (V_{DD}). A suitable size of the output devices allows us to meet the required static output level specifications.

During stand-by, both output transistors MU and MD are disabled by turning on $M10B$ and $M10A$. It is easily seen that the buffer shows zero power consumption both in static and in stand-by conditions.

B. Variable-Threshold Discriminator D3

A critical point for the preset phase comes from the uncertain value of the starting output voltage $V_{O,i}$. Depending on the previous history, $V_{O,i}$ may have any value. The worst situation corresponds to $V_{DD} > V_{O,i} > V_{O,pr}$. In this case, due to the wide starting range we have the problem of setting the optimum output level at which the output current slope should reverse. We solved this problem using the variable-threshold discriminator shown in Fig. 5. The voltage $V_{O,i}$, stored and sampled on C_S, controls the voltage V_C, which in turn adjusts the threshold voltage of the inverter $M5$–$M6$ through the action of $M4, M8, M9$. With the transistor sizes used, we

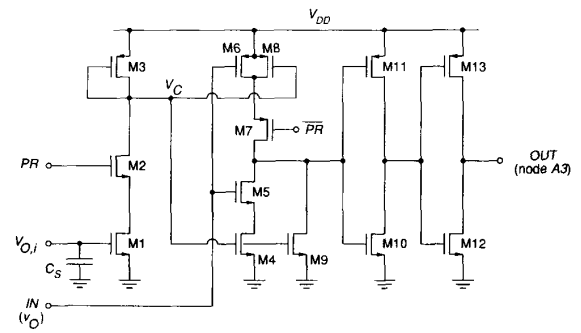

Fig. 5. Circuit diagram of the variable-threshold discriminator $D3$.

have a variation of the threshold voltage from 4.1 V to 2.1 V when $V_{O,i}$ ranges from 5 V to 2.5 V. Two additional inverters provide a sharp transfer characteristic. Switches $M2$ and $M7$ ensure zero power consumption out of preset conditions.

Since we do not have the above problem for $V_{O,i}$ low, we used a conventional inverting scheme for the discriminator $D2$ (Fig. 6(a)). $M15$ ensures zero power consumption out of preset operation. We adopted a similar topology for the inverting buffer $B1$ (Fig. 6(b)).

IV. Integration and Results

The buffer described was designed for a 0.6-μm EPROM CMOS process and was integrated in a 16-Mb EPROM device [28]. The active area of the buffer is less than 0.06 mm^2 (Fig. 7).

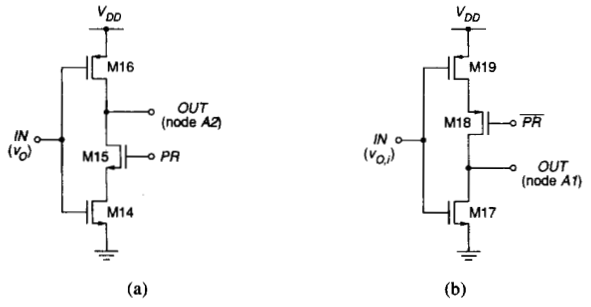

Fig. 6. Circuit diagram of the discriminator $D2$ (a) and of the inverting buffer $B1$ (b).

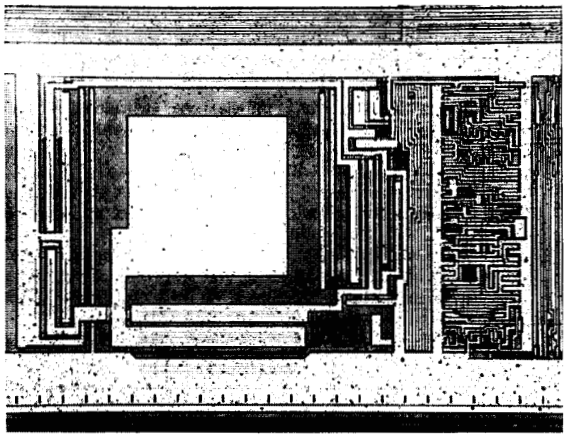

Fig. 7. Microphotograph of the integrated output buffer.

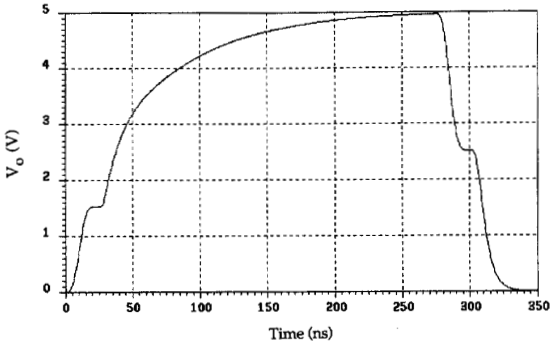

Fig. 8. Simulated output waveforms (C_L = 100 pF): (a) output voltage; (b) output current. Output transition sequence: 0 → 1 → 0. Preset periods: 1 to 26 ns and 276 to 301 ns.

The buffer was designed to complete the preset operation within 25 ns and to ensure that the specified dynamic output logic levels in the subsequent output transition are reached within 15 ns with a load capacitor C_L of 100 pF. This makes the circuit suitable for use in memory devices with an access time of ~60 ns. Dynamic output level specifications were $V_{OL,d}$ = 0.8 V and $V_{OH,d}$ = 2 V.

Fig. 8 shows the simulated output voltage and current waveforms for an output transition sequence 0 → 1 → 0 (C_L = 100 pF). The nominal output preset voltage $V_{O,pr}$ was set at ~2.5 V and ~1.5 V for $V_{O,i}$ equal to 5 V and 0 V, respectively. Target dynamic specifications were met for both preset and output transition. The time derivative of the output current was kept within ±4 mA/ns. If we make a comparison with buffers, designed for a similar fabrication technology, which provide comparable dynamic performance, we achieve an improvement in the peak switching noise by a factor of 4 considering a buffer using only preset without any current control, and by a factor of 6 considering a simpler solution that includes neither preset nor current control. The average current consumption of a single buffer with a cycle time of 60 ns (not including the current for charging/discharging the load capacitor) is less than 0.6 mA.

The 16-Mb EPROM chip was assembled in a 42-pin ceramic dual-in-line package. The parasitic package inductance of the ground and V_{DD} lines was 5 and 10 nH, respectively. Fig. 9 shows the measured output voltage waveform for the same output switching sequence 0 → 1 → 0 (C_L = 100 pF; simultaneous switching of 8 outputs). The actual sensing period in the EPROM device was ~45 ns. However, the target dynamic performance of the buffer is well within reach. The overall peak switching noise is kept within 240 mV. The buffer was also successfully evaluated with load capacitors larger than the specified value (Fig. 10). The effectiveness of the variable-threshold discriminator $D3$ was also demonstrated: the output voltage at the end of the preset period was between 2.6 V and 1.4 V for $V_{O,i}$ in the range from 5 V to 2.5 V (C_L = 100 pF).

Measured static output levels were V_{OH} = 3.5 V @ I_{OH} = −4 mA and V_{OL} = 0.2 V @ I_{OL} = 2.1 mA (V_{DD} = 4.5 V). The guaranteed data hold time of the memory chip is 5 ns.

V. Conclusion

A CMOS data output buffer suitable for use in integrated memories has been described. It minimizes the inductive bounces occurring on supply lines due to output switching while ensuring a high operation speed. The key aspect in the buffer operation is the use of output presetting techniques together with a suitable driving of the output pull-up and pull-down transistors. Output preset is performed during the memory addressing and sensing period. The driving waveform

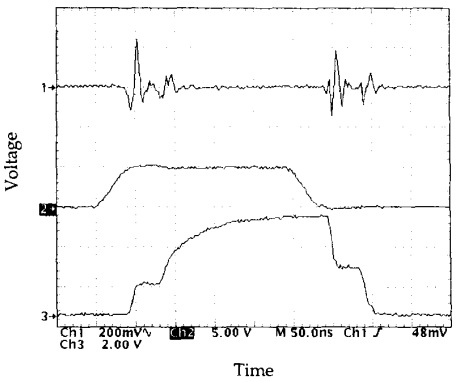

Fig. 9. Measured output voltage waveform ($C_L = 100$ pF; switching of 8 outputs). Track 1: voltage on V_{DD} pin (200 mV/div). Track 2: external address (5 V/div). Track 3: output voltage (2 V/div). Output transition sequence: $0 \rightarrow 1 \rightarrow 0$.

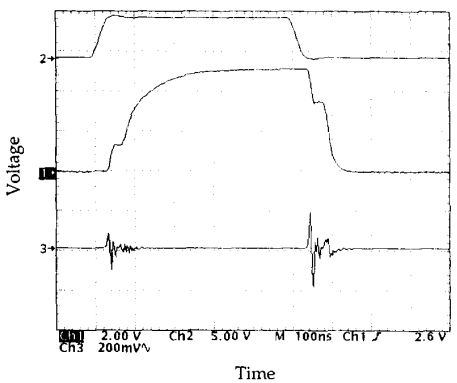

Fig. 10. Measured output voltage waveform ($C_L = 160$ pF; switching of 8 outputs). Track 1: output voltage (2 V/div). Track 2: external address (5 V/div). Track 3: voltage on ground pin (200 mV/div). Output transition sequence: $0 \rightarrow 1 \rightarrow 0$.

of the enabled output transistor is adequately controlled during both output preset and output transition. The experimental evaluation of the buffer integrated in a 16-Mb EPROM device has shown an output transition time within 15 ns with a 100 pF load capacitor, thereby fulfilling the target speed requirements of such memories. The proposed technique can also be applied for higher operation frequencies such as 66 MHz bus clock. In this case, of course, higher switching noise together with larger power dissipation must be accounted for.

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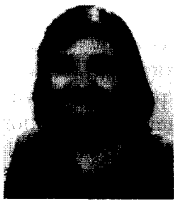

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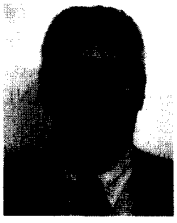
Miss Chioffi is a member of the Italian Electrotechnical and Electronic Society.



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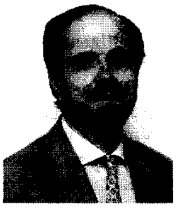

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