

# A Programmable 1.5 V CMOS Class-AB Operational Amplifier with Hybrid Nested Miller Compensation for 120 dB Gain and 6 MHz UGF

Ruud G. H. Eschauzier, Ron Hogervorst, and Johan H. Huijsing

**Abstract**—The paper presents a rail-to-rail class-AB operational amplifier in a standard  $v_{th} = 0.6$  V CMOS technology operating at 1.5 V. A hybrid nested Miller compensation technique yields 6 MHz unity gain frequency at 300  $\mu$ A supply current, 120 dB gain and programmability. Operation down to 1.0 V at 15  $\mu$ A is possible with 400 kHz UGF. The die area of the chip is 0.05 mm<sup>2</sup> (70 mil<sup>2</sup>).

## I. INTRODUCTION

TRADITIONALLY, CMOS operational amplifiers apply cascoding techniques to ensure an acceptable gain with a minimal number of gain stages. The use of cascodes, however, fundamentally limits the lowest supply voltage at which the amplifier circuit is able to operate. Furthermore, the apparent trend towards lower threshold voltages of CMOS processes endangers the applicability of cascoded circuits in the near future. The two restrictions on the use of cascoded opamps are illustrated by Fig. 1 and Fig. 2.

The most immediate drawback of the cascoded amplifier is its relatively high minimum supply voltage. Fig. 1 presents the simplified schematic of a conventional operational amplifier with a push-pull output stage [1]. It consists of the input stage  $M_{30} - M_{35}$  and the output stage  $M_{10}/M_{20}$  separated by cascode transistors  $M_{21}$  and  $M_{24}$ . The bold lines indicate the places where the stacked drain-source voltages of two cascode transistors are present on top of the gate-source voltage of an output transistor. The summed saturation voltages of the cascodes raise the lowest supply voltage one saturation voltage above the minimum obtainable. The minimum supply voltage of a CMOS operational amplifier is mainly determined by the gate-source voltage of the output transistors under the maximum output current condition. When driving high output currents, the supply voltage must suffice to build up the gate-source voltage of the output transistors plus the loss in the driving circuit. The two cascode devices account for a loss equal to their two summed saturation voltages. The minimum supply voltage  $V_{min}$  is therefore given by

$$V_{min} = V_{GS,max} + 2V_{Dsat} \quad (1)$$

where  $V_{GS,max}$  is the gate-source voltage of the output transistors when driving maximum output current. Considering that

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The authors are with Delft University of Technology, Faculty of Electrical Engineering, Mekelweg 4, 2628 CD Delft, The Netherlands.  
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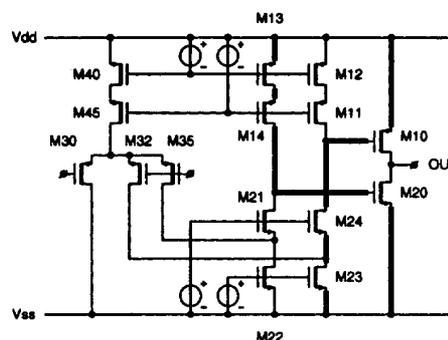


Fig. 1. Limitation on the minimum supply voltage of the conventional cascoded opamp.

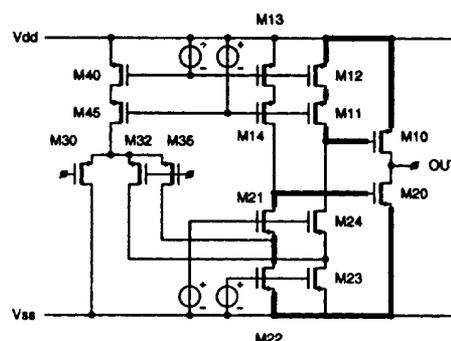


Fig. 2. Limitation on the minimum threshold voltage of the cascoded opamp.

theoretically a single transistor can drive the output transistors, an optimal circuit requires a supply voltage of only

$$V_{min} = V_{GS,max} + V_{Dsat} \quad (2)$$

The supply voltage that follows from (2) is the lowest minimum supply voltage for any CMOS amplifier. A circuit that operates at this limit will therefore be referred to as ultimate low voltage.

A second, more long term, drawback of the cascode circuit is that it is not suited for future I.C. processes with lower threshold voltages. The bold lines in Fig. 2 indicate the places where two stacked drain-source voltages are present between the gate and the source of an output transistor. These are the critical points with respect to the lowest acceptable threshold

voltage of the manufacturing I.C. process. Under quiescent conditions, when the current through the output devices is low, the gate-source voltage  $V_{GS}$  will be close to the threshold voltage  $V_{th}$ . For correct operation of the amplifier, the stacked drain-source voltages  $V_{DS}$  of the cascode transistors  $M_{11}/M_{12}$  and  $M_{21}/M_{22}$  must fit into the gate-source voltages  $V_{GS}$  of the output transistors. Since the lowest drain-source voltage for normal operation is the saturation voltage  $V_{Dsat}$ , the summed saturation voltages have to be smaller than the gate-source voltages of the output transistors. The gate-source voltages  $V_{GS}$  of the output transistors lower proportionally to the threshold voltage, however, while the saturation voltage remains fixed. Redimensioning the circuit for a lower threshold process therefore requires an increased  $W/L$  ratio of the cascode transistors, enlarging the occupied die area. The continuously diminishing threshold voltages will eventually result in excessively large cascode components.

The observation that the cascode transistors must be widened to reduce their saturation voltage in processes with a lower threshold voltage becomes more alarming, when it is realized that there is a fundamental limit to the reduction of the saturation voltage. This lower limit is set by the subthreshold saturation voltage of a MOS device. The cascode transistors enter the subthreshold mode of operation when they have been widened to such extent that their current densities drop below the limit for normal operation. Under the subthreshold regime, a MOS transistor essentially operates as a bipolar component, with a fixed saturation voltage. The value is given by

$$V_{Dsat,st} \approx \frac{4kT}{q} \quad (3)$$

which amounts to approximately 100 mV at room temperature. The minimum threshold voltage of the process in which the opamp can still be realized, will eventually be limited by this subthreshold saturation voltage.

The absolute minimum threshold voltage for the cascoded opamp can be found by considering that the two stacked saturation voltages of the cascodes not only have to fit into the nominal threshold voltage, but also, to guarantee an acceptable yield, in its minimum value. The maximum deviation of the threshold voltage is in practice given by the  $3\sigma$  limit. It lies in the order of 150 mV and is not expected to improve appreciably in the future. Combining this value with the subthreshold saturation voltage, the minimum acceptable threshold voltage  $V_{th,min}$  can be found as

$$V_{th,min} = 2V_{Dsat,st} + V_{d,max} \quad (4)$$

where  $V_{Dsat,st}$  is the minimum saturation voltage of the cascode devices and  $V_{d,max}$  is the  $3\sigma$  deviation of the threshold voltage from its typical value.

Equation (4) boils down to approximately 350 mV at room temperature. Realized in a CMOS process with a threshold voltage lower than this value, the gain of the cascoded amplifier will rapidly decrease and the amplifier will become inoperative. This finding strongly suggests that the future applicability of cascoded opamps is uncertain. Fig. 3 substantiates the prediction by showing the development of the threshold voltage as derived from a decade of volumes of the IEEE

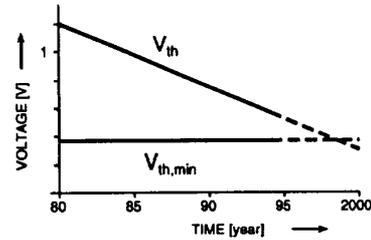


Fig. 3. Development of the threshold voltage compared to the minimum value for conventional topologies.

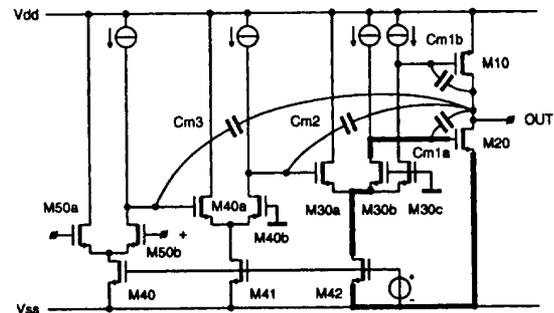


Fig. 4. Opamp with four cascaded gain stages and Nested Miller Compensation.

JOURNAL OF SOLID-STATE CIRCUITS. The horizontal line in the Fig. represents the minimum threshold voltage of 350 mV. The descending line, which plots the threshold voltage of a typical process, lies well above this limit for early and more recent processes. Although the  $W/L$  ratio of the cascode transistors already may have to be large, no severe problems are faced when realizing the cascoded opamp at this moment. By the turn of the century, however, the gate-source voltage of the output transistors is likely to drop below the value where it becomes impossible to accommodate the two stacked drain-source voltages of the cascode transistors. At that moment an important class of opamp circuits will lose its significance.

The traditional alternative to cascodes to obtain a high gain is the use of a cascade topology. Cascading or chaining amplifier stages is an effective approach to obtain a high gain. Conventional cascoded CMOS amplifiers suffer from identical restrictions as their cascode counterparts. These limitations are strongly related to necessity for frequency compensation.

Methods to robustly frequency compensate operational amplifiers containing four stages are rare. An exception is the nested Miller compensation (NMC) structure [2]. This compensation strategy consists of Miller capacitors that are nestedly connected from the output terminal of the amplifier to the inputs of the subsequent internal amplifier stages. Fig. 4 shows a four stage nested Miller compensated amplifier with push-pull output stage. Capacitors  $C_{m1}$ ,  $C_{m2}$ , and  $C_{m3}$  are the respective nested capacitors. Differential pairs implement the stages  $M_{30}$  and  $M_{40}$  to accomplish a correct sign for the feedback loops closed by the Miller capacitors.

The differential pairs in the NMC circuit lead to the presence of two stacked drain-source voltages inside the gate-source

voltages of the output transistor and two drain-source voltages on top of these gate-source voltages. The bold lines in Fig. 4 reveal the voltage loops of the first limitation.

This paper describes two ultimate low voltage amplifiers. Realized in a  $V_{th} = 0.6$  V CMOS process and with a total supply current of  $300 \mu\text{A}$ , their minimum supply voltage is 1.5 V. Reducing the total supply current to  $16 \mu\text{A}$ , the minimum supply voltage becomes as low as 1.1 V. Furthermore, the opamps will remain functional in future processes with extremely low threshold voltages. The keys to these results are the techniques used for the frequency compensation. The first opamp employs a hybrid nested Miller compensation scheme, resulting in a unity gain frequency of 2 MHz. The second is compensated by a multipath hybrid nested Miller structure. Its unity gain frequency is 6 MHz. The bandwidth improvement relies on a multipath input stage that directly drives the output transistors, thus bypassing the intermediate stages. Since the multipath technique depends on transconductance and capacitor ratios only, the pole-zero doublet inherent to feedforward techniques can be matched as closely as 1% in a standard CMOS technology. Both opamps have a D.C. gain of 120 dB.

In Section II the principles of operation of hybrid nested Miller compensation and multipath hybrid nested Miller compensation are explained. Section III addresses two ultimate low voltage CMOS opamps. The experimental results are shown in Section IV, and finally Section V gives the conclusions.

## II. PRINCIPLE OF OPERATION

Summarizing, the two demands on CMOS ultimate low-voltage operational amplifier circuits prepared for future lower threshold voltages, are

- Only one stacked drain-source voltage  $V_{DS}$  in between the gate and the source of an output transistor.
- Only one drain-source voltage  $V_{DS}$  on top of the gate-source voltage of an output transistor.

Fig. 5 suggests a basic topology of the opamp that meets the ultimate low voltage demands. It comprises of three cascaded common source NMOS transistors  $M_{10} - M_{30}$  and a differential input stage  $M_{40}$ . Because of the inverting nature of the intermediate and output stages, traditional frequency compensation techniques fail. Consider Fig. 6 for instance, which shows the circuit with three additional capacitors for nested Miller compensation. The capacitors intend to separate the poles at each of the nesting levels, resulting in a straight 20 dB/dec roll-off of the gain magnitude. The middle Miller capacitor  $C_{m2}$  closes a feedback loop with a positive sign, however. The positive feedback will direct the poles into the right half of the complex  $s$ -plane and the circuit will become unstable even before overall feedback is applied.

### A Hybrid Nested Miller Compensation

The proposed solution for frequency compensation is the hybrid nested Miller compensation (HNMC) structure, depicted in Fig. 7. The structure again employs feedback capacitors, comparable to nested Miller compensation, but in this case the two Miller loops with  $C_{m1}$  and  $C_{m2}$  are at the same nesting level. It can easily be verified that the feedback sign of all

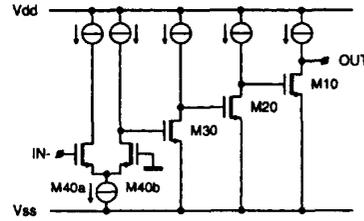


Fig. 5. Basic ultimate low-voltage topology.

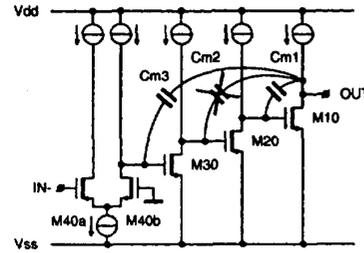


Fig. 6. Ultimate low-voltage circuit with traditional nested Miller compensation.

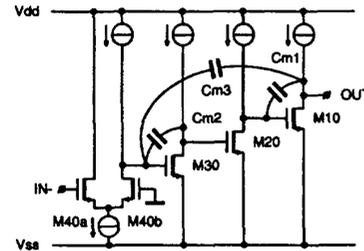


Fig. 7. Ultimate low-voltage circuit with hybrid nested Miller compensation.

internal loops is correct. This is the case for the loops with  $C_{m1}$  and  $C_{m2}$ , since these are ordinary Miller capacitors, but also  $C_{m3}$  is part of a negative feedback loop, because three inverting stages are present between its terminals.

For the purpose of analysis, the hybrid nested Miller structure is redrawn in Fig. 8 with the added dashed capacitor-resistor combinations  $p_2 - p_4$ . These represent the intermediate poles of the respective stages. The load impedance constitutes pole  $p_1$ . The effect of the two Miller capacitors at the lowest nesting level  $C_{m1}$  and  $C_{m2}$  is shown in Fig. 9. The line  $a$  in this figure plots the frequency response of the circuit without the feedback capacitors. Clearly the four dominating poles can be distinguished. Inserting the two Miller capacitors  $C_{m1}$  and  $C_{m2}$  cause the two poles at the input and the output of each of the transistors to split apart. Capacitor  $C_{m1}$  moves pole  $p_1$  up to  $p'_1$  and  $p_2$  down to  $p'_2$ , while capacitor  $C_{m2}$  positions  $p_3$  at the higher frequency  $p'_3$  and  $p_4$  at the lower frequency  $p'_4$ . The shifting of the poles results in the curve  $b$  in the Bode of Fig. 9. The transfer now contains the two dominating poles  $p'_2$  and  $p'_4$ . Miller capacitor  $C_{m3}$  splits these poles apart, as shown by line  $c$  of Fig. 9. The result is the much desired 20 dB/dec slope, up to the third order secondary poles  $p''_1$ ,  $p''_2$  and  $p''_3$ . The dominating pole frequency of the overall frequency response is  $p''_4$ .

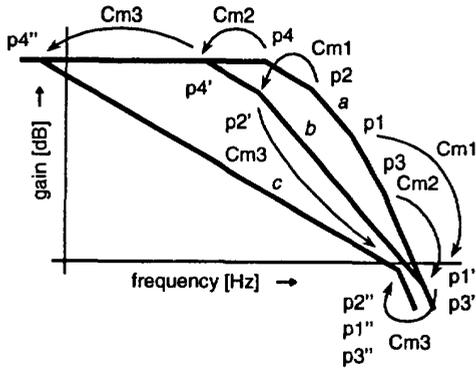


Fig. 8. Poles of the hybrid nested Miller compensation circuit.

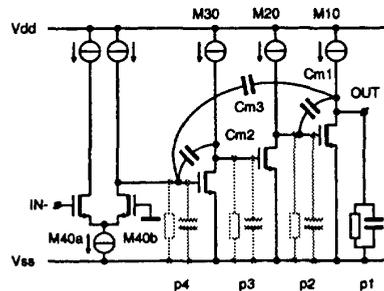


Fig. 9. Pole positioning of the hybrid nested Miller compensation structure.

The expressions for the dimensioning of the hybrid nested Miller compensation structure can be derived from demanding a maximal flat (Butterworth) amplitude response of the opamp with unity gain feedback. Since unity gain is the worst case condition, this approach secures that the amplifier will be stable for any resistive feedback network. The frequency compensation is well designed when

$$\frac{g_{m20} C_{m3}}{C_{m1} C_{m2}} = \frac{1}{2} \frac{g_{m10}}{c_l} \quad (5)$$

where  $c_l$  is the load capacitance, and

$$\omega_t = \frac{g_{m40}}{C_{m3}} \leq \frac{1}{4} \frac{g_{m10}}{c_l} \quad (6)$$

where  $\omega_t$  is the unity gain frequency of the opamp. The equality sign in (6) corresponds to the limiting case of a maximal flat response, while the inequality yields an even higher degree of stability.

Equation (6) indicates that the maximum unity gain frequency of the hybrid nested Miller compensation structure is determined by the transconductance of the output stage and the load capacitance  $c_l$ . This is equivalent to the two-stage case with ordinary, single, Miller compensation. Since such an amplifier can have a unity gain frequency of  $\omega_t = g_{m10}/(2c_l)$ , the bandwidth reduction of hybrid nested Miller compensation compared to single Miller compensation is a factor 2. Although this reduction is clearly undesirable, it is better than what can be obtained from nested Miller compensation, which would reduce the bandwidth by another factor of 2. The key to this

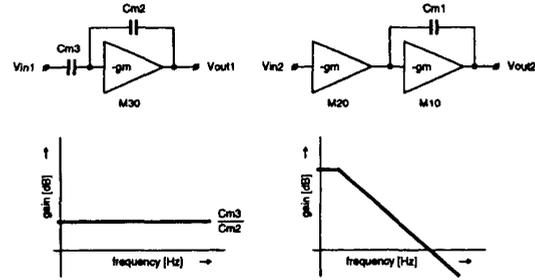


Fig. 10. Hybrid nested Miller compensation with additional multipath input stage.

improvement lies in the fact that four stage hybrid nested Miller compensation only has two nesting levels, whereas nested Miller compensation has three. Every nesting level results in approximately a factor of two bandwidth reduction. Therefore the realizable bandwidth of *four*-stage hybrid nested Miller compensation is equal to that of *three*-stage nested Miller compensation. This is reflected by the dimensioning equations (5) and (6), which are identical to the expressions for *three*-stage nested miller Compensation [4], except for the factor  $C_{m3}/C_{m2}$  in (5). The appearance of this factor can be understood from Fig. 10. In this figure, representing the transistors by the idealized transconductors, the outer Miller loop with  $C_{m3}$  is opened and the circuit divided into two parts. The part on the right, consisting of transistors  $M_{10}$  and  $M_{20}$ , can be thought of as a two-stage Miller compensated amplifier. The left part, comprising  $M_{30}$ , acts as a voltage amplifier with a flat frequency response. The capacitive feedback network around  $M_{30}$  results in a voltage-to-voltage amplifier with a gain of  $C_{m3}/C_{m2}$ . This gain accounts for the factor in (5), since it boosts the signal that is fed back from the output, through the outer Miller capacitor  $C_{m3}$  to the gate of  $M_{20}$ .

The representation of the hybrid nested Miller compensation structure of Fig. 10 suggests an additional design consideration. For the dimensioning expressions (5) and (6) it is assumed that the voltage amplifier with  $M_{30}$  has an infinite bandwidth. This is clearly not the case, since a pole in the transfer will occur at a frequency determined by the input impedance of the integrator  $M_{30}/C_{m2}$  and the Miller capacitor  $C_{m3}$ . The location of the pole is given by  $g_{m30}/C_{m3}$ . To eliminate the effect of this pole, it must lie well above the unity gain frequency of the feedback loop closed by  $C_{m3}$ . That requirement leads to the final dimensioning equation

$$\frac{g_{m30}}{C_{m3}} > \frac{g_{m10}}{c_l} \quad (7)$$

### B. Multipath Hybrid Nested Miller Compensation

Although the bandwidth reduction of hybrid nested Miller compensation is small compared to other methods for frequency compensation, in some cases even this small reduction is not acceptable. In that situation the multipath technique is an attractive option [4], resulting in multipath hybrid nested Miller compensation (MHNMC). Fig. 11 shows a multipath hybrid nested Miller compensated amplifier. Added to the previous circuit of Fig. 10 is an additional input stage  $M_{50}$

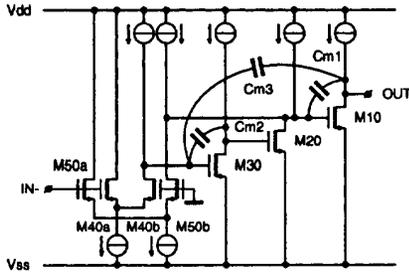


Fig. 11. Basic multipath hybrid nested Miller compensation schematic.

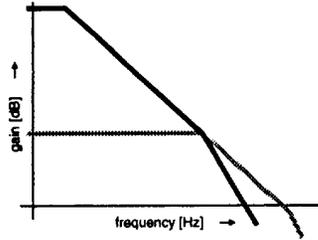


Fig. 12. Frequency response of the multipath hybrid nested Miller compensation technique.

that directly drives the output transistor  $M_{10}$ . The extra input stage and the output stage together constitute a two-stage amplifier with relatively low gain, but a high bandwidth. This is presented in the Bode plot of Fig. 12 by the light line. The rest of the circuit, a four stage amplifier with hybrid nested Miller compensation, couples a low bandwidth to a high gain. This leads to the solid line in Fig. 12. The two curves together yield a 20 dB/dec roll-off with both a high unity gain frequency and a high gain. Since the bandwidth is determined by the two-stage amplifier with single Miller compensation, it is close to the theoretical maximum that can be obtained with a given transconductance of the output stage and load capacitance.

The dimensioning equations for multipath hybrid nested Miller compensation are very similar to those obtained for the circuit without the multipath input stage. The first expression is

$$\frac{g_{m20}C_{m3}}{C_{m1}C_{m2}} \approx \frac{1}{20} \frac{g_{m10}}{c_l} \quad (8)$$

This relation is not very critical. It basically states that, everything else remaining the same, the transconductance  $g_{m20}$  of the second stage should be chosen considerably smaller in case of MHNMC than for HNMC. This is a prime aspect of the multipath technique and is related to the fact that the positions of the poles do not change because of the multipath input stage. Hence, adding the parallel input stage without redimensioning the circuit will not lead to any bandwidth improvement. The value of 20 in the denominator of the right hand term is a practical compromise. A higher value, which improves the bandwidth slightly, would require an extremely low transconductance of the third stage  $M_{20}$ , however. This in turn would render its drain currents unmanageably small.

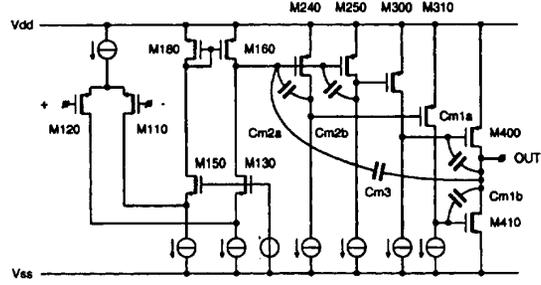


Fig. 13. Simplified schematic of the ultimate low-voltage amplifier.

The second design equation for multipath hybrid nested Miller compensation becomes

$$\omega_t = \frac{g_{m40}}{C_{m3}} \leq \frac{1}{2} \frac{g_{m10}}{c_l} \quad (9)$$

which is indeed a factor of two higher than the corresponding expression (6) for hybrid nested Miller compensation.

Due to the easing of the bandwidth requirement of the four-stage amplifier part—it merely has to supply the gain—(7) for multipath hybrid nested Miller compensation relaxes into

$$\frac{g_{m30}}{C_{m3}} > \frac{1}{10} \frac{g_{m10}}{c_l} \quad (10)$$

The introduction of the factors 1/20 in (8) and 1/10 in (10) indicate that the bias currents of the multipath hybrid nested Miller compensated circuit can be considerably lower than those of the hybrid nested Miller amplifier. In practical situations this will about balance the extra current required for the multipath input stage. Therefore, the bandwidth amelioration of the multipath technique goes without a current penalty and the bandwidth-to-power ratio is improved. Also the die area of the chip does not increase when using multipath hybrid nested Miller compensation, since the higher bandwidth allows the compensation capacitors to be chosen smaller.

A fourth dimensioning expression that has no counterpart in hybrid nested Miller compensation, arises from the fact that the two sections that constitute the 20 dB/dec slope of Fig. 13 have to be closely matched. If the matching is not accurate, a pole-zero doublet occurs in the passband. Placing the pole exactly on the zero requires

$$\frac{g_{m50}}{g_{m40}} = \frac{C_{m1}}{C_{m3}} \quad (11)$$

Since this relation depends on transconductance and capacitor ratios only, matching can be as close as about 1% in a standard CMOS process and 0.1% for a bipolar technology.

### III. THE ULTIMATE LOW VOLTAGE OPAMPS

Fig. 13 shows the simplified circuit of the ultimate low voltage opamp with a push-pull output stage for obtaining rail-to-rail operation. The  $P$ -channel input pair  $M_{110}/M_{120}$  followed by folded cascodes  $M_{130}/M_{150}$  ensures a common mode input range that includes the negative rail. The current mirror  $M_{160}/M_{180}$  performs differential-to-single conversion

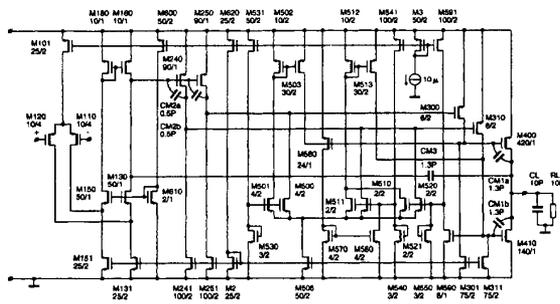


Fig. 14. Total schematic of the ultimate low-voltage opamp with hybrid nested Miller compensation.

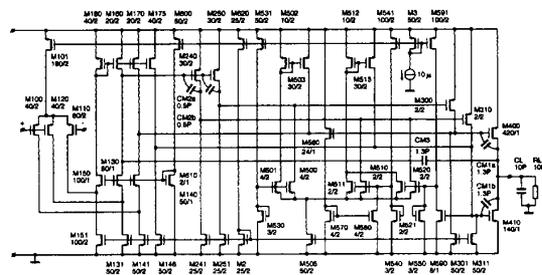


Fig. 15. Total schematic of the ultimate low-voltage opamp with multipath hybrid nested Miller compensation.

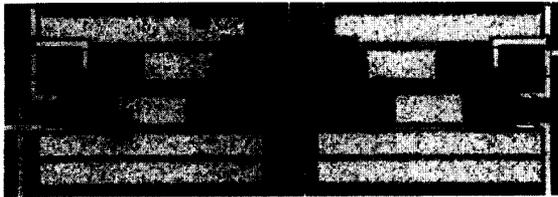


Fig. 16. Die photomicrographs of the two ultimate low-voltage CMOS opamps.

of the signal. The four gain stages can be recognized as the input stage  $M_{110}/M_{120}$ , the first intermediate stage  $M_{240}/M_{250}$ , the second intermediate stage  $M_{300}/M_{310}$  and finally the output stage  $M_{400}/M_{410}$ . The intermediate stages comprise two transistors each to correctly generate the driving signals for the push-pull output stage. The capacitors in Fig. 13 are inserted according to the hybrid nested Miller compensation scheme. The lowest level capacitors are also doubled to deal with push-pull output stage.

Fig. 14 shows the total schematic of the realized low-voltage opamp circuit with hybrid nested Miller compensation. Added to the simplified circuit of Fig. 13 are biasing elements and a feedback class-AB control which ensures a minimum quiescent current through the inactive output transistor to prevent shut-off. The four amplifier stages in Fig. 14 are: input stage  $M_{110}/M_{120}$ , second stage  $M_{240}/M_{250}$ , third stage  $M_{300}/M_{310}$  and output stage  $M_{400}/M_{410}$ . The hybrid nested Miller capacitors are inserted according to Fig. 13. The class-AB control is constructed around differential amplifier  $M_{501}$  —

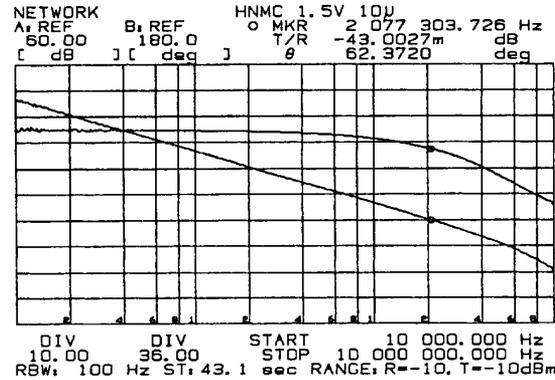


Fig. 17. Measured frequency response of the ultimate low-voltage opamp with hybrid nested Miller compensation.

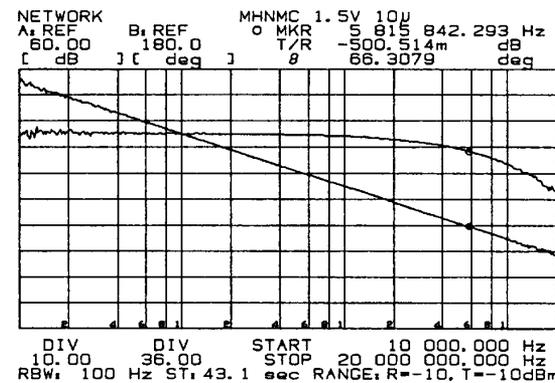


Fig. 18. Measured frequency response of the ultimate low-voltage opamp with multipath hybrid nested Miller compensation.

$M_{520}$ . The currents through output devices  $M_{400}$  and  $M_{410}$  are measured by  $M_{560}$  and  $M_{590}$ . The drain currents of these measurement transistors are converted into voltages at the gates of  $M_{511}/M_{510}$  and  $M_{521}/M_{520}$ , two inputs of the class-AB control amplifier. The voltage that represents the lowest of the two output transistor currents is compared to the reference voltage available at the third input of the control amplifier, the gates of transistors  $M_{501}/M_{500}$ . The selection of the input voltage that corresponds to the smallest transistor current is performed by the decision pair consisting of transistors  $M_{510}$  and  $M_{520}$ . The transistor that senses the highest voltage at its gate enters the active current conducting mode. It therefore acts as a source follower, transferring its gate-voltage to the common source node of the class-AB amplifier. The other device, with the lowest gate voltage, is shut off and does not contribute to the signals in the class-AB loop. Depending on the difference between the actual lowest transistor current and the aimed at limiting value, a correction signal is fed to the input of the third gain stage ( $M_{300}/M_{310}$ ). To guarantee stability of the class-AB control loop an identical signal is fed directly to the output transistors, bypassing the third stage. This is analogous to the use of a multipath input stage for the overall frequency compensation of the circuit. The low gain-high frequency parallel path passes through the current mirrors  $M_{502}/M_{503}$  and  $M_{512}/M_{513}$ .

TABLE I  
MEASUREMENT RESULTS OF THE ULTIMATE LOW  
VOLTAGE CMOS OPAMPS AT  $I_{DD} = 300\mu A$ .

symbol	parameter	condition	HNMC			MHNMC			unit
			min	typ	max	min	typ	max	
$T_{op}$	temperature range		-55		125	-55		125	°C
$V_{dd}$	supply voltage range		1.5		5.5	1.5		5.5	V
$I_{dd}$	supply current	$V_{dd}=1.5V$		300			290		$\mu A$
$I_o$	max/min output current			5			5		mA
$V_{out}$	output voltage swing	over full temperature range	$V_{dd}\times 0.2$		$V_{dd}\times 0.2$	$V_{dd}\times 0.2$		$V_{dd}\times 0.2$	V
$V_{os}$	offset voltage		3			4			mV
$A_{ol}$	open loop voltage gain			120			120		dB
$f_{ug}$	unity gain frequency			2			6		MHz
$\phi_m$	phase margin	over full temperature range		59		65		60	°
$S_r$	slew rate			5			13		V/ $\mu s$
$T_s$	1% settling time (100mV step)			320			140		ns

TABLE II  
MEASUREMENT RESULTS OF THE ULTIMATE LOW VOLTAGE  
CMOS OPAMPS AT APPROXIMATELY  $I_{DD} = 15\mu A$ .

symbol	parameter	condition	HNMC			MHNMC			unit
			min	typ	max	min	typ	max	
$T_{op}$	temperature range		-55		125	-55		125	°C
$V_{dd}$	supply voltage range		1.5		5.5	1.5		5.5	V
$I_{dd}$	supply current	$V_{dd}=1.1V$		16			15		$\mu A$
$I_o$	maximum output current			0.5			0.5		mA
$V_{out}$	output voltage swing	over full temperature range	$V_{dd}\times 0.1$		$V_{dd}\times 0.1$	$V_{dd}\times 0.1$		$V_{dd}\times 0.1$	V
$V_{os}$	offset voltage		3			4			mV
$A_{ol}$	open loop voltage gain			120			120		dB
$f_{ug}$	unity gain frequency			0.2			0.6		MHz
$\phi_m$	phase margin	over full temperature range		58		64		45	°
$S_r$	slew rate			0.2			0.7		V/ $\mu s$
$T_s$	1% settling time (100mV step)			2900			1570		ns

Fig. 15 shows the total schematic of the ultimate low voltage opamp with multipath hybrid nested Miller compensation. Apart from the multipath input stage, comprising transistor  $M_{100}$ , and the subsequent transistors in its signal path, the circuit is identical to that of the hybrid nested Miller compensated amplifier. Some of the biasing components have been redimensioned, however, to comply with the design equations (8)–(11).

IV. REALIZATIONS AND MEASUREMENT RESULTS

The CMOS operational amplifier with hybrid nested Miller compensation and the circuit with the multipath technique to double the bandwidth have been realized in a standard  $V_{th} = 0.6V$  process with a minimum feature size of  $0.8\mu m$ . The photomicrographs of the chips are shown in Fig. 16. The micrographs demonstrate that, despite the fact that for practical purposes the capacitors of both circuits were chosen to be the same values, there is hardly any die area penalty for the addition of a multipath input stage. The area of both chips is  $0.05mm^2$  ( $70mil^2$ ). Further, although the class-AB control appears to be rather complex in the circuit diagram, the occupied die area of this circuit part is negligible. This is due to the small sizes of the devices in the class-AB circuit. Fig. 17 shows the open loop Bode plot of the opamp with

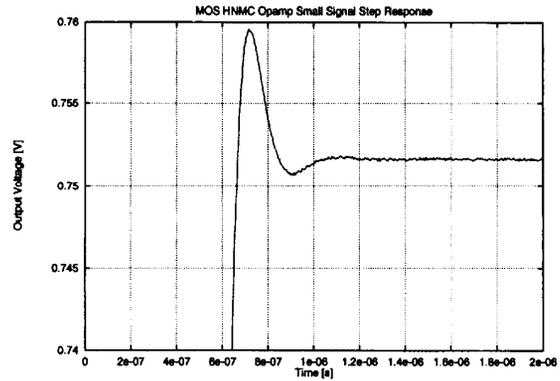


Fig. 19. Step response of the ultimate low-voltage opamp with hybrid nested Miller compensation.

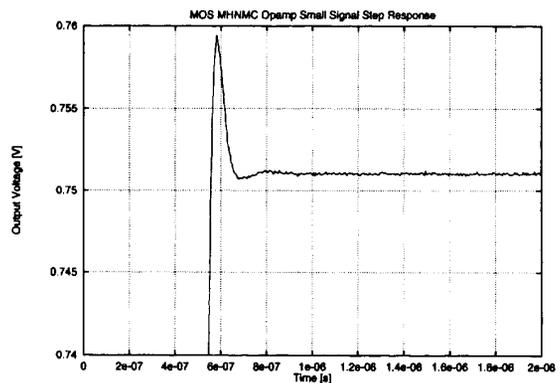


Fig. 20. Step response of the ultimate low-voltage opamp with multipath hybrid nested Miller compensation.

hybrid nested Miller compensation of Fig. 13 at a total supply current of  $300\mu A$ . The unity gain frequency is 2 MHz.

The Bode plot of Fig. 17 demonstrates the effect of a second input stage on the unity gain frequency by showing the open loop gain of the circuit with multipath hybrid nested Miller compensation. The unity gain frequency now rises to 6 MHz, slightly more than expected. In both cases the load of the opamp consisted of a  $10k\Omega$  resistor parallel to a capacitor of  $10pF$ . Finally, the responses of the two amplifiers to a  $100mV$  step input are shown in Figs. 19 and 20. The higher bandwidth of the multipath hybrid nested Miller compensated amplifier is reflected in the more narrow peak in the step response. No slow settling components are detectable in the plot, indicating that the matching of the pole-zero doublet is better than 1%. The settling times to 1% are 320 and 140 ns, respectively.

The experimental results of the CMOS opamps are gathered in two tables. To illustrate the robustness of the hybrid nested Miller compensation structure, the measurements were performed at two quiescent supply currents: approximately  $300\mu A$  (Table I) and approximately  $15\mu A$  (Table II). The programming of the quiescent current was accomplished by varying the bias current source feeding  $M_3$ . In the  $16\mu A$  case the unity gain bandwidth reduces to 400 kHz for the

MHNMC amplifier, but also the minimum allowable supply voltage lowers to 1.1 V, bringing the total power consumption down to 17  $\mu$ W.

#### V. CONCLUSION

The design of ultimate low voltage CMOS opamps topologies, requires frequency compensation methods that are suited for a cascade of inverting gain stages. Hybrid Nested Miller compensation and multipath hybrid nested Miller compensation meet that demand, whereas traditional methods fails. Employing these new techniques, a four stage CMOS opamp with a gain of 120 dB and a unity gain frequency of 6 MHz is demonstrated. The operational amplifier operates at a supply voltage of 1.5 V and consumes 300  $\mu$ A of supply current. The supply current can be programmed down to 16  $\mu$ A, reducing the minimum supply voltage even further to 1.1 V. Furthermore, the opamp topology is suited for use in future manufacturing processes with substantially lower threshold voltages.

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**Ruud G.H. Eschauzier** was born in Vlaardingen, the Netherlands, on August 10, 1967. He received the M.Sc. degree in electrical engineering in 1990 from the Delft University of Technology.

He is now finishing the Ph.D. degree at the Electronic Instrumentation Laboratory of the Delft University. His research subjects include analog integrated circuits with extremely high bandwidth-to-power ratios.



**Ron Hogervorst** was born in Voorschoten, the Netherlands, on December 2, 1967. In 1991 he received the M.Sc. degree in electrical engineering from the Delft University of Technology, Delft, The Netherlands.

Since then he has been working towards the Ph.D. degree at the same university on the subject of CMOS low-voltage operational amplifiers.



**Johan H. Huijsing** was born in Bandung, Indonesia, on May 21, 1938. He received the M.Sc. degree in electrical engineering from the Delft University of Technology, Delft, the Netherlands, in 1969, and the Ph.D. degree from this University in 1981 for work on operational amplifiers. His thesis was "Integrated Circuits for Accurate Linear Analogue Electric Signal Processing," supervised by Prof. I. J. Davids.

Since 1969 he has been a member of the Research and Teaching Staff of the Electronic Instrumentation Laboratory, Department of Electrical Engineering, Delft University of Technology, where he is now Professor of Electronic Instrumentation. He teaches courses on Electrical Measurement Techniques, Electronic Instrumentation, Operational Amplifiers and Analog-to-Digital Converters. His field of research is analog circuit design (operational amplifiers, analog multipliers, etc.) and integrated smart sensors (signal conditioning on the sensor chip, frequency and digital converters which incorporate sensors, bus interfaces, etc).

Dr. Huijsing is the author or co-author of approximately 100 scientific papers and has filed 15 patents.