1 V Power Supply, Low-Power Consumption A/D Conversion Technique with Swing-Suppression Noise Shaping

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***Abstract*— A 1 V power supply and low-power consumption A/D conversion technique using swing-suppression noise shaping is proposed. This technique makes it possible to power the on chip A/D converter in digital LSI's directly by a one-cell battery, without a dc–dc converter. Experimental results indicated good performance for the RF-to-baseband analog interface of a digital cordless phone. The A/D converter, fabricated with a 0.5 μm CMOS process, operates on a 1 V power supply, has a 10 bit dynamic-range with a 384 ksps sampling speed and consumes only 1.56 mW.**

I. Introduction

BATTERY operated cordless equipment, such as cellular phones, audio and video equipment, and multimedia devices, are widely used because of their portability. The key components for lighter and higher performance portable devices are VLSI's. Low-power circuit designs for longer battery life and onchip analog interfaces for the man-machine interface are the main requirements for the LSI's described herein [1].

For low-power digital LSI's, various circuit schemes [2], parallel architecture [3] and several process technologies [4], [5] have been proposed. The most effective way to reduce power consumption is to reduce the supply voltage, since the power consumption is determined by CV^2f and falls in proportion to the square of the supply voltage. Because the lowest voltage from a single-cell rechargeable battery or dry cell is 1 volt, we have developed 1-V high-speed digital circuits that operate at over 10-MHz by using multithreshold voltage CMOS (MTCMOS) technology with both normal and low-threshold voltage transistors [2].

Furthermore, direct battery operation of the analog circuits by a single rechargeable cell or dry cell achieves low-noise power supply because of low impedance of the battery and a ripple-free stable dc power supply. Low-voltage analog circuit technologies have been reported only for amplifiers and filters [6], [7]. There are few reports of A/D converters operating with a supply voltage under 3 V. The lowest supply voltage reported for an A/D converter is 2.5 V [8]. Making an A/D converter for a 1 V supply is difficult because lowering the supply voltage causes two problems: One is the decreased speed and narrowed output range of the amplifiers, and the other is poor analog switching. Here, we introduce a swing-suppression noise shaping A/D conversion technique using an *RC* integrator suitable for 1 V operation [9]. We also discuss the principle of this technique and describe the performance of an A/D converter test chip. The chip was designed using 0.5 μm CMOS technology for the RF analog interface of a digital cordless phone baseband LSI.

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II. Problems of 1 V Battery Operation

Noise-shaping A/D converters using the switched-capacitor technique are widely used for the analog-digital interface in communications and audio LSI's because they provide high accuracy with low sensitivity to process fluctuation [10], [11]. However, the low voltage operation of A/D converters using the switched-capacitor technique has serious problems. With a 1-V power supply, accuracy diminishes for two reasons: poor amplifier performance and poor analog switching because of decreasing in V_{gs}-V_{th} voltage.

Amplifier speed and analog switch performances are both improved by lowering the threshold voltage (V_{th}) of transistors because this causes an increase in V_{gs}-Vth voltage. However, in the amplifier, a narrowing of the output range decreases the S/N ratio because the signal amplitude decreases but the noise which includes flicker and $1/f$ is not decreased. With the analog switch, the large subthreshold leakage current of the switch increases by a factor of 6 to 10 in V_{th} for 0.1 V decreases. This large leakage current degrades the accuracy of the switched capacitor circuit.

III. 1 V Power Supply Noise-Shaping A/D Conversion Technique

To solve the above mentioned low-power supply problems, we propose an *RC* integrator circuit and have developed a swing-suppression noise-shaping scheme.

A. RC Integrator

Fig. 1 is a block diagram of a basic noise-shaping A/D converter. It consists of an integrator, a quantizer and a feedback DAC. The component most sensitive to leakage current is the integrator.

Fig. 2(a) shows a switched-capacitor integrator circuit in which the input capacitor (C_i) converts the input analog voltage (V_i) into charges (Q_{ci}) which are given by $Q_{ci} = V_i \bullet C_i$, and this charge is integrated into the integration

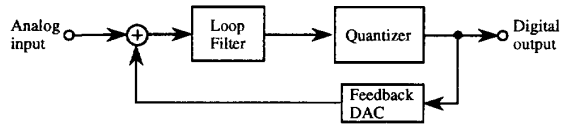
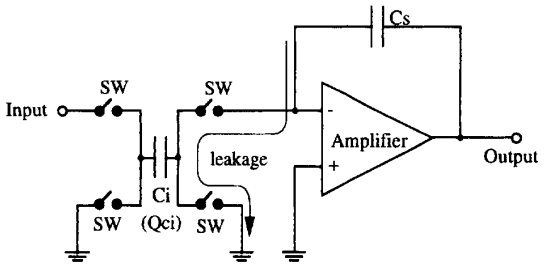
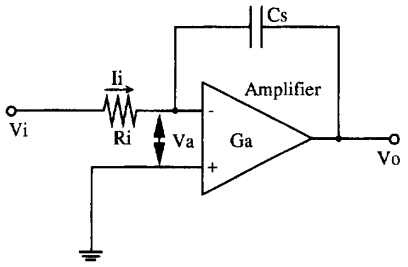


Fig. 1. Block diagram of a basic noise-shaping A/D converter.



(a) Switched-capacitor integrator



(b) RC integrator

Fig. 2. Integrator circuits. (a) Switched-capacitor integrator. (b) RC integrator.

capacitor (C_s) by the amplifier. However, the charge in an integration capacitor (C_i) leaks through the analog switch to GND, and this leakage decreases the S/N ratio of the A/D converter. Therefore, it is necessary to solve this current leakage problem to achieve high accuracy.

One effective solution is to use the *RC* (resistor and capacitor) integrator shown in Fig. 2(b). In this circuit, the input resistance (R_i) converts the input voltage (V_i) into the current (I_i) which are given by $I_i = V_i/R_i$, and the integration capacitance (C_s) integrates this current. In this configuration, no leakage occurs from the amplifier input nodes, which are most sensitive to leakage currents. I_i is not influenced by the leakage current because there is no analog switch, and thus, I_i is proportional only to V_i. This *RC* integrator appears quite suitable for use in a noise-shaping A/D converter with low V_{th} transistors.

B. Swing-Suppression Noise-Shaping Scheme

A large amplitude signal, which is the sum of the input signal and the quantization noise, is usually integrated into the integrator in the noise-shaping A/D converter. If the output

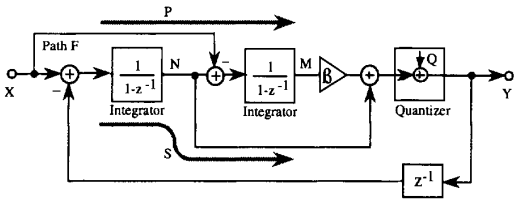


Fig. 3. Swing-suppression scheme.

range of the amplifier is narrowed by the low-voltage power supply, the signal amplitude has to be reduced. A scaling technique [12]–[15] has been presented for reducing this amplitude. This approach also reduces input signal amplitude. However, the circuit noise in the amplifier, which are flicker and $1/f$, are not reduced. Therefore, the S/N ratio is degraded. To reduce S/N ratio degradation due to a narrowing of the output range, we have developed a swing-suppression noise-shaping scheme.

This noise-shaping scheme is diagramed in Fig. 3. The feed-forward path (F) is added to the conventional feed-forward scheme [10]. The output Y of this scheme is given by

$$Y = X + \frac{(1 - z^{-1})^2}{1 - (1 - \beta)z^{-1}}Q. \tag{1}$$

The complete second-order noise-shaping characteristic is given by setting $\beta = 1$. The frequency response of the input signal is flat and is not influenced by β.

The signal (X) is eliminated by path F and does not flow to the second integrator. As a result, the signal flows through path (S), which includes only one integrator. Quantization noise flows through path (P), which includes two integrators. It is clear by (1) that the noise-shaping characteristic is continuously variable from first order to second order by the value range of β ($0 < \beta \leq 1$). Accordingly, this scheme becomes very stable by setting β to little smaller than 1.

Signal flows of the conventional second-order delta-sigma scheme using the scaling technique are shown in Fig. 4. The integrator outputs (N and M) of the delta-sigma scheme with $K1 = K2 = 1$ are given by,

$$N = X - z^{-1}(1 - z^{-1})Q, \tag{2}$$

and

$$M = X - z^{-1}Q - z^{-1}(1 - z^{-1})Q. \tag{3}$$

Furthermore, the integrator outputs (N and M) of the swing-suppression scheme when $\beta = 1$ are given by,

$$N = X - z^{-1}(1 - z^{-1})Q, \tag{4}$$

and

$$M = -z^{-1}Q. \tag{5}$$

By (2) to (5), the integrator output swings of the swing-suppression scheme are smaller than the second integrator output swing of the delta-sigma scheme. The simulated integrator output waveforms of these schemes, with $\beta = 1$, $K1 = K2 = 1$, and 2-bit DAC, are shown in Fig. 5. The

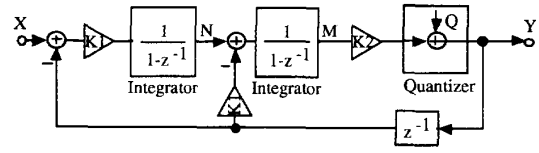


Fig. 4. Second-order delta-sigma scheme with scaling.

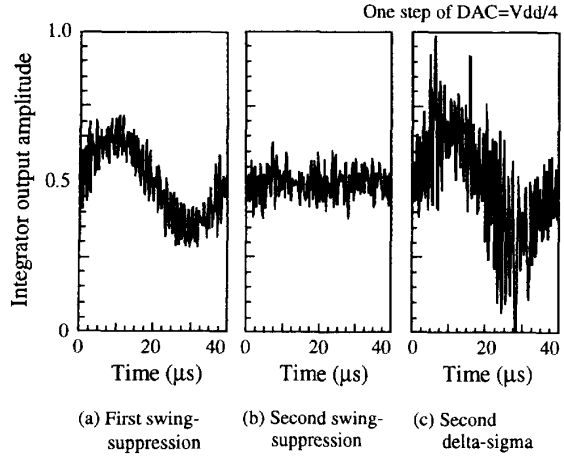


Fig. 5. Integrator output waveforms.

second integrator output swing of the delta-sigma scheme is twice as large as the first integrator output swing of the swing-suppression scheme for the same input signal. This means that the twice amplitude signal can be inputted into the swing-suppression scheme in comparison with the delta-sigma scheme using the same integrator output range. Furthermore, in the case of the low-voltage power supply A/D converter, circuit noise, such as flicker, $1/f$, and clock jitter, decreases the S/N ratio. This noise has no relation to the scheme and the width of the integrator output range. Therefore, the S/N ratio of the swing-suppression scheme is better than that of conventional schemes because signal amplitude is large.

If $K1$ and $K2$ in the delta-sigma scheme are set at 0.5 and 2.0, respectively, the integrator swing is reduced by half. Fig. 6 shows the signal flow of this case in respect to the amplifier circuit noise of Qa. The output Y of this flow is given by,

$$Y = X + K2 \bullet Qa + (1 - z^{-1})^2 Q \quad (K2 = 1/K1). \quad (6)$$

Using the scaling technique, signal amplitude is improved. However, circuit noise is increased by the scaling, and the S/N ratio is not improved. Therefore, the swing-suppression scheme has the advantage of achieving a high S/N ratio with a low-voltage power supply.

The other advantage of the swing-suppression scheme is a high immunity to integrator characteristic variation. The best way to eliminate current leakage problems is to use the *RC* integrator mentioned earlier. *RC* variation caused by manufacturing processes, however, has to be considered. Simulated S/N ratios as a function of *RC* variation are shown in Fig. 7 at the amplifier unity-gain bandwidth of 30 MHz and the β of 0.9. The variation of the S/N ratio is only 3 dB, given

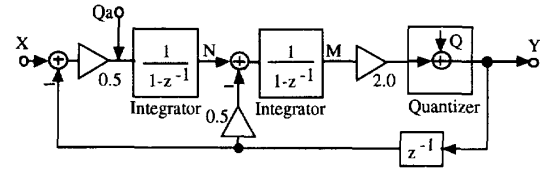


Fig. 6. Delta-sigma scheme in respect to the circuiit noise.

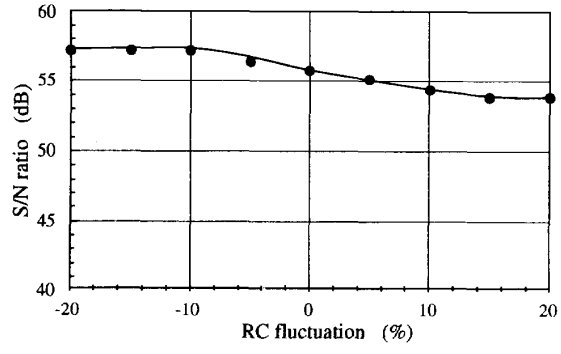


Fig. 7. Simulated S/N ratios versus *RC* fluctuation.

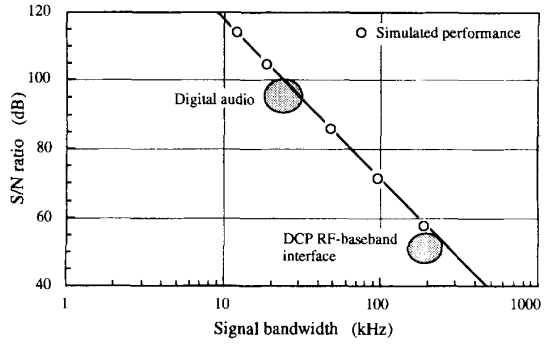


Fig. 8. Simulated S/N ratio.

RC variation of $\pm 20\%$. Thus, the swing-suppression scheme with an *RC* integrator is suitable for use with low-voltage power supply.

Simulated S/N ratios using the ideal integrator are shown in Fig. 8. These are for the sampling frequency of 6.144 MHz and the 2 bit quantizer. The S/N ratio is 60 dB in the digital cordless phone's interface bandwidth of 192 kHz, and 105 dB in the audio signal bandwidth of 20 kHz.

A high-order noise-shaping scheme above the second order is shown in Fig. 9. This can be easily implemented by using the swing-suppression scheme. First and second stage outputs ($Y1$, $Y2$) are given by,

$$Y1 = z^{-1}X + \frac{z^{-1}(1 - z^{-1})^2}{1 - (1 - \beta)z^{-1}} Q1, \quad (7)$$

and

$$Y2 = -\frac{z^{-1}(1 - z^{-1})^2}{1 - (1 - \beta)z^{-1}} Q1 + \frac{(1 - z^{-1})^4}{1 - (1 - \delta)z^{-1}} Q2. \quad (8)$$

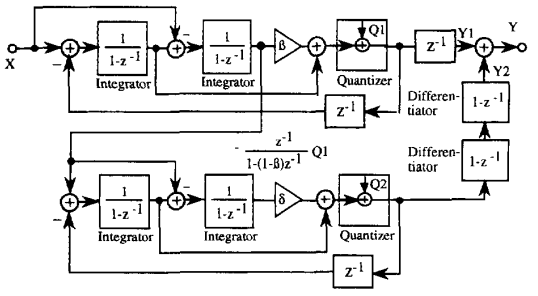


Fig. 9. Fourth-order cascade-connected swing-suppression scheme.

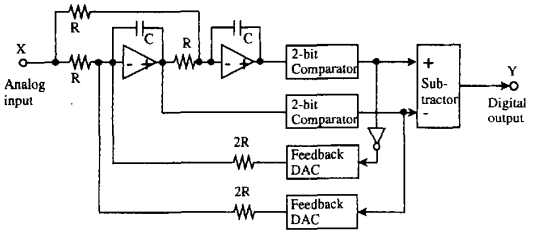


Fig. 10. Circuit blocks of the A/D converter.

The term of $Q1$ in $Y1$ is the same as that in $Y2$. A cascade connection is thus possible and first-stage quantization noise is completely negated by the second-stage output despite the value of β. Output Y for the scheme shown in Fig. 8 is,

$$Y = z^{-1}X + \frac{(1-z^{-1})^4}{1-(1-\delta)z^{-1}}Q2. \tag{9}$$

With a cascade scheme of swing-suppression, fourth-order noise-shaping characteristics are obtained.

IV. Design

To demonstrate the swing-suppression scheme, we designed a 1 V supply A/D converter for the RF interface of a digital cordless phone's baseband LSI. This requires a signal bandwidth of 192 kHz and a resolution of 8 bits [16]. This A/D converter was fabricated by 0.5 μm MT-CMOS process technology.

A. Swing-Suppression A/D Converter Circuit

The circuit blocks of the A/D converter based on the swing-suppression scheme, which is suitable for use with an *RC* integrator, are shown in Fig. 10. This circuit consists of two *RC* integrators, two 2 bit quantizers, two feedback DAC's and a digital subtractor. The sampling frequency is 6.144 Msps, which gives an oversampling ratio of 16. The feedback DAC is operated at 24.576 MHz.

The multibit quantizer and DAC provide one effective way to overcome the S/N degradation due to the circuit noise, because these increase the input signal amplitude by decreasing the quantization noise. A correction technique for the multibit feedback DAC is usually needed to achieve high accuracy [17]. However, the pulse width modulation (PWM) DAC does not need this because its accuracy is determined by clock accuracy and noise in the power line [18].

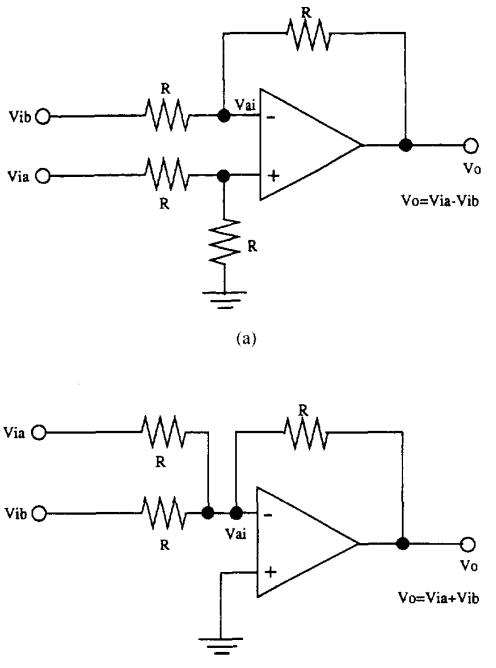


Fig. 11. Analog subtractor (a) and adder (b) circuits.

The signal flows of the swing-suppression scheme shown in Fig. 3 include the subtraction function. The input range (V_{ai}) of the differential amplifier in the analog subtractor shown in Fig. 11(a) is defined by,

$$V_{ai} = V_{dd} - V_{\mathrm{thn}} - V_{\mathrm{thp}} - V_{is}. \tag{10}$$

The conventional amplifier current source includes a current mirror circuit. The term, V_{is}, is the source-drain voltage of the current source. In this case, V_{is} is nearly equal to V_{thn}. If V_{thp} and V_{thn} are 0.3 V, V_{ai} is only 0.1 V. Therefore, the input range of the analog subtractor is very narrow and the analog subtractor is not used because the required range of V_{ai} is $V_{ia}/2$. However, the analog adder which uses the *RC* integration, shown in Fig. 11(b), does not require a wide input range to the amplifier because the required range of V_{ai} is only $(V_{ia}+V_{ib})/2G$ (G is the amplifier gain). Furthermore, the design of the differential multibit quantizer is difficult because it is difficult to make the differential standard voltage. Therefore, we remove the analog subtractor using the analog adder, two multibit quantizer, and the digital subtractor shown in Fig. 10. This relaxes the requirement for a wide input range of the amplifier.

The value of β is easily set by adjusting the ratio of the resistors between the first integrator and the feedback DAC. In this A/D converter circuit, the β of 0.5 is made by setting the feedback DAC resistor value to 2R. MT CMOS logic cells are used in the digital circuits for operation at an sampling frequency of over 6.144 MHz and on a 1 V power supply.

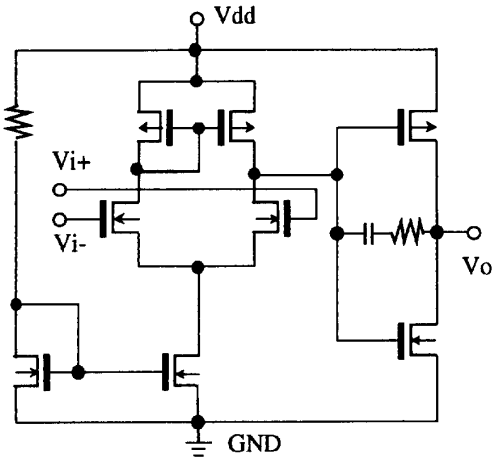


Fig. 12. Amplifier circuit.

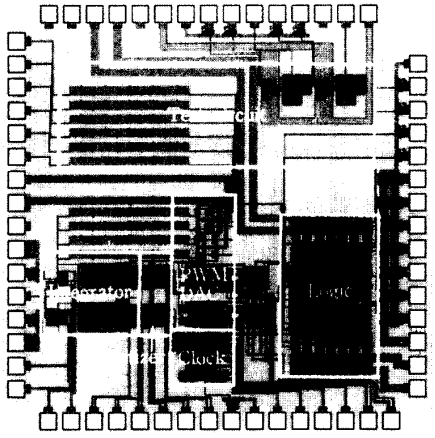


Fig. 13. Chip photomicrograph.

B. Amplifier

The main component circuits are the amplifier, the quantizer and the feedback DAC. Quantizer circuit noise is shaped and suppressed just as the quantization noise was. A highly accurate DAC is easily implemented by using the PWM method [18]. For the amplifier, however, wide bandwidth, wide output range, high gain, high linearity and low noise are required. The amplifier is, thus, both the most important circuit and the one most difficult to design.

Fig. 12 shows the amplifier circuit for the *RC* integrator. This is the simplest construction for the differential amplifier. To ensure a wide bandwidth, wide active range and high gain, this circuit uses low-$V_{\rm th}$ transistors and a simple push-pull output stage.

V. Results

An A/D converter was fabricated using 0.5 μm MT CMOS process technology. A photomicrograph of the converter is in Fig. 13. The chip's active area is 1.1 × 2.3 mm^2. It uses gate polysilicon resistors and metal-insulator-metal capacitors.

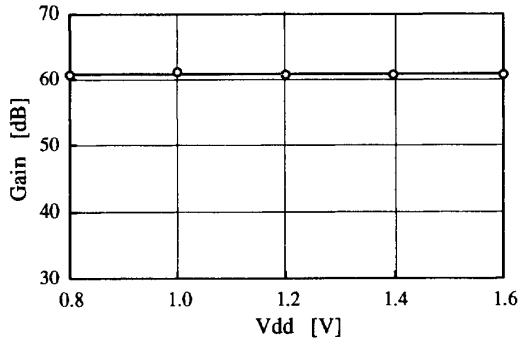


Fig. 14. Gain versus supply voltage.

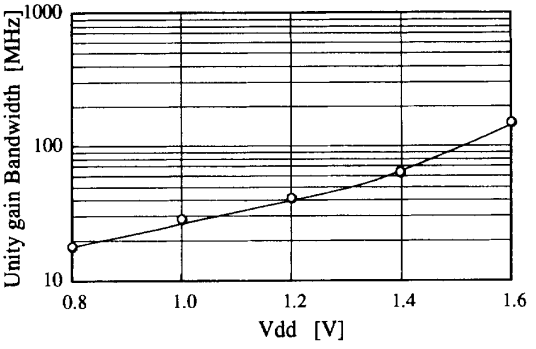


Fig. 15. Unity gain bandwidth versus supply voltage.

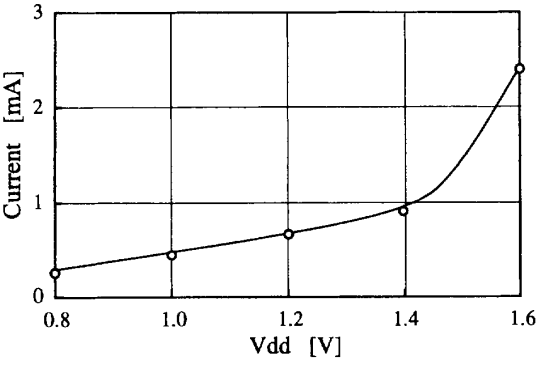


Fig. 16. Circuit currentversus supply voltage.

A. Amplifier Performance

Fig. 14 plots amplifier gain as a function of supply voltage. The low-$V_{\rm th}$ transistors resulted in a gain of 62 dB between 0.8 V and 1.6 V. The unity gain bandwidth is shown in Fig. 15 as a function of the supply voltage. At a 1 V supply, the bandwidth was 30 MHz. This bandwidth was for the sampling frequency of 6.144 Msps. Fig. 16 plots circuit current as a function of

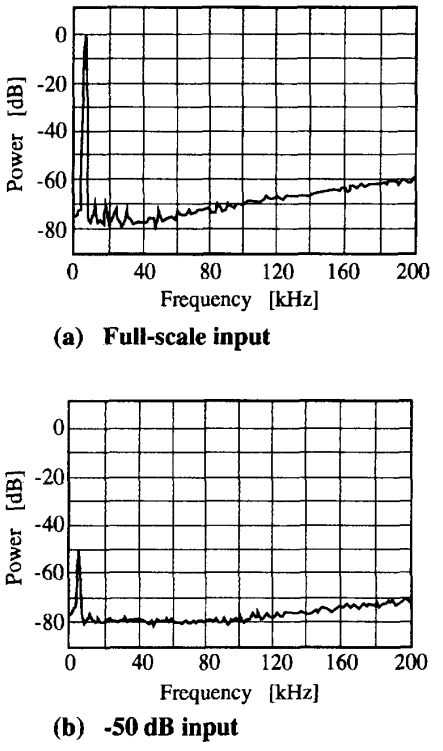


Fig. 17. Measured spectra. (a) Full-scale input. (b) -50 dB input.

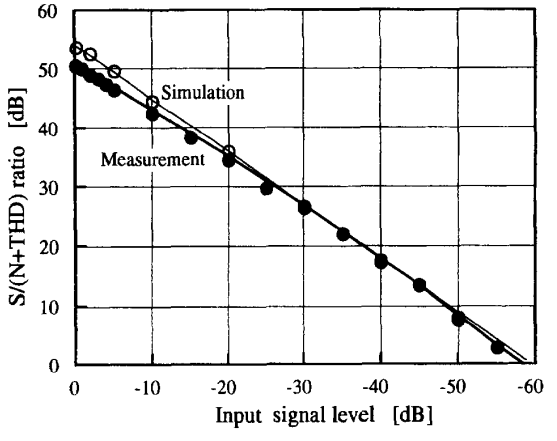


Fig. 18. S/N ratio versus input signal levels.

the supply voltage. The circuit current was proportional to V_{dd}^2. This is characteristic of the saturation region of the MOS transistor. With a 1 V supply, the current was 0.5 mA and power consumption was 0.5 mW.

B. A/D Converter Performance

Measured spectra of the A/D converter are shown in Fig. 17: (a) is for full-scale input, and (b) is for minus 50 decibel input. The noise floor in the low-frequency region was very low. The harmonic distortion was under minus 70 dB.

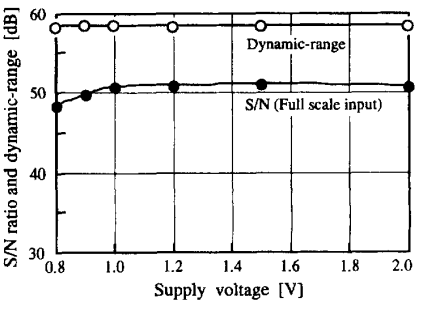


Fig. 19. S/N ratio and dynamic-range versus supply voltage.

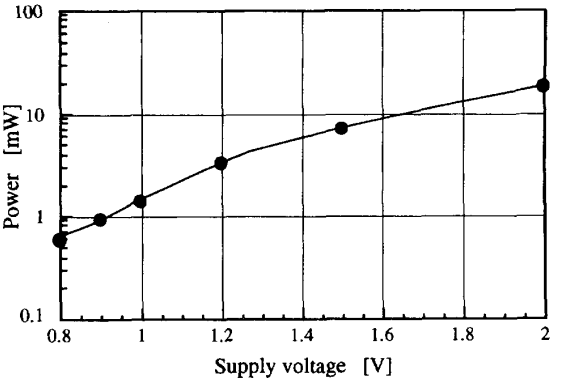


Fig. 20. Power consumption versus supply voltage.

The S/N ratios as a function of input level are shown in Fig. 18. With a 1 V power supply an accuracy of 10 bits was obtained at a low input level. An accuracy of 9 bits was obtained at the full-scale level. These characteristics are within 3 dB of the simulated characteristics.

The S/N ratios and dynamic-ranges as functions of the supply voltage are shown in Fig. 19. The S/N ratios and dynamic-ranges did not degrade in the range from 2 to 0.9 V. This outcome is suitable for battery discharge characteristics and it allows direct battery operation without a dc–dc converter.

Fig. 20 plots power consumption as a function of supply voltage. At 1 V, consumption is 1.56 mW. Power consumption versus sampling frequency is plotted in Fig. 21 for previously reported converters and for the swing-suppression A/D converter. The solid line shows the performance limits of the conventional technology. The power consumption of a swing-suppression A/D converter was only one-fifth that of the best converters using conventional technology. The performance of the proposed A/D converter (summarized in Table I) clearly demonstrated that A/D conversion with direct operation from a one-cell battery is possible.

VI. Conclusion

We have proposed a swing-suppression noise-shaping method for implementing an A/D converter that operates on a one-cell battery and consumes low power. Using this method, we developed an A/D converter for the analog interface of a digital cordless phone. This converter operates with a 1

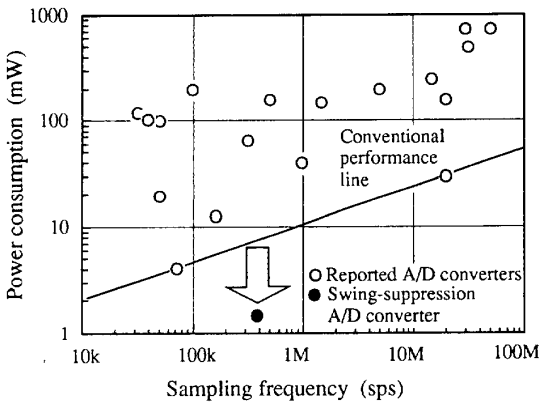


Fig. 21. Comparison of power consumption.

TABLE I
A/D CONVERTER PERFORMANCE

Resolution		10 bits
Signal bandwidth		192 kHz
Sampling frequency		6.14 Msps
Over-sampling rate		16
S/(N+THD)		51 dB
Dynamic-range		58 dB
Vdd	minimum	0.8 V
	maximum	2.0 V
Analog signal swing		0.4 Vpp
Power consumption		1.56 mW
Test chip active area		1.1 x 2.3 mm^2

V power supply and has a 10 bit dynamic-range, a signal bandwidth of 192 kHz and a power consumption of 1.56 mW.

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