Measurement of Digital Noise in Mixed-Signal Integrated Circuits

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Abstract— **This paper proposes a method of measuring the influence of digital noise on analog circuits using wide-band voltage comparators as noise detectors. Noise amplitude and rms voltage are successfully measured by this method. A test chip is fabricated to measure the digital noise influence. From the experimental results, it is shown that the digital noise influence can be considerably reduced by using a differential configuration in analog circuits for mixed-signal IC's. The digital noise influence can be further reduced by lowering the digital supply voltage. These results show that the voltage-comparator-based measuring method is effective in measuring the influence of digital noise on analog circuits.**

I. Introduction

RECENTLY, there has been an increasing need for mixed-signal integrated circuits (IC's) such as video signal processors [1]. Future multimedia applications require image processing circuits that can run at speeds over 100 MHz with gate-counts of over 100 kG (kilo-gates) on a single-chip. At the same time, an on-chip Analog to Digital converter is desired that has greater than 10-bit accuracy. In order to accommodate this high-performance nature of both analog and digital domains on a single-chip, it is of considerable importance to reduce the coupling of digital noise to analog circuits.

Noise problems in mixed-signal IC's have recently been discussed [2]. There are noise transmission paths both inside and outside the IC's. It is well known that if the power supply lines and the ground lines are connected separately to the digital and analog circuits, the coupling of switching noise is minimized. However, it is very difficult to reduce coupling via the substrate to an analog circuit by substrate noise produced by digital clock signal switching. Various ways of reducing the substrate noise, such as using guard-rings [2] or bonded-SOI wafers and trench process [3], are proposed. Furthermore, current-mode logic techniques for CMOS mixed-mode ASIC's are proposed for reducing the digital noise [4].

Though noise reduction techniques are important in IC fabrication, it is also important to understand the noise transmission mechanism in solving the noise problem in large scale ASIC's. Therefore, it is necessary to investigate the noise transmission path and to measure the amount of substrate noise. Switching noise in mixed-signal IC's has been measured with a single transistor amplifier [5]–[7]. Su *et al.* described several approaches to reducing substrate crosstalk and discussed the effect of reducing the bias inductance. However, the influence of digital noise on on-chip analog circuits, such as in an A/D converter, has not been addressed. The dependence on the number of digital circuits also needs to be better understood. In order to measure the influence of digital noise coupling through the substrate on analog circuits, a method of measuring digital noise using voltage comparators as noise detectors is proposed. In this voltage-comparator-based measuring method [8], a chopper type voltage comparator is used as a noise detector. Since a voltage comparator is used in an A/D converter, the actual influence of digital noise on on-chip analog circuits can be observed. Because the chopper type voltage comparator, which has a wide input bandwidth over 100 MHz, amplifies the difference between two input nodes and then outputs digital voltage, it is suitable for detecting high-speed digital noise and is not influenced by analog noise outside the circuit. As a result, statistical noise analysis with the voltage comparator has a high reliability.

In this work, the noise measuring method involving a voltage comparator is considered. The rms voltage and noise amplitude are successfully measured by analyzing the distribution of metastability in the comparator. A test chip for use in noise measurements is configured and was fabricated by 0.8 μm CMOS technology. In this test chip, the number of activated digital logic gates, the digital noise source, can be selected to measure the dependence of noise amount on the number of digital gates. Single-ended and differential comparators are configured as noise detectors in order to compare the influence of noise. The digital noise dependence on frequency and digital supply voltage was measured using the test chip.

In this paper, the voltage-comparator-based measuring method is described in Section II. Measurement accuracy, the rms voltage and amplitude for noise measurement obtained by computer simulation are shown in Section III. The test chip configuration and the experimental results are described in Sections IV and V.

II. Voltage Comparator Measuring Method

In the voltage comparator measuring method, the outputs are determined to be logic "high" or "low" depending on the relative level of the input voltage V_{in} with respect to the reference voltage V_{ref}. An example of a noise waveform input into the noise detector is illustrated in Fig. 1. Noise

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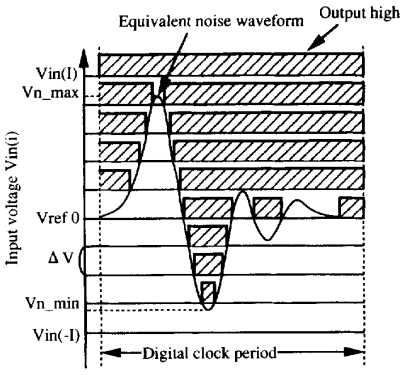


Fig. 1. An example of a noise waveform.

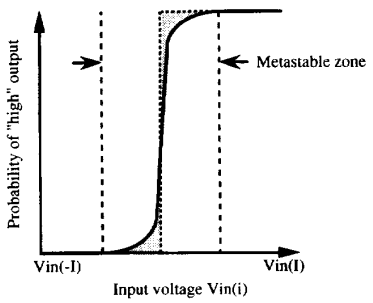


Fig. 2. Probability of "high" output.

is considered to occur at the rising and falling edge of the digital clock signal and to have voltage values from $V_{n\_\min}$ to $V_{n\_\max}$. The horizontal axis represents sampling points. The vertical axis, representing the input voltage, can be expressed by

$$V_{\text{in}}(i) = \Delta V \cdot i + V_{\text{ref}}. \qquad (i = -I, \ldots 0, \ldots I) \quad (1)$$

where ΔV is the change in input voltage. If there is no noise added to V_{ref}, the probability of a "high" output changes sharply from 0 to 1 at $V_{\text{in}} = V_{\text{ref}}$. In contrast, if noise is equivalently added to V_{ref}, the output shows high levels as in the shaded part of Fig. 1.

In the measurement, as the digital clock frequency does not synchronize with the comparator sampling frequency, the sampling point is randomly selected within the period of equivalent one digital clock signal. For statistical analysis, output levels for each given $V_{\text{in}}(i)$ have to be measured sufficiently many times (N) over a number of digital clock periods. It represents that the equivalent sampling rate is N times the one sequence of digital clock. Then, the probability of a "high" output can be calculated. This probability $P(i)$ at input voltage $V_{\text{in}}(i)$ is shown in Fig. 2. It can be expressed as

$$P(i) = \frac{1}{N} \sum_{n=1}^{N} q(n, i). \qquad (2)$$

Here, $q(n, i) = 1$ when $V_{\text{in}}(i) > V_{\text{ref}}$, and $q(n, i) = 0$ when $V_{\text{in}}(i) < V_{\text{ref}}$. Due to the noise, $P(i)$ changes gradually from 0 to 1, producing a metastable zone. Consequently, the percentage of metastability $p(i)$ at input voltage $V_{\text{in}}(i)$ is expressed as

$$p(i) = \frac{1}{N} \sum_{n=1}^{N} q(n, i) \quad (i < 0)$$
$$1 - \frac{1}{N} \sum_{n=1}^{N} q(n, i) \quad (i > 0). \qquad (3)$$

It is clear that the percentage of metastability $p(i)$ is high around $V_{\text{in}} = V_{\text{ref}}$. In Fig. 2, the shaded part represents the noise power, N_p which can be calculated using $p(i)$:

$$N_p = \sum_{i=-I}^{-1} (V_{\text{in}}(i) - V_{\text{m}})^2 \{p(i) - p(i-1)\} + \sum_{i=1}^{I} (V_{\text{in}}(i) - V_{\text{m}})^2 \{p(i) - p(i+1)\} + (V_{\text{in}}(-I) - V_{\text{m}})^2 p(-I) + (V_{\text{in}}(I) - V_{\text{m}})^2 p(I). \quad (4)$$

Here, V_{m} is the mean value of noise. From the percentage of metastability $p(i)$, the probability of metastability $p2(i)$ can be calculated by normalizing the percentage of metastability by integrating it from $-I$ to I. This is represented as

$$p2(i) = p(i) / \sum_{i=-I}^{I} i \cdot p(i). \qquad (5)$$

Since the probability of metastability $p2(i)$ represents the stochastic nature of the noise, the noise amplitude can be determined from the probability distribution of metastability. Here the standard deviation σ can be expressed as:

$$\sigma = \Delta V \cdot \sqrt{\sum_{i=-I}^{I} i^2 \cdot p2(i)}. \qquad (6)$$

In our measurements, the value 3σ in the distribution is determined to be the noise amplitude.

III. Computer Simulation

A. Measurement Accuracy

In this comparator based measuring method, the digital noise influence has been observed statistically, as shown in the above section. The value of ΔV and the error in ΔV determine the measurement accuracy, since V_{in} is determined by (1). In order to evaluate this method, these factors are simulated by computer. In this simulation, measurement accuracy is discussed in terms of the error in rms voltage. The error in rms voltage is calculated as the ratio of the root mean square value of N_p shown in (4) to the rms voltage calculated from the time record data.

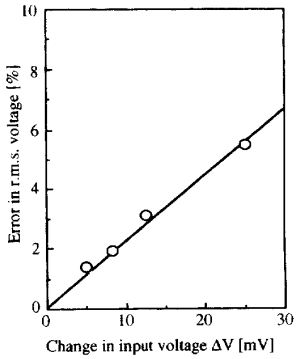


Fig. 3. Error in rms voltage dependence on ΔV.

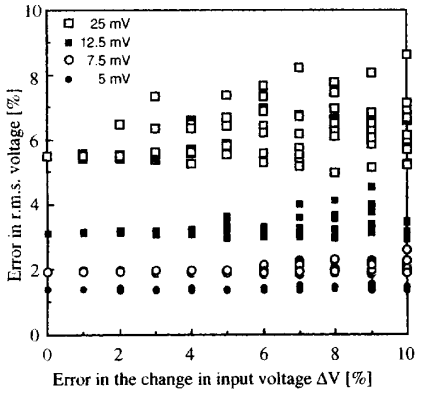
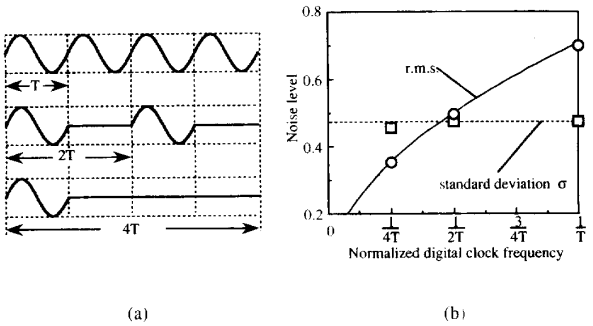


Fig. 4. Error in rms voltage dependence on error in ΔV.



(a) (b)

Fig. 5. Simulation results for standard deviation and rms voltage. (a) Simulated noise waveforms. (b) Simulated noise voltage.

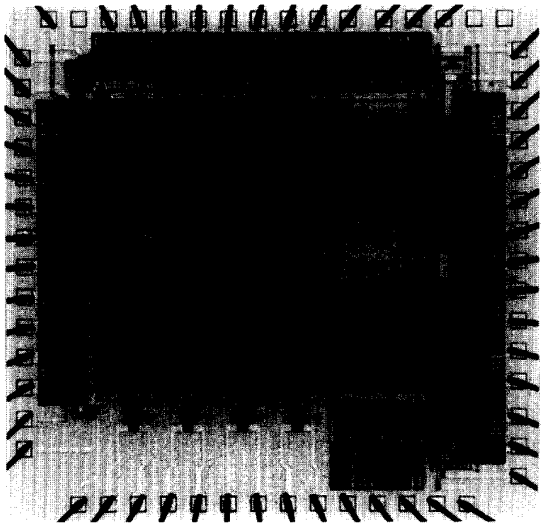


Fig. 6. Photograph of the test chip used to measure digital noise.

The dependence of the error in rms voltage on ΔV is shown in Fig. 3. In this simulation, the noise amplitude is assumed to be 1 V and the noise is sinusoidal. The error in rms voltage increases with increases in ΔV. If ΔV is smaller than 50 mV, it can be measured within 10 percent accuracy.

The error in ΔV dependency is shown in Fig. 4. If ΔV becomes small, the error in rms voltage becomes small. This means that the error in ΔV does not have much affect on measurement accuracy when ΔV is small enough.

This shows that the change in input voltage ΔV determines the measurement accuracy.

B. Noise Characteristics

The next simulation involves the use of rms voltage and standard deviation in noise estimation. Noise is considered to occur at the rising and falling edge of the digital clock signal. Therefore, the noise waveform is considered to depend on the rising speed of the digital clock, not on the digital clock frequency. In order to prove this assumption, three kinds of noise waveforms are used to evaluate the rms voltage and standard deviation. The simulated noise waveforms are shown in Fig. 5(a). These waves have the same amplitude, but different periods. If a wave has a long period it means that the digital clock frequency is low. The simulated noise voltage is shown in Fig. 5(b). According to these results, rms power (circles) changes in inverse proportion to the duration of the noise, while the standard deviation (squares), which represents the amplitude, is constant. This shows that rms power and amplitude of noise can be measured by this comparator based measuring method and that these two values are effective in estimating the characteristics of the rising and falling edge noise. Unlike conventional methods, the voltage-comparator-based measuring method estimates the noise from either the amplitude or rms power. This method can be applied to any circuit configurations or circuit applications.

IV. Design of Experimental Chip

In order to measure the influence of noise using our voltage-comparator-based measuring method, a test chip was fabricated. A die photograph of the test chip is shown in Fig. 6. It was fabricated by 0.8 μm CMOS technology and is 3.6 mm $\times$ 3.6 mm. Because our primary interest is the coupling through

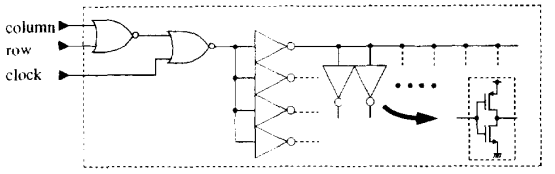
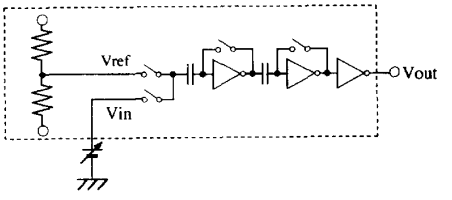
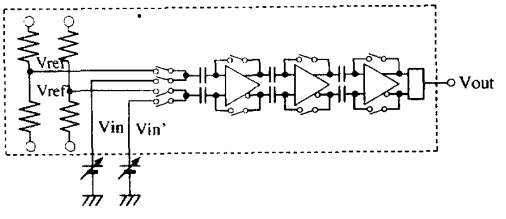


Fig. 7. Implementation of the noise source.



(a)



(b)

Fig. 8. Implementation of the noise detectors. (a) Single-ended implementation. (b) Differential implementation.

TABLE I
SIMULATED NOISE DETECTOR CHARACTERISTICS

	Single-ended	Differential
Resolution	< 0.2 mV	< 0.5 mV
Input bandwidth	> 200 MHz	> 200 MHz

TABLE II
TYPICAL MEASUREMENT CONDITIONS

Digital clock frequency	1 MHz
Sampling frequency	10 MHz
Digital supply voltage	3.3 V
Analog supply voltage	3.3 V
Change in input voltage	0.5 mV
Number of sampling points	1024

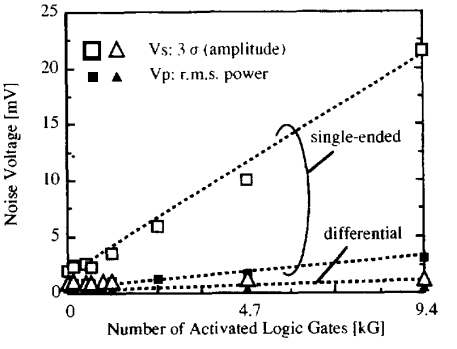


Fig. 9. Measured noise dependence on the number of activated logic gates.

the substrate, the supply voltage is connected separately to the digital and analog circuits to minimize the coupling of switching noise through the power supply lines. The noise source implementation is shown in Fig. 7. It comprises CMOS digital logic gates (inverter) consisting of 80 blocks (8 rows, 10 columns). Each block can be activated by selecting a row and column as a unit. Each group of inverters is connected in-parallel to minimize noise cancellation between the inverters. There are 9.4 k equivalent gates.

Both single-ended and differential comparators are implemented as noise detectors as shown in Fig. 8. As the resistors are made inside the well region of the test chip and the well region is connected to the external stable voltage, the noise capacitively coupled through the substrate to the resistors can be minimized. Both the reference and the input voltages are supplied externally on a basis of pure ground, so these voltages are stable to the substrate noise. Then the measured noise can be considered to be perfectly detected all in the comparator. Both single-ended and differential comparators were integrated in-parallel to facilitate comparison between the two implementations. The simulated noise detector characteristics are shown in Table I. The resolution is calculated from the gain of the comparators and the bandwidth is calculated from the bandwidth of the comparator input circuits. Because the comparator samples the input signals and outputs the compared result, the bandwidth of the input circuits determines the bandwidth of the noise measurement. Both single-ended and differential comparators have wide bandwidths over 100 MHz and high resolutions of 0.5 mV, so they are considered to have sufficient gain and bandwidth to detect noise.

The typical measurement conditions are shown in Table II. The frequency of the digital clock, which activates the noise source, is 1 MHz. It can be changed according to the aim of the measurement. The comparator sampling frequency is 10 MHz. The digital and analog supply voltages are 3.3 V. The change in the input voltage (ΔV) is 0.5 mV, since the resolution of the comparators is 0.5 mV. In this case, if the noise amplitude is assumed to be 10 mV, the rms voltage can be measured within 10% accuracy as confirmed by simulation. There were 1024 sampling points. When the digital clock frequency is 1 MHz, the equivalent noise sampling frequency is 1 GHz.

V. EXPERIMENTAL RESULTS

The measured noise dependence on the number of digital logic gates is shown in Fig. 9. It is clear that both rms power (V_p) and the 3σ value (V_s) increase in proportion to

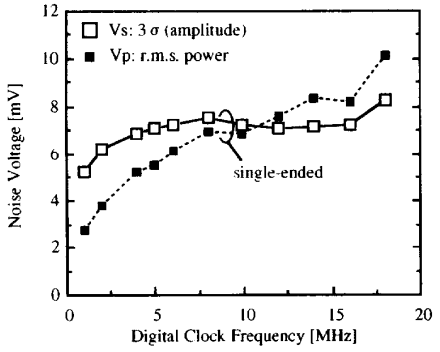


Fig. 10. Measured noise dependence on digital clock frequency.

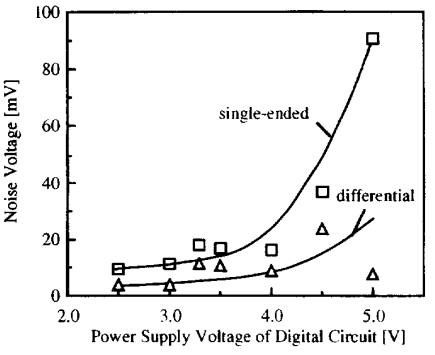


Fig. 11. Measured noise dependence on digital power supply voltage.

the number of digital logic gates in a single-ended comparator. This shows that the digital noise influence can be observed by the voltage-comparator-based measuring method. In the differential configuration, the change in input voltage of 0.5 mV is not small enough for accurate measurement. However, the measured results show that the digital noise is considerably reduced in the differential comparator and the measured noise is roughly 1/10 the value of the single-ended version.

This observation also shows that the rms voltage is smaller than the 3σ value in the probability distribution, which indicates that the noise is produced at the rising and falling edge of the digital clock signals. To confirm this, the dependence of digital noise on the digital clock frequency was measured with a single-ended comparator. In this measurement, the comparator sampling frequency is 10 MHz. As is shown in Fig. 10, rms power increases with increasing frequency, while the standard deviation is almost constant. This observation shows that the noise produced in a given period increases its power with higher digital clock frequencies, as was shown by computer simulation in Fig. 5. This observation also suggests that the noise produced at the rising and falling edge of the digital clock is transferred to and influences the analog circuits.

The measured dependence of noise on the digital power supply voltage is shown in Fig. 11. In this measurement, the analog supply voltage is set at 3.3 V to keep the sensitivity of the noise detector the same. In the single-ended comparators, the digital noise clearly decreases with decreasing supply voltage. The same effect is also observed for the differential detectors. This observation shows that decreasing the power supply voltage of digital circuits is effective in fabricating high-reliability mixed-signal IC's.

VI. Conclusion

In fabricating mixed-signal IC's, reducing the digital noise influence on analog circuits is important to obtain high reliability. For this purpose, a method of measuring digital noise in mixed-mode IC's using voltage comparators as noise detectors is proposed. Using this method, the actual influence of digital noise on on-chip analog circuits can be measured and the rms voltage and amplitude of noise can be analyzed statistically.

A test chip was fabricated to measure the influence of digital noise. A noise source consisting of CMOS inverter logic gates, as well as a voltage comparator to measure the digital noise influence were fabricated on the same substrate.

From the experimental results, it was shown that the effect of digital noise can be reduced considerably by using a differential configuration for analog circuits for mixed-signal IC's. The digital noise influence can be further reduced by lowering the digital supply voltage. These results show that the voltage-comparator-based measuring method is effective in measuring the influence of digital noise on analog circuits. This knowledge can be applied in designing low noise, high-reliability analog and digital mixed-signal IC's. The proposed method will be applied to measure the noise performance of different types of digital circuits and to compare the noise characteristics. It becomes important to estimate the noise before fabricating mixed-signal IC's. For this purpose, this method would be coupled with the substrate noise coupling simulation tools [9].

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