A High Temperature Precision Amplifier

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Abstract—**A precision operational amplifier has been developed for instrumentation applications in which the circuitry must operate in ambient temperatures as high as 200°C. At 200°C the amplifier maintains an input offset voltage and current of less than 200 μV and 1 nA respectively, a gain bandwidth product of 2.2 MHz, and a slew rate of 5.4 V/μS. The amplifier is fabricated in a standard CMOS process and consumes 5.5 mW of power at a supply voltage of 5 V. A continuous time auto-zeroed amplifier topology is used to achieve the low offset voltage levels. At high temperatures the leakage currents of the sample and hold switches used to achieve auto-zeroing degrade the offset correction voltages stored on the hold capacitors. This degradation is reduced by using large external hold capacitors and by minimizing the diffusion area of the switches through the use of a doughnut shaped layout. The effect of the voltage degradation is reduced by sensing the offset correction voltage with a low sensitivity differential auxiliary input stage. A new input switch topology is used to reduce the amplifier's input offset current at high temperatures.**

I. Introduction

PRECISION high-temperature amplifiers are a basic building block for instrumentation systems which must operate in hot environments. The range of applications is diverse, including instrumentation used in automotive engine monitoring, industrial process control, and oil and gas well testing. A good example which demonstrates the requirements for a high-temperature amplifier is the measurement of pressure in oil and gas well testing applications. The great well depth (which can exceed 5000 m) coupled with the very small output signal levels (a strain gauge pressure transducer typically has a 30 mV full scale output signal) requires that signal processing/conditioning circuitry be used *in situ* with the pressure transducer in order to preserve the signal integrity. This requires that the precision amplifier have the usual characteristics of high dc gain, low noise, and low input offset voltage and current while operating at the high ambient temperatures found in a deep well (which may exceed 200°C [1]).

This paper describes the development of a precision amplifier capable of operating at temperatures up to 200°C. The amplifier is fabricated in a standard 5 V 1.2 μm CMOS process to allow for the inclusion of additional digital/analog circuitry required to create a monolithic instrumentation system. Such a system should reduce size and cost while increasing performance and reliability compared to the hybrid systems currently used for most high temperature instrumentation.

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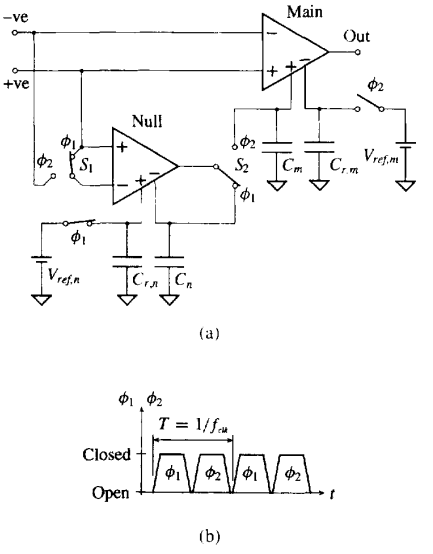

Fig. 1. Auto-zeroed amplifier. (a) block diagram, (b) clock timing.

The amplifier uses an auto-zeroed topology [2]–[4]. Any variation in offset voltage due to temperature change or aging is quickly sensed and reduced. Other benefits of auto-zeroed amplifiers include high dc gain, low $1/f$ noise, and high CMRR and PSRR. A new input switch topology is used to lower the input offset current at high temperatures.

A brief review of the operation of an auto-zeroed amplifier is given in Section II. The influence of leakage currents on circuit performance is discussed in Section III along with the design of the input switches, the sample and hold circuitry, and the internal amplifiers. Measurements of amplifier performance for the 20–200°C range are presented in Section IV.

II. Principles of Operation

An auto-zeroed amplifier periodically measures and reduces its offset voltage. The complexity of the auto-zeroed amplifier is determined by whether it processes signals in discrete or continuous time.

For discrete time applications, such as switched capacitor filters, only a single internal amplifier is required [3]–[5]. One phase of the clock is used to sense and reduce the offset while the other phase is used to process the signal. Continuous time operation requires two internal amplifiers [2], [6], [7] as shown in Fig. 1(a). The main amplifier is unswitched and continuously amplifies the input signal. On alternate clock phases the nulling amplifier disconnects from the signal path and zeros

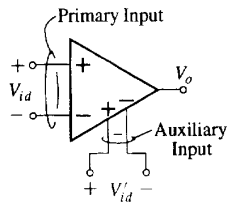

Fig. 2. Internal amplifier.

itself and then reconnects to the main amplifier to zero it. During the times when an amplifier is not being actively zeroed its differential offset correction signal is maintained by storing the correction voltages on capacitors. This paper focuses on continuous time auto-zeroed amplifiers. The determination of the effective offset of discrete time auto-zeroed amplifiers has been extensively reported in the literature [3]–[5]. This is not the case for continuous-time auto-zeroed amplifiers. Following a similar approach to that in [4] we extend Coln's work [2] to include unequal primary and auxiliary path gains, a differential auxiliary input, and the perturbation error of the hold capacitor voltages due to switching effects.

A. Internal Amplifier Model

Each internal amplifier (i.e., the main and nulling amplifiers) requires an auxiliary input through which the offset correction signal is applied. The output voltage of an internal amplifier (Fig. 2) can be expressed as

$$V_o(s) = (V_{\rm id} + V'_{\rm id}/\alpha + V_{\rm os})A(s), \tag{1}$$

where $V_{\rm id}$ and $V'_{\rm id}$ are the differential input voltages of the primary and auxiliary inputs, respectively, and $V_{\rm os}$ is the amplifier's offset voltage referred to its primary input. Throughout this paper a "$'$" is used to denote parameters belonging to the auxiliary input, whereas the subscript modifiers "m" and "n" denote parameters belonging to the main and nulling amplifiers, respectively. The internal amplifiers are designed to be dominant pole, therefore the gain from the internal amplifier's primary input to its output ($A(s) = V_o/V_{\rm id}$) can be modeled as

$$A(s) = \frac{A_o}{(1 + s/w_d)(1 + s/w_h)}, \tag{2}$$

where A_o is the dc open loop gain, w_d is the dominant pole, and w_h is a high frequency pole ($w_h > A_o w_d$). The auxiliary input will usually have the same poles as the primary input but will have a different open loop dc gain A'_o. This assumption is valid for implementations where the auxiliary and primary input signals are combined within the internal amplifier's first stage. If the ratio of the open loop dc gains between the primary and auxiliary inputs is defined as

$$\alpha = \frac{A_o}{A'_o}, \tag{3}$$

the open loop gain from the internal amplifier's auxiliary input to its output will be $A'(s) = A(s)/\alpha$. It will be shown that a large α desensitizes the auxiliary input to noise, charge injection, and switch leakage and improves frequency stability.

B. Effective Offset

The offset reduction cycle is now described in more detail. The timing of the clock controlling the amplifier's internal switches is shown in Fig. 1(b).

During ϕ_1, switch S_1 disconnects the inverting input of the nulling amplifier from the signal path and connects it to the non-inverting input thereby allowing the nulling amplifier to sense its own inherent offset voltage. Concurrently, switch S_2 connects the nulling amplifier's output back to its own inverting auxiliary input. By the end of ϕ_1, the negative feedback will force the nulling amplifier's output to

$$\frac{A_{\rm on}V_{{\rm os},n} + A'_{\rm on}V_{{\rm ref},n}}{1 + A'_{\rm on}}. \tag{4}$$

When the switch S_2 disconnects from C_n, charge injection (ΔQ), sampled noise (kT/C), and leakage current (I_L) all perturb the voltage stored on the capacitor by an amount

$$\Delta V_{C_n} = \left(\Delta Q + \sqrt{kTC_n} + I_L t\right)/C_n. \tag{5}$$

A similar voltage perturbation occurs on the hold capacitor connected to the reference voltage $V_{{\rm ref},n}$.

When ϕ_2 goes high, switch S_1 connects the inverting input of the nulling amplifier back into the signal path and switch S_2 connects the nulling amplifier's output to the auxiliary input of the main amplifier. The hold capacitors C_n and $C_{r,n}$ maintain the differential offset correction voltage on the nulling amplifier's auxiliary input during ϕ_2. As a result, the effective offset, during ϕ_2, of the nulling amplifier is

$$\frac{V_{{\rm os},n}}{A'_{\rm on}} - \frac{\Delta V_{C_n} - \Delta V_{C_{r,n}}}{\alpha_n} + \frac{V_{{\rm ref},n}}{A_{\rm on}}. \tag{6}$$

An auto-zeroed amplifier *must* operate with external feedback. During ϕ_2 the feedback allows the nulling amplifier (which now has a greatly reduced effective offset) to sense the inherent offset of the main amplifier and to generate the correction signal required to reduce it. The effective offset of the overall amplifier during ϕ_2 is

$$V_{\rm os} \simeq \frac{V_{{\rm os},m}(\alpha_m/\alpha_n) + V_{{\rm os},n}}{A'_{\rm on}} - \frac{\Delta V_{C_n} - \Delta V_{C_{r,n}}}{\alpha_n} + \frac{V_{{\rm ref},n} - V_{{\rm ref},n}}{A_{\rm on}}. \tag{7}$$

At the end of ϕ_2, switch S_2 opens and a perturbed version of the main amplifier's differential correction voltage is stored by C_m and $C_{r,m}$. As a result of the perturbation, the effective offset during ϕ_1 is

$$V_{\rm os} \simeq \frac{V_{{\rm os},m}(\alpha_m/\alpha_n) + V_{{\rm os},n}}{A'_{\rm on}} - \frac{\Delta V_{C_n} - \Delta V_{C_{r,n}}}{\alpha_n} + \frac{\Delta V_{C_m} - \Delta V_{C_{r,m}}}{\alpha_m} + \frac{V_{{\rm ref},n} - V_{{\rm ref},m}}{A_{\rm on}}. \tag{8}$$

The last term in both (7) and (8) can be eliminated by setting the reference points for the auxiliary input of both the null and main amplifiers to the same level. The worst case offset is then

$$V_{\rm os}^{\rm max} \simeq \frac{V_{{\rm os},n}^{\rm max}(\alpha_m/\alpha_n) + V_{{\rm os},n}^{\rm max}}{A'_{\rm on}} + \frac{\Delta V_{{\rm aux},n}}{\alpha_n} + \frac{\Delta V_{{\rm aux},m}}{\alpha_m}, \tag{9}$$

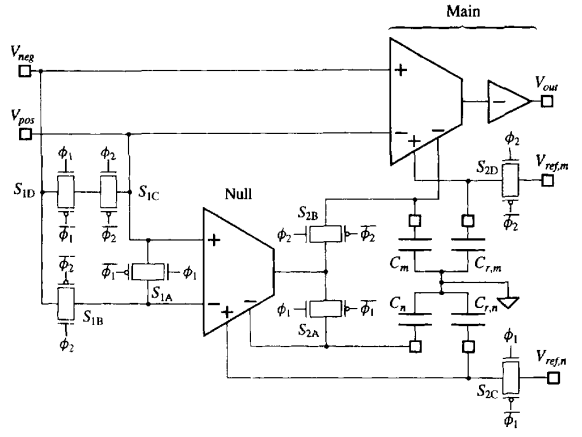

Fig. 3. Complete auto-zeroed amplifier. Capacitors C_n, C_m, $C_{r,n}$, and $C_{r,m}$ are external.

where $\Delta V_{\text{aux},m(n)}$ is the magnitude of the maximum perturbation in the differential correction voltage ($\Delta V_{C_{m(n)}} - \Delta V_{C_{r,m(n)}}$), and $V_{\text{os},m(n)}^{\max}$ the magnitude of the maximum inherent offset voltage. The optimal choice for α_m and α_n can then be determined from (9) by first letting $a = \alpha_m/\alpha_n$ and then solving simultaneously the equations

$$\frac{dV_{\text{os}}^{\max}}{d\alpha_n} = \frac{aV_{\text{os},m}^{\max} + V_{\text{os},n}^{\max}}{A_{\text{on}}} - \frac{\Delta V_{\text{aux},n}}{\alpha_n^2} - \frac{\Delta V_{\text{aux},m}}{a\alpha_n^2} = 0 \quad (10)$$

$$\frac{dV_{\text{os}}^{\max}}{da} = \frac{aV_{\text{os},m}^{\max}}{A_{\text{on}}} - \frac{\Delta V_{\text{aux},m}}{a\alpha_n^2} = 0. \quad (11)$$

The effective offset will be minimized if

$$\frac{\alpha_m}{\alpha_n} = \sqrt{\frac{\Delta V_{\text{aux},m} V_{\text{os},n}^{\max}}{\Delta V_{\text{aux},n} V_{\text{os},m}^{\max}}}, \quad (12)$$

and

$$\alpha_n = \sqrt{\frac{A_{\text{on}} \Delta V_{\text{aux},n}}{V_{\text{os},n}^{\max}}}. \quad (13)$$

III. Implementation

High temperature design considerations can be broken down into two broad areas: devices and circuit topology. The device behavior has been covered extensively elsewhere [8]–[12]. We will focus primarily on topology. High temperature operation affects the design of the auto-zeroed amplifier's input switches, the sample and hold switches, choice of hold capacitor size, and bias current levels. The complete auto-zeroed amplifier is shown in Fig. 3.

Leakage currents affect almost all high temperature design issues. Each MOSFET's source/drain diffusion forms a reverse biased pn junction with the substrate or well in which it is fabricated. At room temperature the leakage current of a moderately sized source/drain diffusion is on the order of picoamperes or less and usually has no significant effect on circuit operation. For low to moderate temperatures the reverse bias leakage current is dominated by generation-recombination

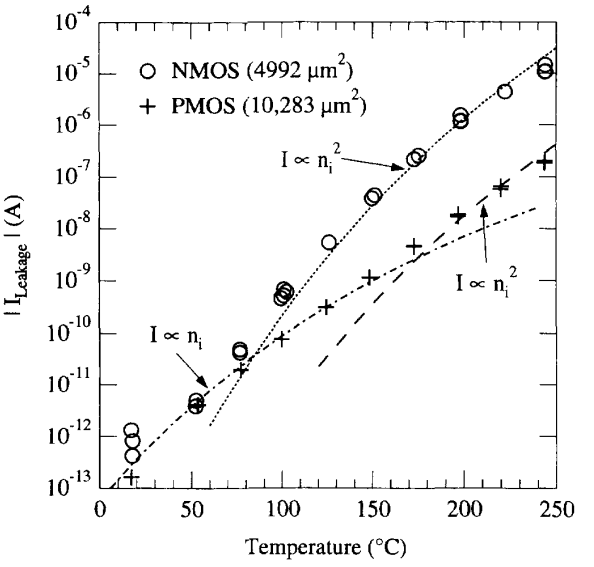

Fig. 4. Source/drain diffusion leakage currents of large MOSFET's fabricated in a n-well 1.2 μm CMOS process. The source/drain diffusion areas are given in parentheses for each device. The circles and cross markers represent measured currents (for multiple devices) while the solid and dashed lines are fitted characteristics showing the dependence of the leakage current on n_i and n_i^2.

mechanisms and increases with temperature at a rate proportional to n_i, the intrinsic carrier concentration of the semiconductor. The intrinsic concentration has a strong dependence on temperature [11]

$$n_i = 7.785 \times 10^{15} T^{3/2} \exp(-E_g/2kT) \quad (14)$$

where the temperature T is in degrees Kelvin and

$$E_g = 1.170 - \frac{4.73 \times 10^{-4} T^2}{T + 636}. \quad (15)$$

At high temperatures the leakage current is determined primarily by diffusion mechanisms and increases more rapidly at a rate proportional to n_i^2.

Fig. 4 shows leakage current measurements for very large N and P MOSFET's fabricated in the same n-well process that was used for the amplifier. The phenomenon of leakage current suppression described in [12] is clearly visible. At 200°C the leakage current (per unit area) of the NMOS transistor which is fabricated directly in the substrate is over a 100 times greater than that of the PMOS device fabricated in the n-well.

Leakage current suppression largely eliminates any possibility of reducing the net leakage current at a circuit node by compensating the leakage of a diffusion of one polarity with that of a diffusion of the opposite polarity. At high temperatures, the primary source of leakage currents in an n-well technology will be the source/drain diffusions of the NMOS transistors. For the process used, a near minimum dimensioned NMOS transistor (diffusion area of 3 μm $\times$ 6.3 μm) will leak approximately 5–10 nA at 200°C.

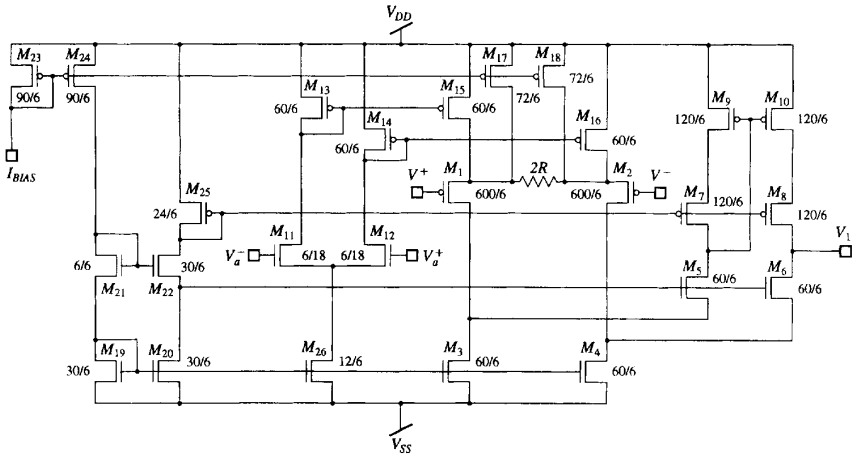

Fig. 5. Input stage.The primary and auxiliary input differential pairs are M_1, M_2 and M_{11}, M_{12}, respectively. All device sizes are in μm.

A. Input Switches

A new topology is used for the amplifier's input switches (Fig. 3) which minimizes the input offset current at high temperatures. Traditionally, only switches S_{1A} and S_{1B} are used. The amount of source/drain diffusion area exposed to each of the amplifier's input terminals changes with clock phase. This leads to a time-varying input leakage current component which becomes significant at high temperatures. A matched pair of dummy switches S_{1C} and S_{1D}, which are driven in opposite phase to S_{1A} and S_{1B}, respectively, are added to reduce the leakage current's time-varying input component. With perfectly matched switches, the diffusion area exposed to each input terminal is constant.The new input switch topology reduces the input offset current at the expense of increased input leakage (which approximately doubles). In typical instrumentation applications the amplifier interfaces to a bridge transducer which presents a balanced source impedance to the amplifier. In such uses, the input offset current is more important than the input bias current. The source impedance of a bridge transducer may be as large as 10 kΩ. Therefore, the 10 nA (or greater) input offset current at 200°C which is expected for the traditional input switch topology would contribute an error equivalent to a 100 μV offset voltage. Input offset current minimization is therefore critical to the successful use of an auto-zeroed amplifier at high temperatures.

B. Sample and Hold

Each internal amplifier has its offset actively zeroed during one half of a clock cycle. To maintain a low effective offset, the differential offset correction signal must be stored on hold capacitors for the remaining half period without substantial degradation.

At high temperatures the primary source of hold capacitor voltage degradation is the sampling switch leakage current. The degradation can be reduced by increasing the clock frequency, increasing the capacitor size, and reducing the leakage currents. The maximum clock rate is limited by second order effects such as the settling time requirements of the nulling amplifier and input switch charge injection. Capacitor size is limited by the availability of high quality capacitors rated for operation at 200°C. In our design, external 100 nF hold capacitors are used. Although the use of large external hold capacitors prevents the implementation of a truly monolithic amplifier, the level of leakage currents present at 200°C prevents the use of on-chip capacitors (which are limited to a maximum of approximately 100 pF). Most commercial auto-zeroed amplifiers use external hold capacitors in the range of 100–1000 nF. With large hold capacitors, the perturbation of the capacitor's voltage in (5) due to switch charge injection and kT/C noise is insignificant and can be neglected.

The switch leakage is minimized by using a doughnut shaped layout for the MOSFET's. The centre diffusion of the doughnut is connected to the hold capacitor while the outer diffusion is connected to the nulling amplifier's output (or the reference voltage source in case of the reference hold capacitors). The centre diffusion area is the minimum size allowed by the technology thereby minimizing the leakage current for a given gate width. A further reduction in the effect of capacitor voltage degradation can be obtained by using a differential auxiliary input. For a differential input the worst case estimate of the degradation in the differentially applied correction voltage over the hold time is

$$(\Delta V_{C_{n(m)}} - \Delta V_{C_{r,n(m)}}) \approx \frac{1}{f_{\text{clk}}} \frac{I_L}{C} \left(\frac{\Delta I_L}{I_L} + \frac{\Delta C}{C} \right) \quad (16)$$

where I_L and C are, respectively, the nominal values for the switch leakage current and hold capacitor, $\Delta I_L/I_L$ and $\Delta C/C$ are the relative mismatch of the leakage current and capacitors, respectively, and f_{clk} is the frequency of the auto-zeroing clock. A low auxiliary path gain will further desensitize the auxiliary input to leakage current effects.

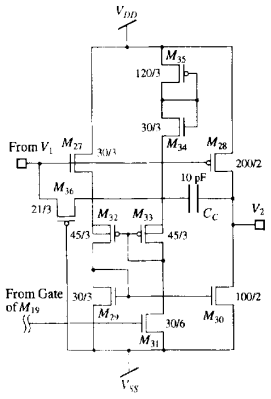

Fig. 6. Main amplifier's output stage. All device sizes are in μm.

C. Internal Amplifiers

A folded-cascode design [13] was chosen for the nulling amplifier due to its high dc gain and ability to drive the large capacitive loads presented by the hold capacitors (Fig. 5). The main amplifier consists of an input stage identical to the nulling amplifier coupled to an additional output stage which provides drive capability for resistive loads (Fig. 6). The folded-cascode stage was modified to provide an auxiliary differential input.

A variety of methods have been used to implement an auxiliary input for an amplifier. These include using an adjustable current mirror [3], [14]–[16], a voltage follower [2] which combines the primary and auxiliary input signals before they are applied to the input differential pair, a second differential pair in parallel to the primary pair [3], [17], and a differential difference amplifier (DDA) [18].

We chose a new topology for the implementation of the auxiliary input. A small resistance of value $2R$ is inserted in the source leads of the primary input's differential pair (Fig. 5). A differential pair (M_{11}, M_{12}) controlled by the auxiliary input signal ($V_a^+ - V_a^-$) generates a differential current ΔI which flows through the resistance. This creates a differential voltage ΔIR between the sources of the primary differential pair transistors M_1, M_2 that can be used to compensate the offset voltage.

Provided that $2R \ll 1/g_{m1}$, the presence of the $2R$ resistor will not degrade the gain of the primary signal path significantly but will allow a large gain ratio α to be obtained between the primary and auxiliary paths. A large gain ratio is important for high temperature operation in order to desensitize the offset correction input from the degrading effect of leakage currents on the hold capacitors.The primary signal path gain of the input stage (Fig. 5) is

$$A_o = \frac{V_1}{V^+ - V^-} \simeq \frac{g_{m1} r_o}{1 + (g_{m1} + g_{mb1})R}, \tag{17}$$

where g_{m1} and g_{mb1} are the primary input differential pair's gate-source and body-source transconductances respectively, and r_o is the output impedance of the folded-cascode stage.

For the auxiliary input, the gain is

$$A_o' = \frac{V_1}{V_a^+ - V_a^-} \simeq g_{m11} r_o R \frac{g_{m1} + g_{mb1}}{1 + (g_{m1} + g_{mb1})R}. \tag{18}$$

The ratio of primary to auxiliary path gains is therefore

$$\alpha = \frac{A_o}{A_o'} \simeq \frac{1}{g_{m11} R(1 + \eta_1)} \tag{19}$$

where $\eta_1 = g_{mb1}/g_{m1} \simeq \gamma/(2\sqrt{2|\phi_F| + V_{SB1}}$, γ is the bulk threshold parameter, and $2|\phi_F|$ is the surface potential at strong inversion.

The choice of R is bounded by the requirements that $2R \ll 1/g_{m1}$ and that the maximum offset voltage that can be compensated is $2I_{D26}R$, where I_{D26} is the drain current of M_{26}. The maximum gain ratio α is ultimately limited by the supply voltages and the maximum offset voltage to be corrected.

A 100 μA bias current was chosen for the primary differential pair M_1, M_2 to ensure that the nulling amplifier is able to slew from one supply rail to the other (-2.5 to $+2.5$ V) within one half of a clock period ($f_{\rm clk} = 100$ Hz). A fast slew rate ensures that the nulling amplifier's output can reach the required correction voltage within one clock cycle. The large bias current level also ensures that source/drain diffusion leakage currents do not significantly alter the bias current levels at high temperatures.

The primary differential pair transistors M_1, M_2 are sized $W/L = 600/6$ in order to achieve a large g_m and relatively low inherent offset. The maximum inherent offset of the input stage due to random errors in device sizes and threshold voltages was estimated using the methods in [19] to be approximately 5.5 mV. To provide a margin of error, the maximum offset to be compensated was taken as 10 mV.

Based on preliminary experimental work we expected the leakage currents of the sample and hold switches to have $I_L \leq 6$ nA, with a mismatch of $\Delta I_L \leq 1$ nA at 200°C. The MOSFET's used in the hold switches have a doughnut shaped layout with a $W/L = 15.7/3$ and a centre diffusion area of 15.4 μm^2. The hold capacitors are 100 nF ($\pm$20%) ceramic cased high temperature (+200°C) capacitors. At 200°C, these capacitors retain 40% of their 25°C capacitance, and have a measured parasitic leakage current of <0.7 nA. Using (16), a worst case estimate of the degradation of the differentially applied correction voltage over one half of a clock period ($f_{\rm clk} = 100$ Hz) at 200°C yields a 0.6 mV change.

The nulling amplifier's dc open loop gain $A_{\rm on}$ was estimated using SPICE to be approximately 10^5. For this value of $A_{\rm on}$, the offset at 200°C should be minimized if α_n is ~80 and α_m/α_n is unity.

To allow compensation of up to $\pm$10 mV of offset voltage a resistance of 1000 Ω was chosen for $2R$ along with a bias current of 10 μA for the auxiliary input differential pair M_{11}, M_{12}. With the transconductance of the primary differential pair transistors M_1, M_2 being approximately 500 μA/V the addition of the resistor degrades the primary signal path gain by less than 2.5 dB. The resistor is implemented using p^+ doped polysilicon (45 $\Omega/\Box$). The current mirrors M_{13}, M_{15} and M_{14}, M_{16} are unity gain. Transistors M_{17}, M_{18}

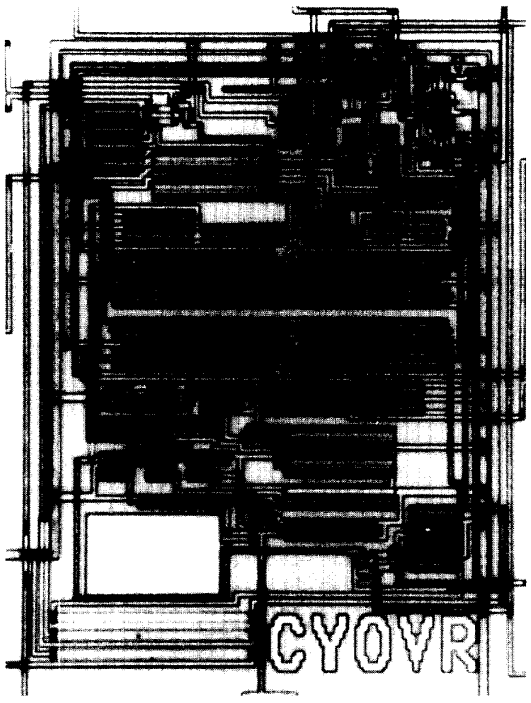

Fig. 7. Amplifier die photograph.

TABLE I
MEASURED AMPLIFIER PERFORMANCE. OFFSET VOLTAGE WAS MEASURED FOR 48 DEVICES AT 25°C AND FOR 8 DEVICES AT 200°C. THE OTHER SPECIFICATIONS ARE BASED ON MEASUREMENTS FROM AT LEAST TWO DEVICES.

Parameter	Measured 25 °C	Measured 200 °C	
Supply Voltages	+/− 2.5		V
Supply Current	1.1	1.1	mA
Clock Frequency	100	100	Hz
Offset Voltage	< 60	< 200	μV
Temperature Coef.	< 0.8		μV/°C
Input Bias Current		< 25	nA
Input Offset Current		< 1	nA
Unity Gain-Bandwidth w/ $C_L = 100$ pF, $R_L = 10$ kΩ	3.3	2.2	MHz
Phase Margin w/ $C_L = 100$ pF, $R_L = 10$ kΩ	39	42	deg
Slew Rate w/ $C_L = 100$ pF, $R_L = 10$ kΩ	6.8	5.4	V/μS
Power Supply Rejection Ratio	103	89	dB
Common Mode Rejection Ratio	92	92	dB
Peak-to-Peak Equivalent Input Noise Voltage	21	15	μV
Output Voltage Range w/ $R_L = 10$ kΩ	−2.4 → 2.4		V
Input Common Mode Range	−2.5 → 1.5		V

supply the remaining bias current required by the primary differential pair.

The frequency response of the main and nulling amplifiers must be designed to ensure that the auto-zeroed amplifier is stable during both clock phases. Stability during ϕ_1 requires that both the main amplifier's primary input signal path and the nulling amplifier's auxiliary input signal path be unity gain stable. During ϕ_2 the auto-zeroed amplifier has two forward signal paths: one directly through the main amplifier and the other via both the nulling and main amplifiers. If the internal amplifiers have frequency responses of the form in (2) then the open loop frequency response of the overall amplifier during ϕ_2 is approximately

$$\frac{A_{\mathrm{on}}A'_{\mathrm{om}}}{(1+s/w_{\mathrm{dn}})(1+s/w_{\mathrm{hm}})}\cdot\frac{(1+s/w_z)}{(1+s/w_{\mathrm{dm}})} \tag{20}$$

where the zero, $w_z = w_{\mathrm{dm}}\cdot A'_{\mathrm{om}}C_C/C_{n(m)}$, forms a doublet with the main amplifier's dominant pole. The spacing of the doublet's pole and zero is controlled through the main amplifier's auxiliary path gain A'_{om}, and the ratio of the compensation capacitor C_C (see Fig. 6) and the hold capacitor $C_{n(m)}$. As long as $w_z \ll A_{\mathrm{om}}w_{\mathrm{dm}}$, the unity gain bandwidth of the auto-zeroed amplifier is identical to $w_o = A_{\mathrm{om}}w_{\mathrm{dm}}$ during both clock phases.

Because of the zero in (20), the amplifier will only be stable for closed loop gains (noninverting) in the range

$$\frac{\alpha_m C_{n(m)}}{C_C} < \frac{1}{\beta} < \frac{w_o}{w_{\mathrm{hm}}}. \tag{21}$$

where β is the feedback factor. Unlike a conventional amplifier, the auto-zeroed amplifier has a maximum permissible closed loop gain. Using large hold capacitors and a large gain ratio α decreases the degrading effects of switch leakage currents and increases the maximum allowable closed loop gain.

The doublet can increase the settling time of the amplifier [20]. Consider a one volt step applied to an auto-zeroed amplifier with unity gain feedback. During ϕ_2 the amplifier's step response contains a slow settling component which has a time constant $1/w_z$ and a magnitude of

$$\frac{C_C}{\alpha_m C} - \frac{1}{A_{\mathrm{om}}}. \tag{22}$$

We estimate that the magnitude of this slow settling term is less than 10^{-6} for our design. Therefore, for a 1 V input step, the doublet alters the step response of the amplifier by less than 1 μV and so its effect is negligible.

To provide maximum flexibility during testing, an off-chip resistor was used to set the amplifier's bias current. For similar reasons an external clock was used. The reference points $V_{\mathrm{ref},n}$ and $V_{\mathrm{ref},m}$ were both brought off-chip to allow the measurement of the auxiliary path open loop gain. During operation, the reference points are both connected to the midpoint of the supply voltage.

IV. EXPERIMENTAL RESULTS

The amplifier was fabricated in a 1.2 μm n-well CMOS process. A die photograph is shown in Fig. 7. The die area, excluding bonding pads, is approximately 0.4 mm^2. The general specifications for the amplifier are given in Table I.

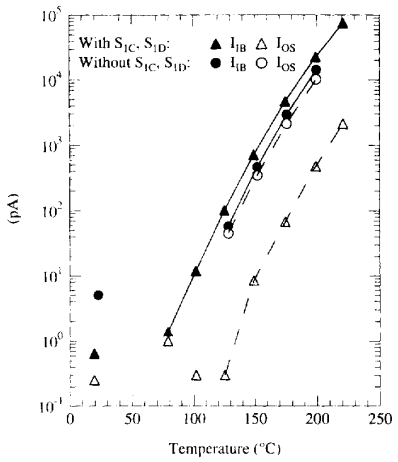

Fig. 8. Inputbias and offset currents for amplifiers with and without leakage current compensation switches S_{1C} and S_{1D}.

TABLE II
(a) MEASURED OPEN LOOP GAIN AND (b) PREDICTED OFFSET VOLTAGE (AT 25°C)

(a)

DC Open Loop Gain		
Complete Amp (Auto-zeroed)	150†	dB
Main Amp Primary Input (A_{om})	113††	dB
Main Amp Auxiliary Input (A'_{om})	72	dB
Null Amp Primary Input (A_{on})	80	dB
Null Amp Auxiliary Input (A'_{on})	39	dB

† Estimated using $A_{on} \times A'_{om}$
†† Estimated using $\alpha_m A'_{om}$

(b)

Amplifier	Offset Voltage Predicted (μV)	Measured (μV)
#1	− 0.3	+ 0.3
#2	+40.8	+48.8
#3	+ 7.4	+ 8.3
#4	−29.0	−23.2

To determine the effectiveness of the leakage compensation switches, two versions of the amplifier were fabricated, one with and one without the leakage compensation switches S_{1C} and S_{1D}. The results are shown in Fig. 8. At 200°C the average input current for the amplifier with switches S_{1C} and S_{1D} has increased to approximately 25 nA from 15 nA when the dummy switches are not included. The offset current, however, drops from 10 nA to less than 1 nA for the amplifier incorporating the dummy switches.

The dc open loop gains of the main and nulling amplifiers were measured along with their uncorrected offset voltages. The effective offset of the amplifier after auto-zeroing was then predicted using (8). The switching effects (ΔV_C's) are

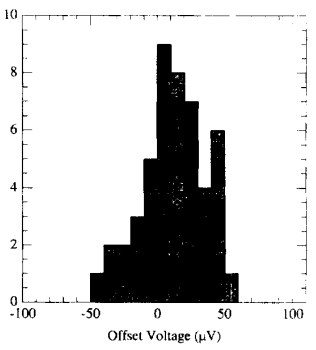

Fig. 9. Input offset voltage at room temperature (48 devices) with $f_{clk} = 100$ Hz.

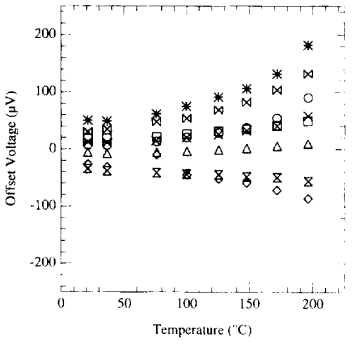

Fig. 10. Input offset voltage versus temperature ($f_{clk} = 100$ Hz) for a sample of eight amplifiers.

negligible at room temperature. The results are shown in Table II. The slight discrepancy between the predicted and measured values is primarily caused by the uncertainty in the open loop gain measurements.At room temperature (≈25°C) the mean offset voltage is 11 μV with a standard deviation of 24 μV for 48 units (Fig. 9). The variation of offset voltage with temperature is shown in Fig. 10 for a random sample of eight amplifiers.

The ±60 μV spread in measured offset voltage at room temperature is greater than expected (±20 μV). The low dc open loop gain A_{on} (10^4 instead of 10^5) of the nulling amplifier is primarily responsible. A careful re-evaluation of the SPICE Level 3 models which we used in our simulations indicates that the drain conductance is underestimated for devices operating with V_{ds} near $V_{ds,sat}$, such as transistors M_4 and M_{10}. The errors in modeling g_{ds} are discussed in detail in [21]. A more accurate BSIM2 model is under development which will allow more accurate gain prediction in future designs.

The value of $2R$ was measured to be approximately 725 Ω for the devices used in the open loop gain measurements given in Table II(a). The low value of the $2R$ resistor increases the gain ratio α to approximately 115 from the designed value of 80 resulting in a further increase in the effective offset. A variation of up to ±30% in the value of the polysilicon resistor

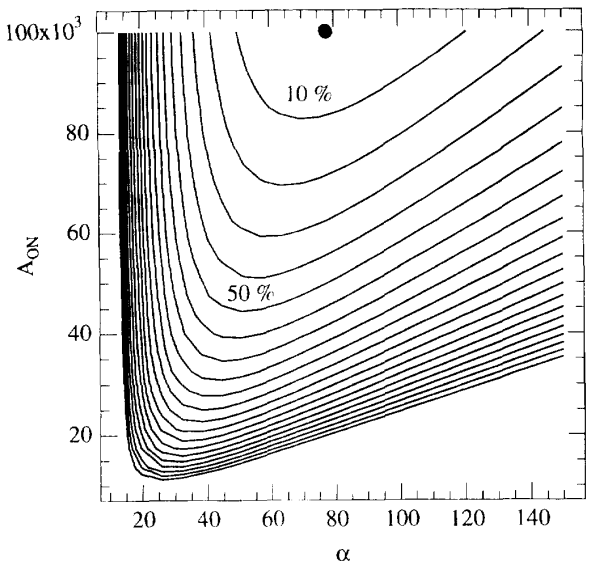

Fig. 11. Variation of the effective offset voltage with α and A_{on} for $V_{os,max} = 10$ mV, and $V_{aux,max} = 0.6$ mV. Contours are spaced at intervals of 10%, 20%, ..., 200% above the effective offset voltage at the optimal point (determined using (13) for $A_{on} = 10^5$). The heavy dot indicates the location of the optimal point.

$2R$ is expected and can be tolerated *if* A_{on} is near the design value. This is shown in Fig. 11. $A \pm 30\%$ change in both α and A_{on} results in less than a 30% increase in the effective offset.

Intermodulation distortion is a potential problem for all auto-zeroed amplifiers. This distortion is caused by the aliasing of signals that are near an integer multiple of the clock frequency. For this design, simulations show that the most significant contribution to intermodulation distortion comes from input signals that are within approximately 4 Hz of the clock frequency or an odd multiple of it. These signals generate attenuated ($>10^4$) distortion components in the dc to 4 Hz frequency range. Any distortion component aliased down to dc will change the amplifier's apparent offset voltage. Experimentally, we are unable to discern any intermodulation distortion components down to a level of approximately 20 μV.

A study of the amplifier's long-term reliability while operating at high temperatures must still be carried out.

V. Conclusion

A continuous-time auto-zeroed amplifier with input offset voltage and current of less than 200 μV and 1 nA, respectively, at 200°C has been developed. The amplifier is fabricated in a standard 1.2 μm n-well CMOS technology and uses an active area of 0.4 mm^2. It operates from a +5 V supply voltage and consumes 5.5 mW.

A new topology is used for the input switches to reduce the high-temperature input offset current. The effect of degradation of the offset correction voltages stored on the hold capacitors is minimized by the use of a desensitized differential auxiliary input, low-leakage switches, and large external hold capacitors. A new topology is used for the implementation of the internal amplifier's auxiliary input stage.

Acknowledgment

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