An Enhanced Slew Rate Source Follower

John G. Kenney, Giri Rangan, Karthik Ramamurthy, and Gabor Temes

Abstract— **A unity-gain buffer capable of high slew rates in both the positive and negative directions is presented. By sensing the drain current of the common-drain device in an NMOS source follower, the extent of slewing is detected, and the tail current of the source follower is dynamically adjusted. A buffer incorporating this strategy was implemented in a 2 μm p-well process. This buffer has over 4 times the negative-going slew rate and twice the bandwidth of a source follower, while requiring only 13% more static power. Moreover, the output voltage swing range is as large as that of a source follower. With a 20 pF output load, the measured 3-dB bandwidth was 9 MHz. The signal-to-total-harmonic-distortion ratio with 2 V_{p-p} sinewave input at a frequency of 2 MHz was better than 50 dB.**

I. Introduction

THE simplest realization of a unity-gain buffer is the source follower shown in Fig. 1. The properties which make it very useful as a voltage buffer are its high input impedance and relatively low output impedance for sufficiently large values of I_1 and $(W/L)_1$. However, when the input to the buffer is fast and has a large amplitude, the slew rate at the output of the circuit is limited. A relation can be established between the amplitude V_{in} of the input voltage and the output slew rate dV_{out}/dt. Assuming a square-law current/voltage relationship and neglecting channel-length modulation effects on transistors $M1$ and $M2$, the rate at which the output voltage V_{out} changes is

$$\frac{dV_{\text{out}}}{dt} = \left(\frac{1}{2}\frac{K_n W_1}{L_1}[V_{\text{in}} - V_{\text{out}} - V_T]^2 - I_1\right)/C_L. \quad (1)$$

where K_n is the intrinsic transconductance of the NMOS device and V_{th} is its threshold voltage. Equation (1) shows that a large voltage difference between V_{in} and V_{out} increases the current through $M1$, thereby charging C_L. This allows the output voltage to track the input voltage for rapidly increasing voltages. When V_{in} is decreased, however, the current flow out of C_L is only provided by the bias current I_1. Since I_1 is constant, the maximum rate at which the output voltage can change is limited to $-I_1/C_L$.

For a large load capacitance C_L, one can set I_1 very large to achieve a high slew rate. This, however, has several drawbacks: the dc power consumption scales linearly up with I_1, and also the positive output voltage swing is reduced; for a large dc input $V_{\text{in}} \cong V_{\text{DD}}$, the output is only $V_{\text{out}} = V_{\text{DD}} - V_T - (2L_1 I_1/K_n W_1)^{1/2}$. However, both the low static power consumption and the output voltage swing can be maintained by increasing I_1 dynamically (i.e., only when there is a large negative-going step on V_{in}).

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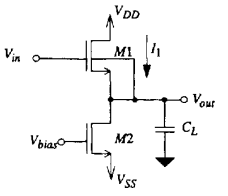

Fig. 1. Simple source follower.

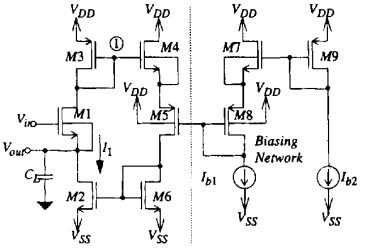

Fig. 2. Enhanced slew-rate source follower.

To achieve such a dynamic biasing of the source follower, the occurrence of slew-rate limiting must be detected [1]. When V_{in} decreases, such that the gate-to-source voltage of transistor $M1$ is less than its threshold voltage, the drain current of $M1$ goes to zero. By connecting a resistor or a diode-connected PMOS transistor to the drain of transistor $M1$ we can convert its drain current into a voltage. (A PMOS transistor is preferred, because it can achieve a larger effective resistance in a smaller area than a passive component [2].) This voltage can then be used to control the value of the bias current I_1.

The resulting slew-rate enhanced source follower is shown in Fig. 2. $M3$ is the diode-connected PMOS transistor which senses the reduction of the drain current I_1 in $M1$. As I_1 approaches zero, the voltage at node 1 rises toward the positive power supply V_{DD}. The small-signal open-loop transconductance from node 1 to the drain of transistor $M2$ is given by

$$\frac{i_{m2}}{\nu_1} = \frac{(W/L)_2}{(W/L)_6}\frac{g_{m4}g'_{m5}}{(g_{m4} + g'_{m5})}. \quad (2)$$

in which $g'_{m5} = g_{m5} - g_{mb5}$ includes the gate-to-source and the body-to-source transconductances of $M5$. Clearly, if ν_1 is positive, the current through $M2$ increases. Moreover, if ν_1 is negative, the current supplied by $M2$ decreases. Thus

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the ability of the source follower to slew in both directions is enhanced, since the I_1 term in (1) is now dynamically adjusted.

The negative-going slew-rate of the enhanced slew rate buffer can be estimated from the maximum voltage at node 1. In its quiescent state, the voltage at V_1 is $V_{\rm DD} - |V_{T0,P}| - V_{{\rm dsat},M3}$, where $V_{{\rm dsat},M3} = (2L_3I_1/K_pW_3)^{1/2}$. When the current in $M3$ goes to zero, V_1 is approximately $V_{\rm DD} - |V_{T0,P}|$, indicating an increase in voltage by $V_{{\rm dsat},M3}$. The total current available for slewing can be as large as

$$I_s = \frac{(W/L)_2}{2(W/L)_6}\frac{\beta_{M4}\beta_{M5}}{\beta_{M4}+\beta_{M5}+2\sqrt{\beta_{M4}\beta_{M5}}} \times (V_1 + V_{{\rm dsat},M3} - V_{G,M5} - V_{T0,N} + V_{T0,P})^2 \quad (3)$$

where $\beta_{M4} = K_n(W/L)_4$ and $\beta_{M5} = K_p(W/L)_5$. For typical saturation voltages, transconductances and with appropriate scaling of $M2$ with respect to $M6$, the slew rate can be improved by a factor of 3 to 5.

II. Output Voltage Swing

The CMOS class AB push-pull output stage, which also has very good slewing properties, has also been used as a unity-gain buffer (Fig. 3). An important advantage that the circuit of Fig. 2 has over a push-pull source follower is that it has a much wider output swing. As in the simple source follower, with all the transistors in saturation the output voltage of the proposed buffer can be as low as $V_{\rm SS} + (2I_1L_2/K_nW_2)^{1/2}$. By contrast, the push-pull follower of Fig. 3 has a minimum output voltage swing given by $V_{\rm SS} + (2I_1L_2/K_nW_2)^{1/2} + (2I_1L_1/K_pW_1)^{1/2} + V_{T,P}$, where $V_{T,P}$ is the threshold voltage of $M2$ and K_p is the intrinsic transconductance of the PMOS device. This is much larger due to the two additional terms. In a p-well process, the body of $M2$ must be connected to $V_{\rm DD}$, making the body effect in this device unavoidable. Consequently, the body effect increases $V_{T,P}$, which further limits the output swing in the direction of $V_{\rm SS}$.

If the wells of all the NMOS devices (for example, $M1$ in Fig. 1) are connected to their sources, both the source follower and push-pull follower will have a maximum output voltage given by

$$V_{\rm out,max} = V_{\rm DD} - V_{T0,N} - V_{{\rm dsat},n} - V_{{\rm dsat},p} \quad (4)$$

where $V_{{\rm dsat},p}$ reflects the fact the source follower is driven by an amplifier stage having a PMOS transistor in saturation. For the buffer of Fig. 2, the maximum output voltage is,

$$V'_{\rm out,max,} = V_{\rm DD} - |V_{T0,P}| - V_{{\rm dsat},n} - V_{{\rm dsat},p} \quad (5)$$

It can be reasonably assumed that $|V_{T0,P}| \approx V_{T0,N}$, and hence the maximum output voltage as determined by (5) is within a few hundred millivolts of the maximum output voltage specified by (4). $V'_{\rm out,max}$ for the new buffer is thus approximately equal to $V_{\rm out,max}$ of a simple source follower.

In conclusion, the overall output swing of the proposed enhanced-slewing source follower, while not as high as that of a common-source output stage [3], is comparable to that of the simple source follower, and is significantly better than the output swing of the push-pull follower. In contrast to the push-pull follower in which the body of one of the output transistors is always the substrate, and hence the body effect is unavoidable, in the proposed buffer the body effect can be prevented by connecting the well of the common-drain transistor to its source. Removing the body effect has the dual benefits of enhancing the output swing range and assuring that the buffer gain is very close to unity.

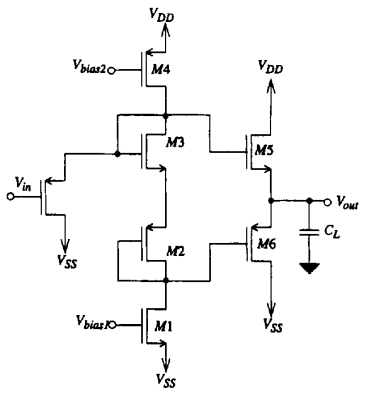

Fig. 3. Push-pull source follower.

III. Stability and Bandwidth

In the circuit of Fig. 2, feedback has been used to achieve the improved slewing performance. Consequently, the conditions for the stability of the loop must be examined. The open-loop gain of the buffer is

$$A(s) = \frac{g_{m1}g_{m2}g_{m4}g'_{m5}}{g_{m3}(g_{m1}+g_{d2}+sC_L)(g_{m6}+sC_1)(g_{m4}+g'_{m5})} \quad (6)$$

where we have assumed that the two dominant poles are determined by the impedances at the output node of the buffer and at the drain of $M3$. The small-signal parameter values needed in (6) were extracted from the actual circuit using HSPICE. It was determined that, with a 20 pF load, the first open-loop pole occurs at 5.9 MHz and the second open-loop pole is at 600 MHz. This analysis was supported by the pole/zero function within HSPICE. The open-loop dc gain for the feedback path is approximately -1.25. Because the dc gain is so low, the unity-gain crossover occurs at roughly the frequency of the first pole. Hence, the circuit has a large ($\approx$90°) phase margin.

Both the simple source follower and the enhanced slew rate source follower have a dominant closed-loop pole associated with their output nodes. The 3-dB bandwidth of the simple source follower is $f_{3\,\rm dB} = (g_{m1} + g_{d1})/2\pi C_L$. The 3-dB bandwidth of the enhanced slew rate circuit can be written as

$$f_{3\,\rm dB} \approx \frac{1}{2\pi C_L}g_{m1}\left(1 + \frac{g_{m2}g_{m4}g'_{m5}}{g_{m6}g_{m3}(g_{m4}+g'_{m5})}\right). \quad (7)$$

When the g_{m2} through g_{m6} are chosen so that the last term in (7) is around 1, the buffer will be stable for any size resistive

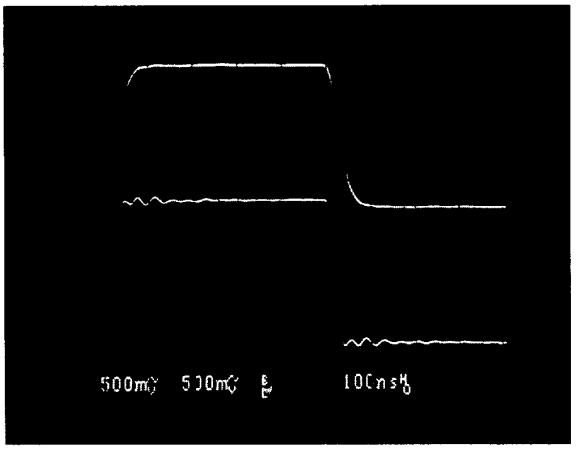

Fig. 4. 1 MHz 1.5 V_{p-p} input signal. Top trace=output; bottom trace=input.

or capacitive load. Moreover, the enhanced slew-rate source follower has about twice the bandwidth of a simple source follower. The added bandwidth helps to reduce the linear settling time. Even higher bandwidth and better slewing could be achieved by replacing $M3$ or $M6$ with a current source. However, this would also tend to reduce the frequency of the second pole by at least an order of magnitude, thus reducing the phase margin of the buffer.

IV. Experimental Results

The buffer of Fig. 2 was fabricated in a 2 μm p-well process. This allowed the connection of the well of transistor $M1$ to its source, thereby avoiding body effect. A load of 20 pF and a supply voltage of 5 V were used. With a 2 V_{p-p} sinewave input, the measured dc gain of the buffer was 0.96 and its 3-dB bandwidth was 9 MHz. The output voltage swing was fairly linear over a voltage range of 2.6 V. A 1 V_{p-p} input signal at a frequency of 100 kHz resulted in a THD below -60 dB; a 2 V_{p-p}, 2 MHz input gave a THD below -50 dB.

The measured transient response of the buffer to a square-wave input is shown in Fig. 4. With a bias current of 230 μA, the source follower $M1 - M2$ requires approximately 90 ns to slew over a 1-volt range for a negative input step. By adding $M3 - M6$, (3) suggests that the enhanced slew-rate buffer provides up to 945 μA of current for a negative-going step. Fig. 4 shows that the output of the buffer slews 1 V in approximately 20 ns. This translates into a current on the order of 1 mA, which closely matches the prediction from (3). The settling time to 1% of final value has been measured to be about 60 ns. The added bias current through transistors $M4, M5$ and $M6$ was 30 μA and thus the total static power consumption was 1.3 mW, compared to 1.15 mW for the much slower basic source follower. Some additional power is used by transistors $M7, M8$, and $M9$ in Fig. 2, which are needed to properly bias the buffer.

V. Conclusion

By monitoring the drain current of the common-drain device in a source follower, occurrence of slew rate limiting can be detected. This enables the dynamic adjustment of the tail current provided by the current source, which greatly enhances the slew rate. In effect, a negative feedback path is placed around the source follower. With an open-loop gain around -1, the bandwidth of the source follower could be doubled. It was also shown that the output voltage range of the enhanced slew-rate source follower is comparable to that of a simple source follower, and much larger than for a push-pull follower. The only penalty for this enhancement to the source follower was some added complexity, and a 10% increase in power consumption.

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References

[1] G. Rangan, J. G. Kenney, K. Ramamurthy, and G. C. Temes, "High speed buffers for op-amp characterization," *Proc. Int. Symp. Circuits and Syst.*, vol. 2, pp. 994–997, June 1993.

[2] R. Gregorian and G. C. Temes, *Analog MOS Integrated Circuits for Signal Processing*. New York: Wiley, 1986.

[3] R. Castello, "CMOS buffer amplifiers," in *Analog Circuit Design*. Dordrecht, The Netherlands: Kluwer, 1993.