Delay Components of a Current Mode Logic Circuit and Their Current Dependency

Yutaka Harada

***Abstract*—The delay of a CML circuit can be described in terms of the delay elements of a bipolar transistor such as junction capacitors C_{BC}, C_{BE}, C_{CS} and a cutoff frequency f_T. A new analysis method is proposed to calculate a CML delay. The nonlinear conductance of a bipolar transistor is approximated by a piecewise linear function. A resistor network is then picked up from the CML equivalent circuit to characterize the dc operation. This resistor network and the delay elements determine the CML delay. Subcircuits containing the resistor network and one or two of the delay elements of C_{BC}, C_{BE}, C_{CS}, and f_T are separately analyzed to clarify the delay components. The total CML delay is estimated from a linear sum of the delay components for a step input response. Current dependency of the CML delay is also discussed.**

I. Introduction

DUE TO their high-speed switching properties, current mode logic (CML) and emitter coupled logic (ECL) have been employed for high-speed mainframe computers. Much effort has been made to improve CML and ECL circuit performance. To develop these circuits further, CML delay estimation is a key issue. For CML and ECL circuit design, it is very important to clarify the delay components with respect to each delay element of a bipolar transistor because these delay components are not always improved by device design at the same time. Only by knowing the separate contribution of each delay element can device design be optimized. Many CML delay estimation schemes have been proposed and used for circuit design [1]–[8]. However these estimation methods are not sufficient enough to obtain an accurate delay because their models for a current switch do not reflect an actual operation.

This article intends to describe the actual switching mechanism of the current switch. For this purpose we propose a new analysis method. Firstly, a simple transistor model is built that includes a resistor, a diode, parasitic junction capacitors and frequency dependent current sources. Next, diodes are replaced by resistors whose approximated conductance values are determined by the transfer characteristic of the current switch. We then pick up the resistor network from the CML equivalent circuit. This resistor network specifies the dc characteristics. It is assumed that the CML delay is a function of the resistor network and delay elements such as C_{BC}, C_{BE}, C_{CS}, and f_T. Because a bipolar transistor pair of the current switch consists of eight parasitic delay elements finding the exact solution involves solving an 8th-order differential equation. To make the problem easier and to clarify the contribution of each delay element, we focus on subcircuits containing the resistor network and a subset of the delay elements. Choosing a subset containing the same kind of delay elements, the subcircuit shows the contribution from this kind of delay element. If two transistors of the transistor pair are identical, this subcircuit is expressed by a first-order differential equation that can be solved easily. Each delay component is obtained from a subcircuit analysis. We also discuss the relation between the total CML delay and the delay components. The total CML delay is estimated from the linear sum of the delay components for a step input response. As an application of this analysis, we also discuss the current dependency of the CML delay.

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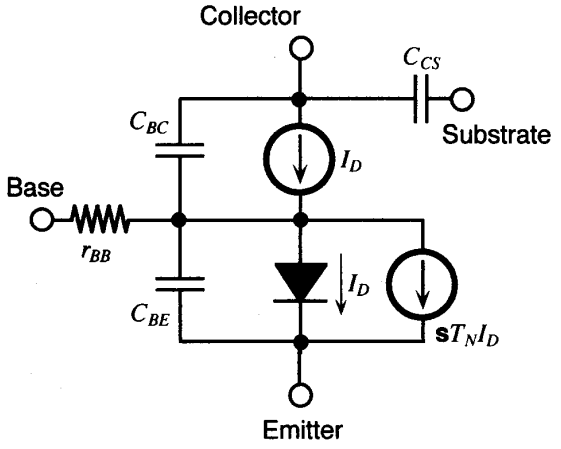


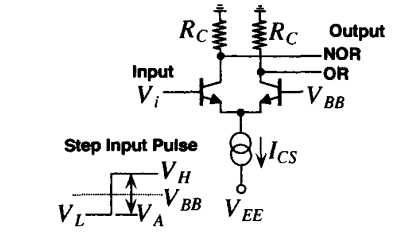
Fig. 1. A simplified transistor model based on the Ebers-Moll model. The current gain is assumed to be infinite.

II. Transistor Model and Transfer Characteristics of the CML Circuit

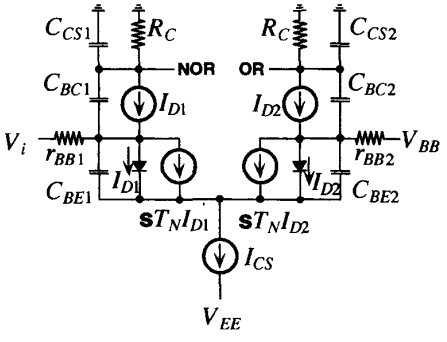
A. Transistor Model

The transistor model is shown in Fig. 1. This transistor model is based on the Ebers-Moll model that is composed of a resistor, a diode, junction capacitors and frequency dependent current sources. An equivalent junction capacitor defined by

$$\overline{C}_j = \frac{1}{V_1 - V_2} \int_{V_2}^{V_1} C_j dV \tag{1}$$



(a)



(b)

Fig. 2. The CML circuit model. Transistors are replace by a simplified transistor model shown in Fig. 1. Operation of this circuit is described by an eight-order differential equation.

is employed for the junction capacitor C_{CB}, C_{BE}, C_{CS} where V_1, V_2 are the maximum and minimum voltages applied to the junction capacitor. Generally, current gain β is given by

$$\beta = \frac{\beta_0}{1 + j\dfrac{\dfrac{\omega}{\omega_T}}{\sqrt{\beta_0^2 - 1}}} \tag{2}$$

where is β_0 is dc current gain and ω_T is the cut off angular frequency (transition frequency) of a bipolar transistor. We assume that β_0 is infinite, then β is given by

$$\beta = \frac{1}{j\dfrac{\omega}{\omega_T}}. \tag{3}$$

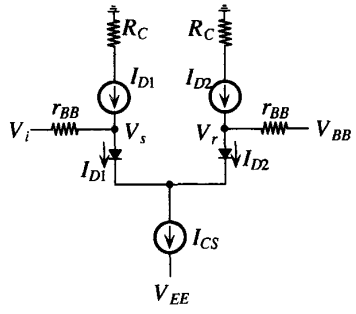
We employ a transition time T_N instead of ω_T, where T_N is defined as $1/\omega_T$. Consequently, the current gain is given by

$$\beta = \frac{1}{sT_N} \tag{4}$$

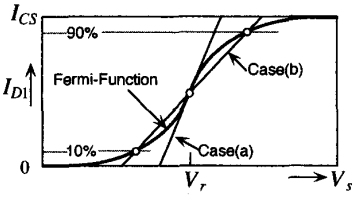
where s is a Laplace operator. According to the above discussion, the transistor model is schematically built as shown in Fig. 1.

B. CML Circuit Configuration and Its Transfer Characteristics

The CML circuit and its equivalent circuit with the transistor model described above is shown in Fig. 2. Here, C_{L1}, C_{L2} are load capacitors connected to output terminals. Let us discuss the nonlinear diode switching operation. The nonlinear diode



(a)



(b)

Fig. 3. The resistor network of the CML circuit and its transfer characteristics. (a) The resistor network. (b) The transfer curve and its two piecewise linear approximations.

characteristic is given by

$$I_D = I_s \exp\left(\frac{qV}{kT}\right) \tag{5}$$

where I_s is the diode saturation current, q is the electron charge, k is Boltzman's constant and V is an applied voltage. For the current switch, the switching current is given by a Fermi-function (6).

$$I_{D1} = I_{\mathrm{CS}}\left\{1 - \frac{1}{1 + \exp\left(\dfrac{q(V_s - V_r)}{kT}\right)}\right\}. \tag{6}$$

To simplify this circuit, we replace diodes by resistors. The $I - V$ characteristic of the diode is approximated by a piecewise linear curve as follow:

$$\begin{aligned} I_D &= g_e V_D + I_0 : I_D \geq 0 \\ I_D &= 0 : \text{Otherwise.} \end{aligned} \tag{7}$$

The approximated diode conductance value g_e is determined by the transfer characteristics of the current switch. To investigate the dc switching characteristics, we pick up and analyze the resistor network from the CML equivalent circuit as shown in Fig. 3(a). With the piecewise linear approximation, the transfer characteristic is written as

$$\begin{aligned} I_{D1} &= 0 : V_s - V_r \leq -\frac{I_{\mathrm{CS}}}{g_e}, \\ I_{D1} &= g_e \frac{V_s - V_r}{2} + \frac{I_{\mathrm{CS}}}{2} : |V_s - V_r| \leq \frac{I_{\mathrm{CS}}}{g_e}, \\ I_{D1} &= I_{\mathrm{CS}} : V_s - V_r > \frac{I_{\mathrm{CS}}}{g_e}, \end{aligned} \tag{8}$$

where V_s, V_r are the input voltage and the reference voltage minus the voltage drop across the base resistors and I_{CS} is the source current for the current switch. We define a transfer conductance g_{CS} as follows:

$$g_{CS} = \frac{1}{2} g_e. \tag{9}$$

Equation (8) shows a transfer curve with the linearized diode characteristic.

Comparing (8) with (6), as shown in Fig. 3(b), we investigate the following two cases to determine the transfer conductance g_{CS}.

(a) The gradient of the approximated transfer curve equals the differential coefficient at the center of the transfer curve.

(b) The gradient of the approximated transfer curve equals that of the line which pass through the 10% and 90% points on the Fermi-function.

The conductance value is calculated to be $g_{CS} = 1/4 \cdot qI_{CS}/kT$ for the case (a) and $g_{CS} = \mathbf{0.4}/\ln \mathbf{9} \cdot qI_{CS}/kT$ for the case (b) in Fig. 3(b). Circuit simulation tells us that the case (b) seems to be a better approximation than case (a). However we have not compared these approximation results enough to make any conclusion. Further investigation will be required.

III. Delay Analysis and Delay Component

A. Analysis Method

The complete configuration of the CML equivalent circuit is shown in Fig. 2. The transient operation of this circuit is described by an 8th-order differential equation since the network consists of eight delay elements. In general, an exact solution of an 8th-order differential equation is not given by a simple equation form. Our concern is not with the exact solution for the transient operation but with the delay component for each delay element. For this purpose, the exact solution is not required. We devise a new method to calculate the delay component focusing on the resistor network with each delay element. Fig. 4 shows the new method to calculate the delay for a high-order linear differential system. Generally, a switching circuit is built with a resistor network and capacitors. The order of the differential equation equals the number of capacitors. The switching circuit is reduced into a set of subcircuits which are combinations of the resistor network and subsets of the delay elements. Each capacitor is distributed to exactly one of the subcircuits. The number of the capacitors in the subcircuit is chosen to be no more than two so that the switching operation can be written in a simple form. The current switch of the CML circuit consists of a transistor pair, which suggests to us to choose the same kind of capacitors from the transistor pair for the capacitor subset. Especially, if both transistors of the transistor pair have the same device parameters, each subcircuit is described by a first-order differential equation. On this basis, we separately analyze subcircuits for each delay element of C_{BC}, C_{BE}, C_{CS}, and f_T. Delay components are calculated with each subcircuit.

Next, we discuss the delay composition. Stating the conclusion first, the total delay for a step response is estimated by summing up delay components. Elmore's delay model

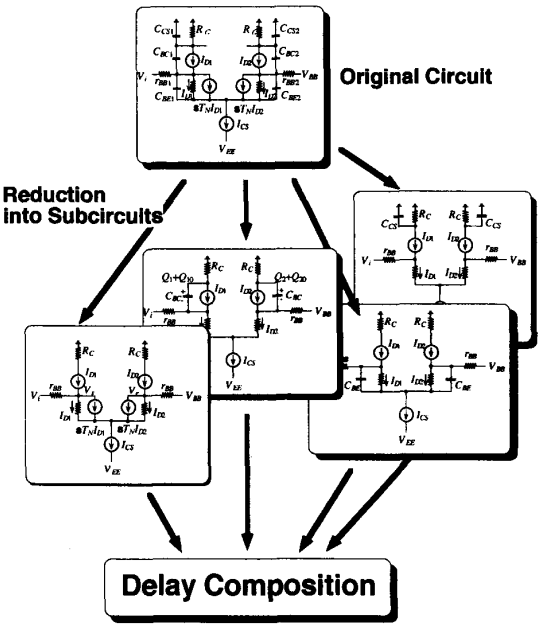


Fig. 4. A new method to calculate delay for a high-order linear differential system. A switching circuit is separately analyzed with combinations of the resistor network and subsets of the delay elements.

supports this conclusion [9]. Generally, a transfer function of the circuit network is expressed by a rational algebraic function

$$F(s) = \frac{1 + a_1 \mathbf{s} + a_1 \mathbf{s}^2 + \cdots + a_m \mathbf{s}^m}{1 + b_1 \mathbf{s} + b_1 \mathbf{s}^2 + \cdots + b_n \mathbf{s}^n} \tag{10}$$

where a_i and b_i are arbitrary real constants and m and n are positive integers. Elmore's theory indicates that a circuit delay t_d is approximated by

$$t_d = b_1 - a_1 \tag{11}$$

where a_1 and b_1 are the coefficients of $\mathbf{s}$ in the rational algebraic function. These coefficients for the CML circuit are expressed as follow:

$$\begin{aligned} a_1 &= r_{a\mathrm{CB}} C_{\mathrm{CB}} + r_{a\mathrm{EB}} C_{\mathrm{EB}} + r_{a\mathrm{CS}} C_{\mathrm{CS}} + \lambda_{aF} T_N \\ b_1 &= r_{b\mathrm{CB}} C_{\mathrm{CB}} + r_{b\mathrm{EB}} C_{\mathrm{EB}} + r_{b\mathrm{CS}} C_{\mathrm{CS}} + \lambda_{bF} T_N \end{aligned} \tag{12}$$

where $r_{a\mathrm{CB}}, r_{a\mathrm{EB}}, r_{a\mathrm{CS}}, \lambda_{aF}$ and $r_{b\mathrm{CB}}, r_{b\mathrm{EB}}, r_{b\mathrm{CS}}, \lambda_{bF}$ are real coefficients of the delay element of $C_{\mathrm{BC}}, C_{\mathrm{BE}}, C_{\mathrm{CS}}$, and f_T. It indicates that the coefficients a_1 and b_1 are written by a linear combination of the delay element values $C_{\mathrm{BC}}, C_{\mathrm{BE}}, C_{\mathrm{CS}}$, and f_T and resistance values of the resistor network. For the calculation of each delay component, we set all except one of the delay element of $C_{\mathrm{BC}}, C_{\mathrm{BE}}, C_{\mathrm{CS}}$, and f_T to zero for each subcircuit. It shows that a combination circuit with the resistor network and the delay element pair corresponds to only one of the product terms in a_1 and b_1. Consequently, a_1 and b_1 for the total delay are expressed by summing up delay components for the subcircuits described above.

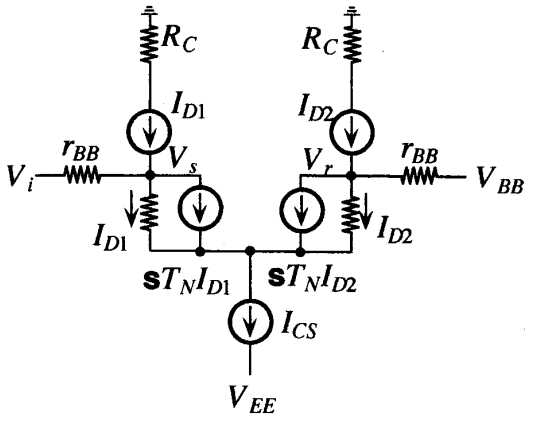


Fig. 5. The equivalent circuit for the delay component analysis of the cutoff phenomenon.

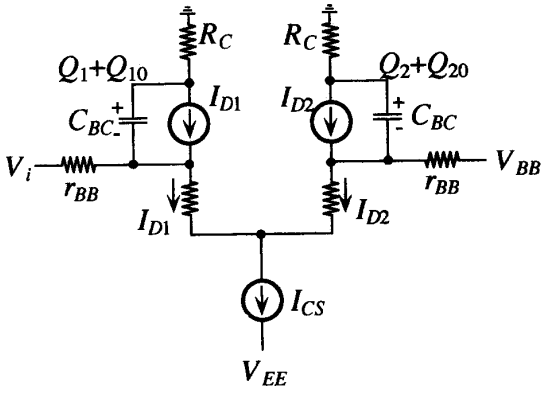


Fig. 6. The equivalent circuit for the delay component analysis of the base-collector junction capacitor.

In this paper, the input pulse V_i is assumed to be a step function. The input amplitude V_A is given by $V_A = I_{CS}/g_{CS}$ to fit into the approximated transfer curve shown in Fig. 3. The low-level V_L and high-level V_H of the input are $V_{BB} - V_A/2$ and $V_{BB} + V_A/2$ respectively. The input V_i is expressed by

$$V_i = \frac{V_{BB} + \frac{1}{2}V_A}{\mathbf{s}} \tag{13}$$

with the initial condition of $V_{BB} - V_A/2$.

B. Delay Components

1) Cutoff Frequency f_T: The cutoff phenomenon is characterized by the transition time T_N. Conventional analysis [5] tells us that the base response is written by $\tau_1 = (T_N/R_c)r_{BB}$. However it is very hard to find a relationship between the cutoff phenomenon of the transistor and the collector resistance from the view point of the CML circuit operation. The equivalent circuit that describes the cutoff phenomenon is shown in Fig. 5. The input voltage abruptly jumps from $V_{BB} - V_A/2$ to $V_{BB} + V_A/2$ at $t = 0$. The initial conditions for the diode current I_{D1}, I_{D2} are 0 and I_{CS} respectively. The diode currents I_{D1}, I_{D2} in a Laplace transform are given by

$$I_{D1} + T_N\mathbf{s}I_{D1} + I_{D2} + T_N(\mathbf{s}I_{D2} - I_{CS}) = \frac{I_{CS}}{\mathbf{s}}. \tag{14}$$

Then we get (15).

$$I_{D1} + I_{D2} = \frac{I_{CS}}{\mathbf{s}}. \tag{15}$$

This indicates that the sum of the two diode currents is constant value I_{CS}. With the transfer characteristics of the current switch in (6), the diode current I_{D1} is given by

$$\left\{\begin{array}{l} I_{D1} = g_{CS}\left\{V_i - r_{BB}T_N\mathbf{s}I_{D1} - \dfrac{V_{BB}}{\mathbf{s}} \right. \\ \qquad \left. + r_{BB}T_N(\mathbf{s}I_{D2} - I_{CS})\right\} + \frac{1}{2}\dfrac{I_{CS}}{\mathbf{s}} \\ V_i = \dfrac{V_{BB} + \frac{1}{2}V_A}{\mathbf{s}} \end{array}\right\}. \tag{16}$$

The solution of (15) and (16) is given by

$$I_{D1} = \left\{1 - \exp\left(\frac{t}{\tau_1}\right)\right\}I_{CS}, \tag{17}$$

$$\tau_1 = 2g_{CS}T_Nr_{BB}. \tag{18}$$

2) Base-Collector Junction Capacitance C_{BC}: Fig. 6 shows the resistor network with the base-collector junction capacitance pair. Charges $Q_1 + Q_{10}$ and $Q_2 + Q_{20}$ are stored charges at junction capacitors with the initial condition of Q_{10} and Q_{20}. The transient operation is expressed in the form shown in (19) at the bottom of the page. With the initial condition, (19) is rewritten as

$$\left\{\begin{array}{l} R_CI_{D1} + \left\{(r_{BB} + R_C)\mathbf{s} + \dfrac{1}{C_{BC}}\right\}Q_1 = -\dfrac{V_A}{\mathbf{s}} \\ -R_CI_{D1} + \left\{(r_{BB} + R_C)\mathbf{s} + \dfrac{1}{C_{BC}}\right\}Q_2 = 0 \\ I_{D1} = g_{CS}V_i + g_{CS}r_{BB}\mathbf{s}(Q_1 - Q_2) \end{array}\right\}. \tag{20}$$

The solution for I_{D1} is given by (21), shown at the bottom of the next page, and (22).

$$\tau_2 = (1 + 2g_{CS}R_C)r_{BB}C_{BC} + R_CC_{BC}. \tag{22}$$

$$\left\{\begin{array}{l} R_C\left(I_{D1} + \dfrac{dQ_1}{dt}\right) + \dfrac{Q_{10} + Q_1}{C_{BC}} + r_{BB}\dfrac{dQ_1}{dt} = -V_i \\ R_C\left(I_{CS} - I_{D1} + \dfrac{dQ_2}{dt}\right) + \dfrac{Q_{20} + Q_2}{C_{BC}} + r_{BB}\dfrac{dQ_2}{dt} = -V_{BB} \\ I_{D1} = g_{CS}\left(V_i + r_{BB}\dfrac{dQ_1}{dt} - V_{BB} - r_{BB}\dfrac{dQ_2}{dt}\right) + \dfrac{1}{2}I_{CS} \end{array}\right\}. \tag{19}$$

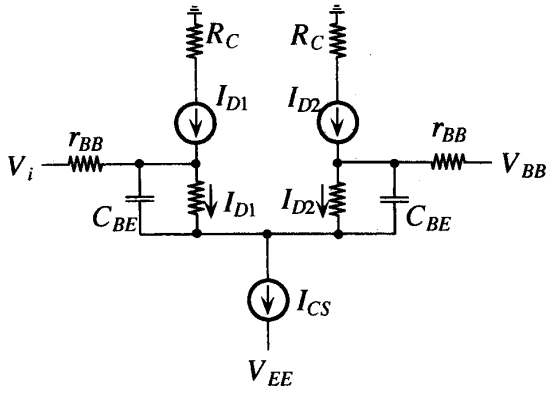


Fig. 7. The equivalent circuit for the delay component analysis of the base-emitter junction capacitor.

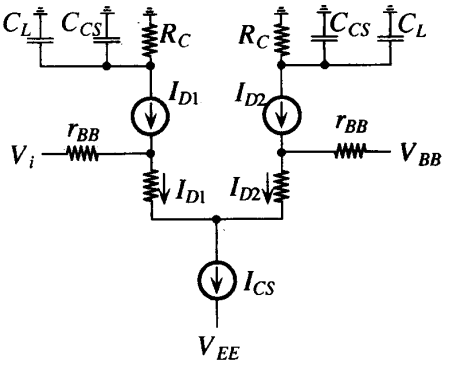


Fig. 8. The equivalent circuit for the delay component analysis of the collector–substrate junction capacitor.

Focusing on the time constant τ_2, the first term of (22) indicates that the input capacitor value through the base resistor $r_{\rm BB}$ is $(1 + 2g_{\rm CS}R_C)C_{\rm BC}$. Because the gain of the current switch is estimated to be $-2g_{\rm CS}R_C$, this term suggests the Miller effect. Conventional analysis tells us that the equivalent base-collector capacitance with the Miller effect is $2C_{\rm BC}$ because the gain of the logic circuit as a digital circuit is -1 [5]. However, our analysis notices that a logic circuit should be discussed as an analog circuit for the Miller effect. The Miller effect contribution for the CML delay is more significant than that of the conventional analysis.

3) Base-Emitter Junction Capacitance $C_{\rm BE}$: Fig. 7 shows the resistor network with the base-emitter junction capacitance $C_{\rm BE}$. The transient response for the input pulse V_i is written as

$$V_i - \frac{r_{\rm BB}C_{\rm BE}}{g_e}\mathbf{s}I_{D1} - \frac{I_{D1}}{g_e} = \frac{V_{\rm BB}}{\mathbf{s}} - \frac{r_{\rm BB}C_{\rm BE}}{g_e}(\mathbf{s}I_{D2} - I_{\rm CS}) - \frac{I_{D2}}{g_e}, \quad (23)$$

$$\frac{C_{\rm BE}}{g_e}\mathbf{s}I_{D1} + I_{D1} + \frac{C_{\rm BE}}{g_e}(\mathbf{s}I_{D2} - I_{\rm CS}) + I_{D2} = \frac{I_{\rm CS}}{\mathbf{s}}. \quad (24)$$

Then we get (25) from (24).

$$I_{D1} + I_{D2} = \frac{I_{\rm CS}}{\mathbf{s}}. \quad (25)$$

The solution of (23) (25) is given by

$$I_{D1} = \left\{1 - \exp\left(-\frac{t}{\tau_3}\right)\right\}I_{\rm CS}, \quad (26)$$

$$\tau_3 = r_{\rm BB}C_{\rm BE}. \quad (27)$$

4) Collector–Substrate Junction Capacitance $C_{\rm CS}$ and Load Capacitance C_L: Fig. 8 shows the resistor network with the collector–substrate junction capacitance $C_{\rm CS}$ and the load capacitance C_L. The transient response for the step pulse is written as

$$I_{D1} = \left\{1 - \exp\left(-\frac{t}{\tau_4}\right)\right\}I_{\rm CS}, \quad (28)$$

$$\tau_4 = R_C(C_{\rm CS} + C_L). \quad (29)$$

C. Delay Composition for a Step Response

Four delay components for $C_{\rm BC}, C_{\rm BE}, C_{\rm CS}$, and f_T, especially their time constant values, have been investigated. Defining the delay time as the time elapsed between when the step function is applied to the circuit and when the response has reached 50% of its final value, the delay components written in term of the time constants are

$$\begin{aligned} t_{d1} &= 0.7\tau_1 \\ t_{d2} &= 0.7\tau_2 \\ t_{d3} &= 0.7\tau_3 \\ t_{d4} &= 0.7\tau_4 \end{aligned} \quad (30)$$

for the delay components of $C_{\rm BC}, C_{\rm BE}, C_{\rm CS}$, and f_T, respectively. Where the coefficient 0.7 indicates approximated value of $\log_e 2$. The total delay t_d is given by

$$t_d = t_{d1} + t_{d2} + t_{d3} + t_{d4}. \quad (31)$$

The delay times given by (30) and (31) are compared with SPICE simulation results for several cases. Delay time calculated by (31) depends on the transfer conductance value. We have shown the transfer conductance $g_{\rm CS}$ by two cases in **2.2**.

We have observed that the conductance value for case (a) results in large error values for the delay estimation such

$$I_{D1} = \left\{1 - \frac{(1 + 2g_{\rm CS}R_c)r_{\rm BB}C_{\rm BC}}{(1 + 2g_{\rm CS}R_C)r_{\rm BB}C_{\rm BC} + R_CC_{\rm BC}}\exp\left(-\frac{t}{\tau_2}\right)\right\}I_{\rm CS}, \quad (21)$$

TABLE I
CURRENT DEPENDENCY OF THE CML CIRCUIT

Circuit Design	I_{CS} / R_C	0.8mA 700Ω	0.2mA 2800Ω
Time Constant	τ_1	104ps(24%)	26ps(3%)
	τ_2	190ps(45%)	295ps(39%)
	τ_3	25ps(6%)	25ps(3%)
	τ_4	105ps(25%)	420ps(55%)
Total Delay	τ_d	297ps	536ps

r_{BB}=350Ω, f_T=6GHz, C_{CB}=0.05pF, C_{BE}=0.07pF, C_{CS} + C_L =0.15pF

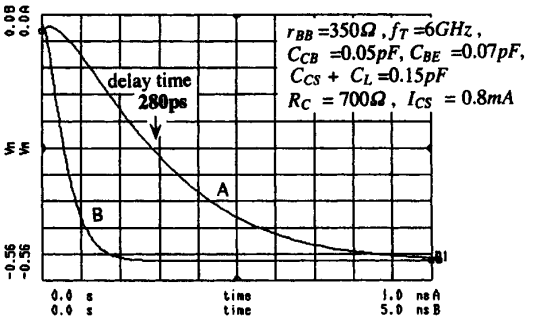
as 20% comparing with simulation values. However, if we employ the value for the case (b), errors remain within 10%. Consequently, the calculated delay times with the transfer conductance value for case (b) agree with simulation results. The error is estimated to be less than 10%.

IV. CURRENT DEPENDENCY OF THE CML DELAY COMPONENT

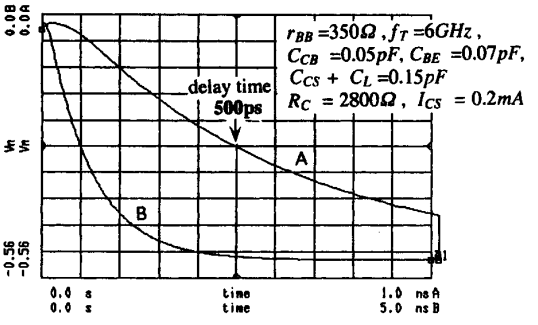
The transfer conductance value g_{CS} depends on the source current I_{CS}. This results in a current dependency of the CML delay. Employing the transfer conductance g_{CS} for the case (b), we compare a set of delay components with that for a different source current. Both delay component sets are compared under the same condition of an output signal amplitude of 0.56 V. Table I shows the delay components for an example CML circuit. The transfer conductance values g_{CS} for the source current I_{CS} of 0.8 and 0.2 mA are 5.6 and 1.4 mS, respectively.

Table I shows the delay components and their ratio in the total delay for the two cases. It indicates that the delay component ratio for the total delay depends on the source current of the current switch even if identical transistors are employed in both CML circuits. This ratio is a very important factor to know for optimizing device design. For example, the delay component for the cutoff frequency f_T is 24% at the source current of 0.8 mA but only 3% at 0.2 mA. Because the transfer conductance value g_{CS} is directly proportional to the source current I_{CS}, the time constant τ_1 at the source current of 0.8 mA is four times larger than that at 0.2 mA. This indicates that the larger source current results in the higher ratio. The delay component for the base-collector capacitance C_{BC} is 45% and 39% for each source current.

These ratios seem to be large number for both cases. The delay component for the collector-substrate capacitance $C_{CS}$is 25% and 55% for each case. Because the collector resistance R_C is designed to be inversely proportional to the source current I_{CS}, the time constant τ_4 at the source current of 0.8 mA is one fourth of that at 0.2 mA. This indicates that the larger source current results in the lower ratio. To improve the switching speed, we should make design choices according to the source current. For example, we try to decrease C_{BC}, C_{CS} and increase f_T for the source current of 0.8 mA. However, we may ignore increasing f_T for the source current of 0.2 mA, because its delay component is a small part of the total delay. We may also ignore decreasing C_{BE} for both. Thus, the delay component ratio indicates how device improvements should be made. The measured delay times with ring oscillators for the case of the source current of 0.8 mA are around 0.3 ns. Total delay times listed in Table I are compared with delay times simulated with the SPICE program (Hewlett Packard Impulse, HP85150B) as shown in Fig. 9. The simulation results tell that the total delay times are around 280 ps and 500 ps for both cases in Table I, respectively. It is estimated that errors are 5% and 8%. If we evaluate the transfer conductance g_{CS} more precisely, we will obtain better agreements.



(a)



(b)

Fig. 9. The simulation results are shown for both cases in Table I with the SPICE program (Hewlett Packard Impulse, HP85150B). The output signal is plotted with different time scales of 0 to 1 ns (marked A) and 0 to 5 ns (marked B) for each case. It is indicated that total delay times are around 280 and 500 ps, respectively.

V. SUMMARY

Delay components of the CML circuit are discussed. To trace the actual switching operation of the current switch, we propose a new analysis method. A simplified transistor model based on the Ebers-Moll model is employed. The diodes of the transistor model are replaced by resistors whose conductance values are determined by dc transfer characteristics of the current switch. We notice that this conductance value is one of the main parameters that determines the CML delay. However this value has been ignored in the conventional analysis. We pick up the resistor network from the CML equivalent circuit. This resistor network specifies a transfer characteristic. The CML equivalent circuit is reduced into a set of subcircuits that are combinations of the resistor network and a subset of delay

elements. The number of the delay elements is chosen to be no more than two so that each subcircuit can be analyzed exactly. We propose to choose a subset containing the same kind delay element pair in the current switch so as to obtain the delay component with respect to each of C_{BC}, C_{BE}, C_{CS}, and f_T. If transistors of the transistor pair have identical parameters, the circuit operation is written by a first-order differential equation. The total delay is calculated by summing up the delay components. This method contributes to lower the order of the differential equation describing the circuit operation that needs to be solved. Applying this method to the CML circuit, we calculate the delay components. We show that the delay component for the cutoff frequency is expressed by a product of the transfer conductance, the base resistance and the transient time of the transistor. This result is different from conventional analysis. We also formulate the delay component for the base-collector capacitor. The input capacitance is also discussed with respect to the Miller effect. Our analysis shows that the Miller effect contribution for the CML delay is more significant than that of conventional analysis. As an application of this analysis, we discuss the current dependency of the CML delay. It is noticed that the delay component ratio for the total delay depends on the source current even if identical transistors are employed for the CML circuit. This ratio indicates how device improvements should be made to achieve an optimized effect.

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