An Analog/Digital Interface for Cellular Telephony

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Abstract—**This paper describes a mixed-signal ASIC for dual-mode (analog/digital) cellular telephony applications. It consists of two transmit and two receive channels corresponding to the I and Q channels of a quadrature phase-shift keying (QPSK) modulation system. It also includes three 8 b DAC's for control purposes, as well as a bandgap voltage reference and bus interface circuitry. The chip is part of a four-chip implementation of an IS-54 dual mode telephone [1]. The chip was implemented in a 0.8 μm n-well double-metal CMOS process and uses a 5 V power supply. The die area of the chip was 23 mm^2 and the average power consumption was 125 mW.**

I. Introduction and System Description

THE increased use of cellular telephony has given rise to cost-effective monolithic implementations [2]–[4]. The IS-54 digital cellular standard offers a threefold increase in capacity over existing analog cellular systems [5]. This increase has been brought about by digital voice compression algorithms and time-division multiple access (TDMA). The IS-54 standard includes the AMPS analog cellular standard. Fig. 1 shows a block diagram of the IS-54 digital cellular subscriber unit [1] of which this chip was a part. The signal from the audio transducers is digitized by a PCM codec and processed by the voice processor that implements echo cancellation and voice coding. The voice processor interfaces to the modem processor that implements error correction, equalization, modem, and TDMA control functions in the digital mode and the FM/FSK signal processing functions in the analog mode of operation. The timing and interface controller (TIC) provides all the clock generation, synchronization, and digital interface functions. The analog/digital interface (ADI), which is the subject of this paper, provides the signal conversion functions and associated filtering that allow the digital subsystem to interface to the system's RF section. It has two receive and two transmit channels which correspond to the I and Q channels of a QPSK modulation system. The signal bandwidths of both receive and transmit channels was 15 kHz. The ADI also provides control signals for the AFC and AGC functions. The ADI communicates with the TIC through a 10 b data bus, a 3 b address bus, a 14.58 MHz master clock, and eight control signals. Fig. 2 is a block diagram of the ADI. Sections II–IV describe the architecture and circuit design aspects of the three major sections of the chip. Section V describes a novel method for generating test sequences to measure the harmonic distortion of the transmit section. Section VI describes the test results.

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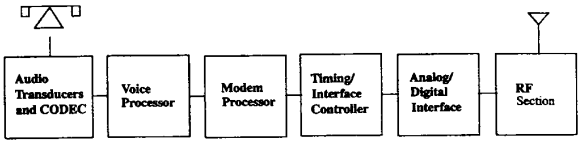

Fig. 1. System description.

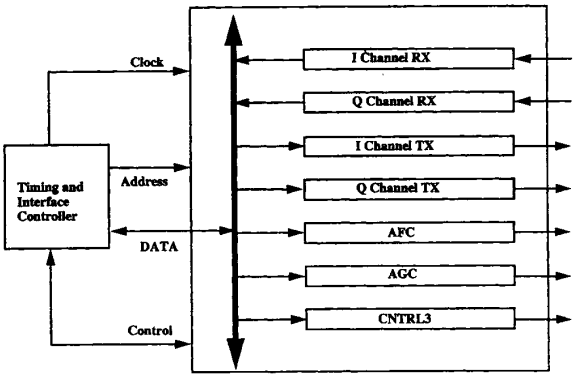

Fig. 2. Block diagram of chip.

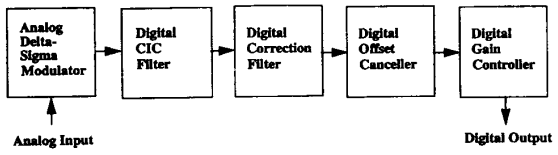

Fig. 3. Receive block diagram.

II. Receive Section

The receive section performs the analog-to-digital conversion for the baseband receive signal. Fig. 3 is a block diagram of the receive section. The receive input signal is specified to be at a maximum in-band level of 0.5 V p–p. The receive I and Q channels of the ADI each consist of an analog $\Delta - \Sigma$ modulator followed by digital filtering. Each receive channel has five gain settings in order to accommodate different RF receiver designs. It is required to have an SNR of 58 dB for the highest gain setting. At the highest gain setting, the worst

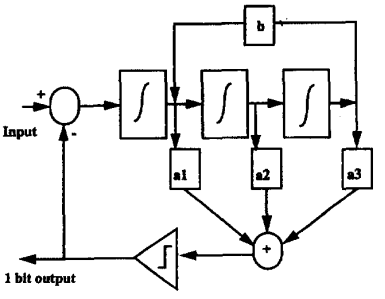

Fig. 4. Receive delta–sigma modulator.

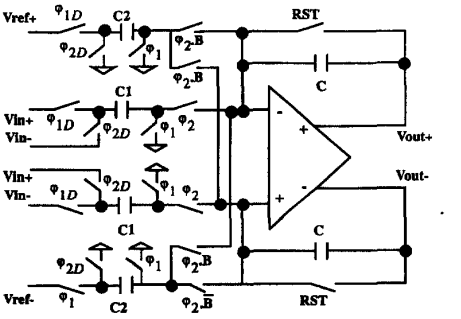

Fig. 5. Integrator 1.

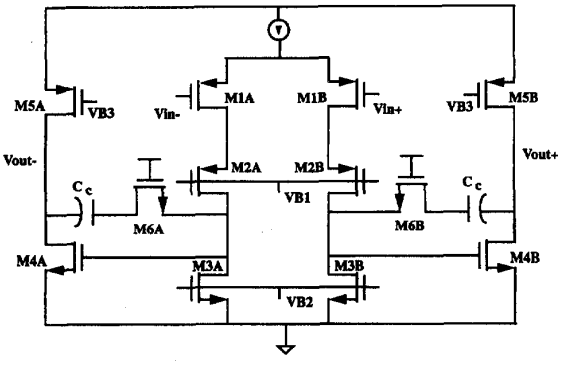

Fig. 6. Integrator 1 op amp.

case noise power in the adjacent channel is 24 dB higher than the passband signal. Therefore, the dynamic range of the receiver needs to be 82 dB. The signal-to-distortion ratio of each receive channel needs to be better than 85 dB so that the nonlinearity will not intermodulate the adjacent or alternate channel into the passband. A third-order delta–sigma modulator (Fig. 4) [6] with an effective oversampling ratio of 162 was chosen (the data rate at the pins of the chip is higher than Nyquist). This choice of architecture allowed us to meet the SNR specification with enough margin. Feedback from the output of the third integrator to the input of the second integrator moves a pair of zeros of the noise transfer function to form a complex pair at the edge of the passband.

The structure of the first integrator is shown in Fig. 5. It is a fully differential switched-capacitor integrator. Each of the switched capacitors has one clock delayed with respect to the other. This avoids signal-dependent charge injection from the switches, which is a source of distortion. This also assures that the charge injection is predictable from die to die. The op amp of the first integrator is designed such that it settles to an accuracy of 15 bits. Since the output of the integrator is sampled, the 15 b accuracy of the final value of this integrator ensures that all nonlinearity errors caused by slewing and nonuniform gain–bandwidth of this op amp are less than $1/2^{15}$ of the final value. This, in turn, ensures that the THD requirement of -85 dB is satisfied. The op amps were designed to have a crossover frequency of 25 MHz under worst case conditions. The phase margins of the op amps were designed to be over 70°. The slew rates of the op amps were kept high enough (180 V/μs) to support the high crossover frequency. The open-loop gain of the first integrator op amp needs to be high in order to reduce static nonlinearities introduced by the op amp. It must be remembered, however, that harmonics introduced into the modulator at any point other than at the input are attenuated. The degree of attenuation is given by the gain of the modulator from the input up to that point. Therefore, nonlinearities introduced at the output of the first integrator are attenuated by the gain of the first integrator, while nonlinearities introduced at the outputs of the other integrators are attenuated by the gains of two or more integrators. This is why the design of the first integrator is of critical importance. It is difficult to do a comprehensive analysis of all the sources of nonlinearity in the modulator. Approximate conservative analysis might not result in the most optimal design, but provides enough information to ensure adequate design margin.

The op amp of the first integrator is a two-stage op amp with a cascoded first stage for higher gain (Fig. 6). It can be noticed from Fig. 6 that only the differential pair is cascoded, and not its load. This is because the load transistors of the differential pair have long channels to minimize input-referred thermal noise and flicker noise [7], and therefore have high output impedances. The transistors that make up the differential pair need to have high transconductance in order to assure a high crossover frequency, and therefore require short channels. The differential pair is made of p-channel transistors for reduced flicker noise and higher slew rate [8]. The op amps of the two other integrators in the modulator drive lower capacitances since thermal noise generated by later stages of the modulator is attenuated by the loop gain of the modulator. Hence, these op amps have reduced power and area.

The digital part of the receive channel contains four blocks: a cascaded-integrator-comb (CIC) filter, a correction filter, a dc offset canceller, and a gain controller (Fig. 3). The CIC filter decimates the 1 b stream coming out of the modulator and provides some low-pass function. The correction filter corrects the passband droop caused by the CIC filter. The dc offset canceller removes any dc offset in the analog input, as well as offset generated by the modulator. The gain controller has the capability of selecting one of five output levels.

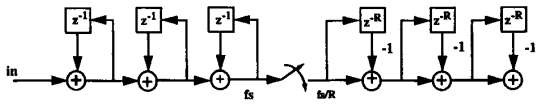

Fig. 7. Receive digital CIC filter.

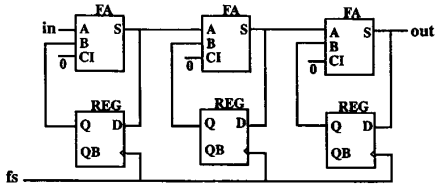

Fig. 8. Integrator and differentiator sections (FA =f ull adder, REG = register). (a) Integrator section. (b) Differentiator section.

A third-order CIC filter is shown in Fig. 7 [9]. Its transfer function is

$$H(z) = \left(\frac{1 - z^{-R}}{1 - z^{-1}}\right)^3$$

where $R = 54$ is the decimation ratio. An additional decimation by three is done inside the modem processor using a raised-cosine filter. The total filtering in the system was found adequate to meet the SNR specification. The CIC filter consists of three integrators operating at clock rate of f_s, followed by three differentiators operating at clock rate of f_s/R. In this design, $f_s = 4.86$ MHz, and $f_s/R = 90$ or 97.2 kHz for the analog and digital modes, respectively. The integrators and differentiators are built of adders and registers, as shown in Fig. 8(a) and (b). The reasons for choosing this filter structure are: 1) easily alterable decimation ratio R, 2) linear phase response resulting in constant group delay; and 3) simple hardware implementation requiring only adders and registers. The datapaths in the integrators and differentiators are both 19 bits wide. This datapath width is chosen after taking into account the maximum magnitude expected at the output of the last differentiator, thus ensuring that there is no overflow [9]. The correction filter is a three-tap FIR filter using power-of-two coefficients and has a linear phase response (Fig. 9). Its coefficients are chosen so that the passband ripple is within 0.1 dB p–p for both modes of operation.

The correction filter is followed by offset-correction and gain-control blocks. A 10 b dc offset is subtracted from the correction filter output. The gain controller provides five output levels from 0 to 24 dB in 6 dB steps. The output might exceed the range for a certain setting. When MSB's are discarded for a gain setting of 6 dB or higher, this might cause a large amount of distortion. In order to keep the amount of distortion low, overflow is detected and the output is clamped at its upper or lower limits. When LSB's are discarded, rounding is used instead of truncation because it results in better SNR. Fig. 10 shows the combined frequency response of the CIC and correction filters.

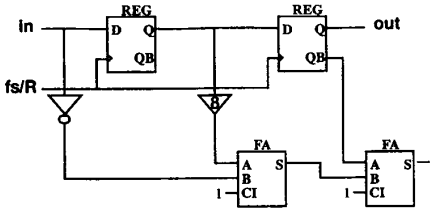

Fig. 9. Receive correction filter.

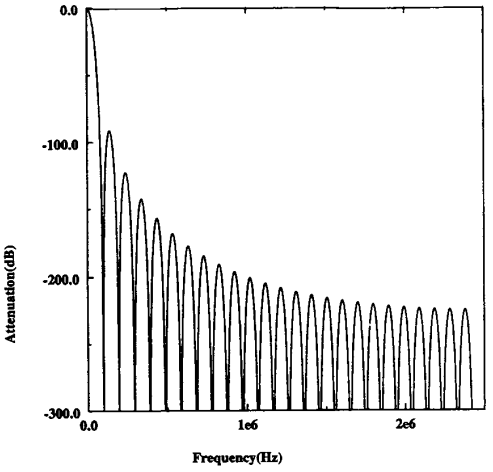

Fig. 10. Receive digital frequency response.

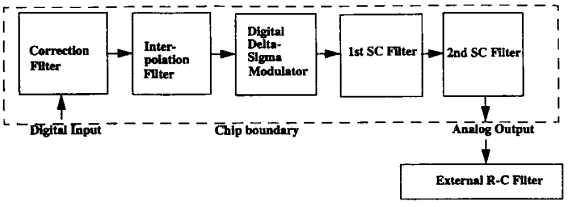

Fig. 11. Transmit block diagram.

III. Transmit Section

The transmit section consists of two Δ–Σ digital-to-analog converters, one each for the I and Q channels. Fig. 11 is a block diagram of the transmit section. The digital part of each transmit channel consists of three blocks: a correction filter, an

interpolation filter, and a second-order Δ–Σ modulator. The correction filter is used to correct the droop in the passband caused by the interpolation filter and the three stages of analog filtering after the modulator. It is a three-tap linear-phase FIR filter. The interpolation filter is used to create samples at the modulator frequency while attenuating images at multiples of the input sample rate. A third-order CIC [9] is also used as the interpolation filter (Fig. 12). It contains three differentiators operating at a clock rate of f_s/R and three integrators operating at a clock rate of f_s. In this design, $f_s = 4.86$ MHz, and $f_s/R = 180$ or 194.4 kHz for the analog and digital modes, respectively. The advantages of using this interpolation filter are the same as those mentioned for the decimator. The datapath widths in the differentiators were 16 bits each, and the datapath widths in the integrators were 26 bits. These widths were chosen to avoid overflow since that would cause the filter to enter an unstable state requiring a device reset. The interpolation filter was implemented using full adders and registers similar to those in the decimator [Figs. 8(a) and 8(b)]. The transfer function of the interpolation filter is

$$H(z) = \left(\frac{1 - z^{-R}}{1 - z^{-1}}\right)^3$$

where $R = 27$ is the interpolation ratio. The integrators of the interpolation filter are all singular at dc, i.e., at $z = 1$. These three dc poles are cancelled by the three zeros at dc provided by the three differentiators, yielding an overall FIR transfer function of

$$H(z) = \left(\sum_{n=0}^{R-1} z^{-n}\right)^3$$

which is stable. If a finite length input sequence to the first integrator leaves its output nonzero, then the outputs of integrators 2 and 3 will grow without bound. In fact, only a triply differentiated waveform will avoid overflow of the integrators. The practical impact of this is that each of the filter state variables must be reset at power-on, and that the clocking of the differentiators must be precisely periodic with respect to the integrators. In the present implementation, the differentiators derive their timing from transmit word writes to the bus interface. The integrators, on the other hand, derive their timing from the master clock supplied to the chip. However, a digital IS-54 channel is time-division multiplexed with two other channels, and hence is only active for 1/3 of a slot. It would have been wasteful to have the timing and interface controller chip (TIC) provide samples during the idle time to prevent the interpolation filter from going unstable. The solution adopted here is to have a time-out circuit which resets the interpolation filter at the end of each slot. The TIC can begin writes at the beginning of the next slot without concern for accurate timing relationship with the previous writes.

The passband of the transmit signal is 15 kHz. The most difficult design constraints on the transmit section, however, are the stopband power requirements. For example, the power in a 300 Hz band above 45 kHz is required to be 85 dB below the input signal in order to meet FCC requirements

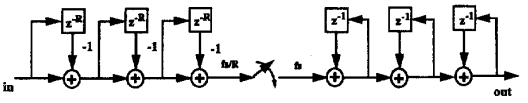

Fig. 12. Transmit interpolation filter.

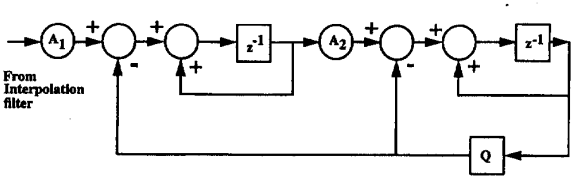

Fig. 13. Transmit digital delta–sigma modulator.

with sufficient margin. The SNR in the passband is only required to be 48 dB. A second-order delta–sigma modulator with an effective oversampling ratio of 162 was found to be sufficient to meet the given specifications [10]. A low-order modulator reduces the amount of quantization noise generated in the stopband, while still achieving the required SNR in the passband. Furthermore, a low-order modulator has the property that the quantization noise density rises with a more gradual slope outside the passband as compared to higher order modulators. This allows the use of fewer stages of analog filtering, while still meeting the stringent stopband requirements. It might be argued that for 10 b performance, some other DAC topology could have been used, especially since the Δ–Σ approach has the disadvantage that the out-of-band quantization noise needs to be filtered. However, the stiff total harmonic distortion specification on the transmit section (-85 dB) made us choose a Δ–Σ approach. Other advantages of the Δ–Σ approach are its ease of implementation and low sensitivity to component mismatches [11]. The structure of the second-order Δ–Σ modulator is shown in Fig. 13. The datapath width in the modulator was 26 bits.

The output of the digital modulator goes through three stages of analog filtering to convert the 1 b stream into an analog waveform with low out-of-band quantization noise. The analog filters also serve to remove any images at multiples of the input sampling rate which were not removed by the digital interpolation filter. The first stage is a first-order switched-capacitor (SC) low-pass filter which also functions as a 1 b digital-to-analog converter (Fig. 14). Delayed clocks are used to avoid signal-dependent charge injection. The slew rate and crossover frequency of the op amp were designed to keep the settling error below the 16 b level (the settling error needs to be less than that of the op amps in the receive Δ–Σ modulator because, in this case, there is no modulator loop gain to attenuate the harmonics). The high settling accuracy assures that the output of this switched-capacitor filter is very linear in a sampled-data sense. In other words, linearity is assured if the settled value is sampled by the next stage. However, there is a substantial slewing component in the settling transient of this filter. This is because the input of the op amp sees a voltage step of size $|V_{REFP} - V_{REFN}|$ at the beginning of $\phi 2$, which

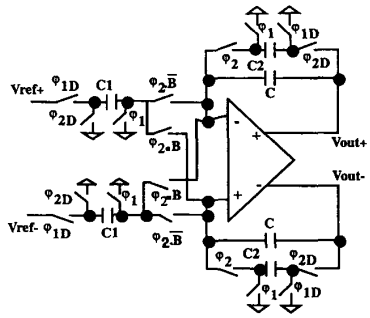

Fig. 14. Transmit SC filter 1 and 1 b DAC (B = modulator output bit).

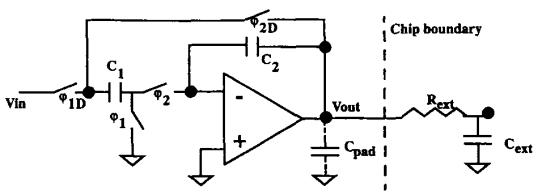

Fig. 15. Transmit SC filter 2 (single-ended version).

causes the op amp to slew. Therefore, the output of this filter cannot be used as a continuous time signal.

The next SC filter has a special topology which allows its output to be extremely linear. A single-ended version of this SC filter is shown in Fig. 15. It had to be assured that this SC filter could drive the output pad without a great degradation in linearity. There are a number of sources of nonlinearity in this SC filter.

First, there is op amp slew limiting. The topology of this SC filter is such that there is very little slewing because the input of the op amp does not see large voltage steps [12]. Specifically, the input of the op amp sees a voltage step equal to the difference between the present input and the previous output, at the beginning of ϕ 2. For highly oversampled systems, these steps are very small and are not enough to send the op amp into slew [13]. The op amp in this SC filter serves to charge any compensation or load capacitances at its output, but as far as capacitances C_1 and C_2 are concerned, there is only passive sharing of charge between them.

Second, there is nonlinearity due to the output capacitance. A two-stage topology was chosen for the op amp to reduce the effects of the output capacitance. In a two-stage op amp, the value of the output capacitance affects only the nondominant pole. The nondominant pole is approximately equal to g_{m2}/C_O where g_{m2} is the transconductance of the second stage and C_O is the output capacitance [8]. This pole changes with the signal because of the voltage variation of the output capacitance (which includes the pad capacitance) and because g_{m2} changes with the output current. However, with high phase margin (>70°), the nondominant pole has minimal effect on the settling transient, and therefore the nonlinearity of the pad capacitance is not an issue.

The third potential source of nonlinearity is not as obvious. This SC filter is followed by an external passive filter composed of the resistance R_{ext} and the capacitance C_{ext} (Fig. 15). This filter provides an additional stage of filtering for the out-of-band energy, and also serves to remove the sampling images at multiples of the clock frequency. This filter, in conjunction with the open-loop output impedance of the op amp, forms a pole-zero doublet (ω_z, ω_p) where

$$\omega_z = \frac{1}{R_{\text{ext}} C_{\text{ext}}}$$

and

$$\omega_p = \frac{1}{(R_{\text{ext}} + R_{\text{out}}) C_{\text{ext}}}.$$

R_{out} is the open-loop output impedance of the op amp at the pole frequency ω_p. This pole-zero doublet gives rise to a settling error E given by

$$E = \frac{\omega_z - \omega_p}{\omega_{co}}$$

where ω_{co} is the crossover frequency of the op amp [14]. The pole frequency of the external filter was about 38 kHz. In a two-stage op amp, the output impedance at high frequencies is approximately equal to $1/g_{m2}$ where g_{m2} is the transconductance of the second stage [8]. Now, g_{m2} varies with the output current, causing this settling error to be a potential source of nonlinearity. The peak output current can be calculated from the peak signal voltage and the complex impedance of the external filter at the highest signal frequency. From the peak signal current, the peak variation in settling error can be calculated. The peak variation in settling error ΔE can be shown to be

$$\Delta E = E \frac{\Delta g_{m2} R_{\text{ext}}}{(1 + g_{m2} R_{\text{ext}})}$$

where Δg_{m2} is the effective peak variation in the transconductance of the second stage. Choosing R_{ext} and C_{ext} to be 1 kΩ and 4 nF, respectively, and assuming g_{m2} to be nominally equal to 4 mmho and the crossover frequency of the op amp to be at 20 MHz, the nominal settling error can be shown to be 0.03%. Since this is a fully differential circuit, and also from the fact that the transconductance of a MOS transistor changes only as the square root of the signal current, the effective change in transconductance Δg_{m2} can be made as small as 3% of g_{m2}. Therefore, the peak value of the variation in settling error is only 0.0009%, which is too small to cause any significant distortion problem.

In the actual implementation, a source follower was used to buffer the output of the op amp (Fig. 16). This was necessary because resistors were used to sense the common mode of the output for the common-mode feedback circuitry. These resistors would have loaded the output and degraded the open-loop gain if source followers were not used. High open-loop gain is needed to reduce the effects of op amp nonlinearity. Even though the preceding analysis assumed an unbuffered two-stage op amp, it still applies to the buffered case because the output impedance of a source follower is also on the order of $1/g_m$. A p-channel source follower was used because

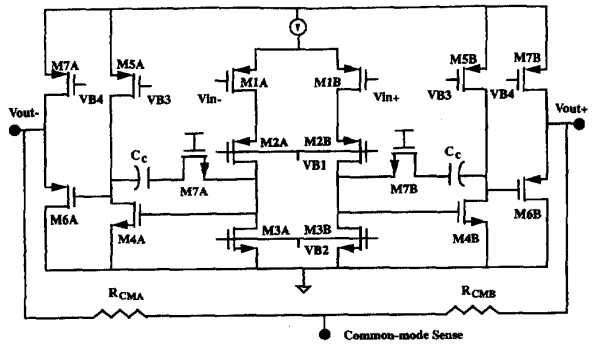

Fig. 16. SC filter 2 op amp.

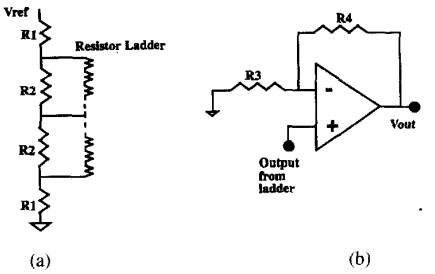

Fig. 17. Control DAC and output driver.

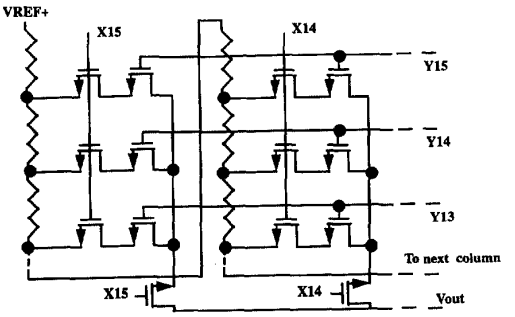

Fig. 18. Control DAC resistor ladder.

n-channel transistors in an n-well process would not have allowed the required output swing due to the body effect. Miller compensation was used around the second stage of the amplifier.

IV. Control DAC's

Three 8 b DAC's with output drivers are implemented on the chip for automatic gain control, automatic frequency control, and a yet unassigned control function. Standard resistor ladder DAC's are chosen because of their inherent monotonicity and their low static noise. Static noise is defined as the noise generated by the DAC when the input word is not changing. Switched-capacitor DAC's were not chosen because the continuous switching in those DAC's might give rise to a static noise problem. The resistor ladder of each DAC is followed by a driver which drives a 10 kΩ–20 pF load. The output of the driver was required to have 3.3 V p–p output swing.

The offset of the DAC's had to be less than 50 mV. The objective was to meet this specification without using self-calibration methods. A number of measures were taken to meet this objective. First, the closed-loop gain of the buffer was kept low so that the offset in the resistor string as well as the buffer offset were not gained up to a high value. Second, the voltage across the resistor ladder was designed to be an exact submultiple of the voltage range required at the output. This ensured that no additional voltage sources were required at the buffer, which would have contributed additional offset [Fig. 17(b)]. Third, as shown in Fig. 17(a), the middle of the bias string was connected to the middle of the main resistor ladder. The bias string, being smaller, was made of wider resistors and was laid out very carefully in order to assure good matching. Since the accumulation of mismatch is largest at the center of the string [16], the tying of the centers of the two strings reduced the offset of the DAC.

Fig. 18 shows part of the resistor ladder. The resistor ladder consists of 16 columns with 16 segments in each column. Each segment has a corresponding row switch and column switch as shown. There is an additional column switch at the bottom of each column as shown in Fig. 18. This column switch assures that the leakage current of the drain and source junctions of all the switches does not flow through the selected segment switches and through the resistor string because this can give rise to additional offset. Even though the leakage current of each junction is in tens of picoamperes, the switch resistances are high (on the order of 50 kΩ) because they are of minimum size and do not have a large V_{GS}. Hence, this can be a significant source of offset, especially at high temperatures. The additional column switch reduces this problem by a factor of 16. The column switch adjacent to the segment resistor is still needed to assure that the leakage current of all the row switches in each column does not flow through the selected row switch and the resistor string.

The resistors are made of n-diffusion. n-channel transistors are used for the tap switches, thus making the resistor string completely contactless and therefore very compact [17]. n-diffusion resistors were chosen because the bottom of the resistor string needs to be at a low potential in order to be a submultiple of the output voltage range for reasons mentioned earlier.

The total harmonic distortion specification of the control DAC's was only about 44 dB. This lax specification was taken advantage of in order to simplify the design. A primary source of nonlinearity in resistor strings is the mismatch between the resistor segments. The mismatch can be reduced by increasing the size of the resistor segments [16]. However, in this design, the resistor segments were made as small as possible in order to minimize area while still meeting the linearity specification. Since these are diffusion resistors, there is voltage variation of resistance along the string, and this contributes to nonlinearity.

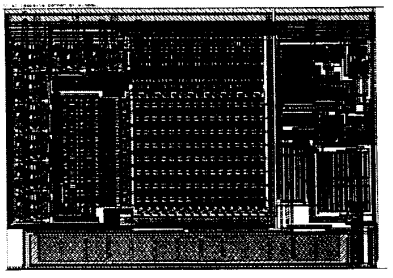

Fig. 19. Control DAC layout.

Assuming a linear relationship between voltage and resistance, it can be shown that

$$\text{Integral Nonlinearity} \approx \frac{(N+1)KV_{\text{REF}}}{8}\,\text{LSB}$$

where K is the fractional variation of resistance per volt and N is the number of segments [18]. The diffusion resistors used had a voltage variation of approximately 1000 ppm/V, and V_{REF} was 1.65 V. Substituting in the above expression gives an INL of 0.05 LSB's, which is small enough for this application. Variation of leakage current along the resistor string is also a source of nonlinearity, but is not a problem at the 8 b level.

Fig. 19 shows the layout of a control DAC. In the middle is the resistor ladder, and on its top and left are the digital latching and decoding circuitry. It can be seen that the digital circuitry occupies almost the same area as the ladder, thus showing that the design and layout are very close to optimal. The DAC's are each 500 × 400 μm in size.

V. Harmonic Distortion Measurement

The signal-to-distortion ratio (SDR) requirement for the transmit section was 85 dB. However, due to package limitations, the input word size was only 10 b. Also, because of limitations of test time and test memory size, it was not considered practical to send a very long sine wave into the part for testing the SDR. Nonuniformity of the spectral density of quantization noise made the SDR of the input worse than 85 dB, and therefore direct measurement of SDR would have given incorrect results. We devised two novel methods for measuring the SDR.

A. Trapezoidal Waveform

This method involves creating a repeating trapezoidal waveform as the test signal. The duty cycle, frequency, and amplitude of a trapezoidal waveform can be chosen in such a way that selected harmonics are absent from the signal. The Fourier series of the trapezoidal waveform shown in Fig. 20 is given by

$$f(n) = \frac{1}{2} - \frac{4}{\pi^2(1-2a)}\left[\sum_{k=\text{odd}}\left(\frac{1}{k^2}\cos(k\pi a)\cos\frac{k\pi n}{L}\right)\right]$$

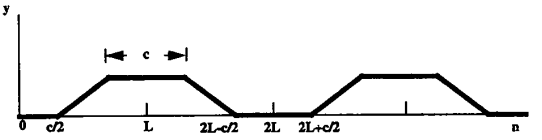

Fig. 20. Trapezoidal waveform.

where $a = c/2L$ and c and L are integers. The kth harmonic has zero amplitude if $k\pi a = \pi/2$, i.e., if $c = L/k$. For example, choosing $c = L/3$ suppresses the third harmonic of the fundamental. Since the period of the waveform is $2L$, and since the x axis is in terms of $1/f_s$, this restricts the fundamental frequency f_0 of the waveform to $f_s/2ck$. Also, the amplitude of the trapezoidal waveform is chosen to be $(n-1)b$ where b is an integer. This assures that all the samples of the trapezoidal waveform are integers, thereby avoiding any quantization effects.

B. Shaped Quantization Noise

The harmonic content of a quantized sinewave can be altered by using notch filters. Let us say we are required to quantize a sinewave of frequency f_0 to b bits. We first quantize the sinewave to $b_1 < b$ bits. We then pass this sinewave through a notch filter having integer coefficients with notch frequency nf_0 where n is the order of the harmonic to be suppressed. The filter will cause the word size to grow to b bits, but the integer operations would prevent any further quantization noise from being produced. For example, the filter

$$H(z) = 1 + z^{-1}$$

produces a notch at half the sampling rate $f_s/2$, and has a dc gain of 2. If a sinewave of frequency $f_s/4$ is quantized to 9 b and applied to this filter, the output will have a word size of 10 b with no quantization noise present at $f_s/2$. This method, however, has the disadvantage that since the starting sinewave is of low resolution, the final quantization noise floor tends to be high. The first method was therefore preferred. It was possible to bring the level of a given harmonic in the input down to about −140 dB using the first method.

VI. Experimental Results

The chip was fabricated using a 0.8 μm, n-well, double-metal CMOS process. Special care was taken in the circuit layout to reduce coupling of digital noise into the analog sections. For example, the digital and analog sections operated from separate power supplies. The total die area was 23 mm^2. The results reported in this section were were the worst-case numbers measured in the characterization laboratory. Fig. 21 is a photomicrograph of the die. The left half of the die is the digital portion, and the right half is the analog portion. The extreme left section of the chip is the transmit digital consisting of the interpolation and correction filters and the digital delta–sigma modulators of the two channels. On the

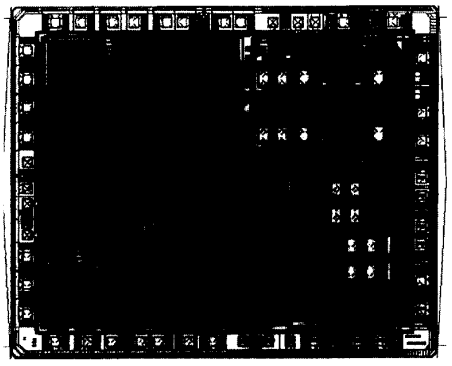

Fig. 21. Die photo.

TABLE I

PARAMETER	MEASURED VALUE
Receive Channel	
Gain Error	1.5%
Offset(uncalibrated)	< 5mV
SNR(0dB gain setting)	68dB
SNR(24dB gain setting)	61dB
Passband	15kHz
Passband Ripple	< 0.1dB
I and Q crosstalk	< -94dB
Total harmonic distortion	< -100dB
Intermodulation distortion	< -100dB
Transmit Channel	
Gain Error	< 3%
Offset	< 20mV
Passband	15kHz
Signal to Noise ratio	65dB
3rd harmonic distortion	<-94dB
Crosstalk (I and Q)	< -89dB
Crosstalk (Transmit and Control DAC)	< -80dB
Control DAC's	
Static noise power	< -80dB
THD	-48dB
SNR	48dB
Integral nonlinearity	1LSB
Crosstalk between DAC's	< -90dB
Output offset	< 20mV
Gain Error	< 3%

right of the transmit digital section is the receive digital section consisting of the CIC and correction filters, and the offset and gain correction blocks of the two channels. Table I shows some of the key results for the different sections of the chip.

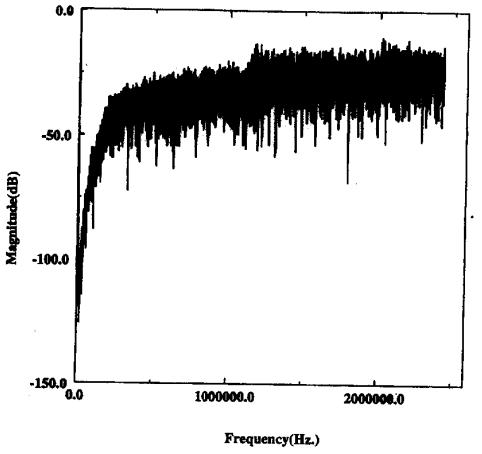

Fig. 22. FFT of receive modulator output.

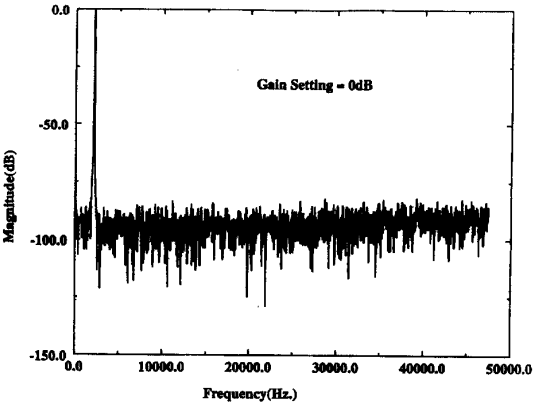

Fig. 23. Receive output spectrum.

The receive channel intermodulation distortion was measured with two signals in the alternate channel, where the alternate channel is the channel which is centered 60 kHz away from the channel under consideration. Both the total harmonic distortion and the intermodulation distortion of the receive section were much better than what the specification required, which shows that 15 b settling accuracy for the op amps was probably a conservative choice. Fig. 22 shows the shaped quantization noise at the modulator output, and Fig. 23 shows the output signal spectrum of the receive section.

System-level measurements showed that the transmit section met the stringent out-of-band requirements. The power consumption of the chip was 125 mW with a 5 V power supply.

VII. Conclusion

A low-power mixed analog–digital ASIC which serves as an analog front end for cellular telephony has been presented. Delta–sigma modulator technology has been extensively used

throughout the chip. Resistor ladders were used to implement the low-resolution digital-to-analog converters. The chip consumes 125 mW and has an area of 23 mm^2.

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