Brief Papers

A Low Supply Voltage High PSRR Voltage Reference in CMOS Process

Khong-Meng Tham and Krishnaswamy Nagaraj

Abstract— **This paper describes a bandgap voltage reference circuit that operates with a 3 V power supply and is compatible with a digital CMOS process. The use of a simple circuit topology results in a small silicon area of 0.07 mm^2, a power consumption of 1 mW and a high power supply rejection over a wide frequency band. The circuit realizes a temperature coefficient of 85 ppm/°C and a standard deviation of 20 mV without trimming.**

I. Introduction

THERE is a growing trend of designing precision analog circuits working off supply voltages in the 3 V range. This trend is driven by the need for battery operated systems. Economic reasons also need these circuits to be realized in a simple process, without resorting to the use of special low threshold devices. Stable voltage and current references are required in practically every analog circuit. Much work has been done in bandgap voltage references [1]–[8]. Some of these circuits use operational amplifiers and additional circuits, thus increasing silicon area and power dissipation. In order to meet the goals of low power supply voltage and low power dissipation, it is desirable to use a simple circuit configuration avoiding an operational amplifier. Simultaneously, it is also necessary to achieve high power supply rejection ratio over a broad frequency range in order to reject noise from the high speed digital circuits on the chip.

An op amp-less bandgap reference is presented in [7]. While this simple circuit topology achieves very high PSRR with low power dissipation, it needs a relatively large supply voltage (>4.25 V) for its operation. This paper will describe an enhancement to the circuit in [7]. This enhancement enables operation of the circuit down to 2.7 V supply without using low threshold devices and achieves high power supply rejection over a wide band of frequencies.

In Sections II and III the basic operations of this bandgap are described. Section IV discusses the sources of errors. Experimental results from test chips are described in Section V.

II. Basic Bandgap Circuit

The core of the bandgap circuit is shown in Fig. 1. The low temperature coefficient of the bandgap voltage is obtained by addition of a negative temperature coefficient (TC) base-emitter voltage of a bipolar transistor, with a positive TC voltage obtained from the difference of two base-emitter voltages biased at different current densities.

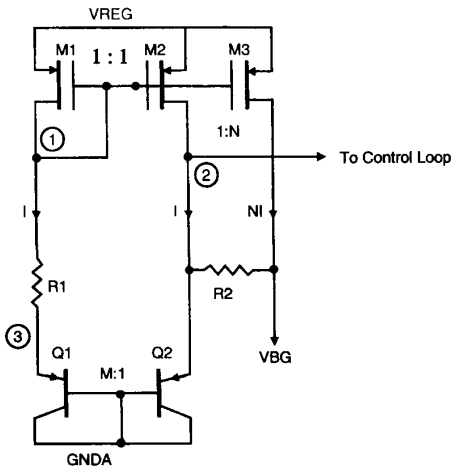

Fig. 1. Basic bandgap circuit.

The supply independence as well as the temperature independence are achieved by a feedback mechanism (discussed in Section III) that forces node 2 to be at the same potential as node 1. This simultaneously ensures that I_{M2} is an accurate copy of I_{M1}. The bandgap voltage VBG can be shown to be

$$\mathrm{VBG} = V_{BE2} + N\frac{R2}{R1}\ln[M(N+1)]V_T \qquad (1)$$

where M is the ratio of the emitter areas of transistors $Q1$ and $Q2$ and N is the ratio of the W/L of M3 and M1.

V_{BE2} has a temperature coefficient of −2.2 mV/°C at 25°C, while V_T has +0.085 mV/°C. By proper choice of $R2/R1$, M and N, temperature coefficient of VBG can be compensated to be zero at 25°C. The bandgap voltage output has a fairly high impedance. Thus, it needs to be buffered for further use.

III. Regulated Supply Generation

The bandgap circuit operates from an internal regulated supply VREG. The value of this voltage is adjusted by means of a high gain feedback loop such that the condition of equality of the voltages at nodes 1 and 2 is achieved. The higher the loop gain, the higher will be the rejection of the variations in the main supply VDDA. To achieve a high power supply

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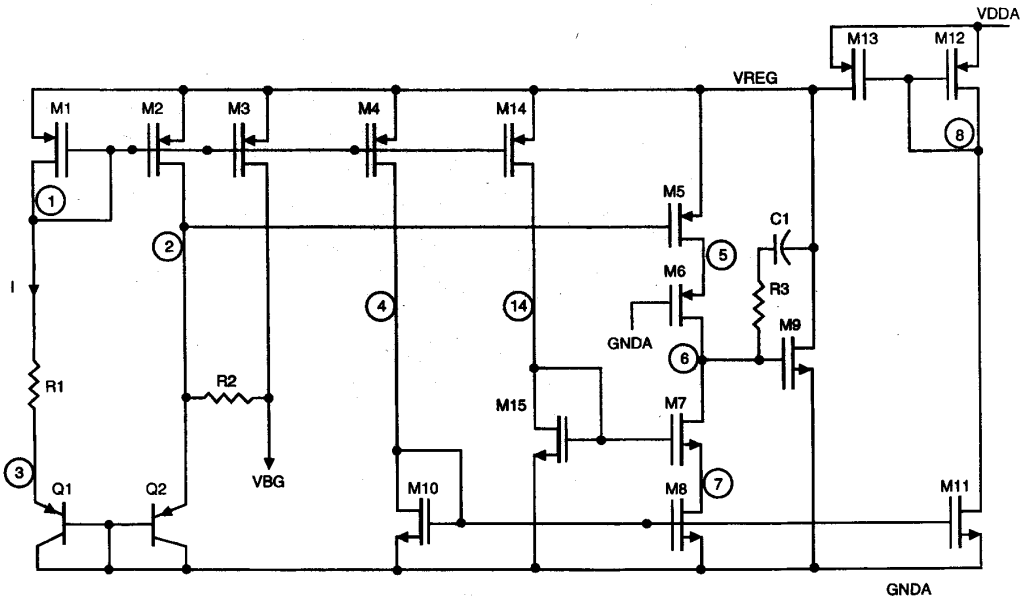

Fig. 2. High PSRR bandgap circuit with regulated supply.

rejection ratio over a broad frequency band while requiring low voltage and power, a simple circuit configuration is used for the feedback loop (see Fig. 2). The operation of this is as follows. The voltage variations at node 2 are sensed by $M5$, which along with $M6, M7$, and $M8$ constitutes a cascode amplifier. The amplified voltage is sensed by $M9$ which feeds a current into the node VREG so as to force it to the right voltage. To determine the loopgain, let us assume an incremental variation v_{reg} in the value of the regulated supply voltage. We can now write the following expressions for the incremental currents in the circuit.

$$i_{m9} = v_6 g_{m9} = (i_{m5} - i_{m8}) r_6 g_{m9} \tag{2}$$

where v_6 is the incremental voltage variation at node 6 and r_6 is the output resistance seen at node 6.

$$i_{m5} = g_{m5} v_{\text{reg}} \tag{3}$$

$$i_{m8} = \frac{g_{m8}}{g_{m10}} \frac{g_{m4}}{g_{m1}} i_{m1} \tag{4}$$

$$i_{m1} = \frac{v_{\text{reg}}}{1/g_{m1} + R1 + re1} \tag{5}$$

where $re1$ is the emitter resistance of $Q1$.

From (2)–(5), we have

$$i_{m9} = v_{\text{reg}} \left(g_{m5} - \frac{g_{m8}}{g_{m10}} \frac{g_{m4}}{g_{m1}} \frac{1}{(1/g_{m1} + R1 + re1)} \right). \tag{6}$$

Since $M4$ and $M5$ have the same gate voltage and $M5$ and $M8$ carry the same dc current, we can show that

$$\frac{g_{m8}}{g_{m10}} = \frac{g_{m5}}{g_{m4}}. \tag{7}$$

Thus, we have

$$i_{m9} = g_{m5} r_6 g_{m9} \left(1 - \frac{1}{(1/g_{m1} + R1 + re1)} \right) v_{\text{reg}}. \tag{8}$$

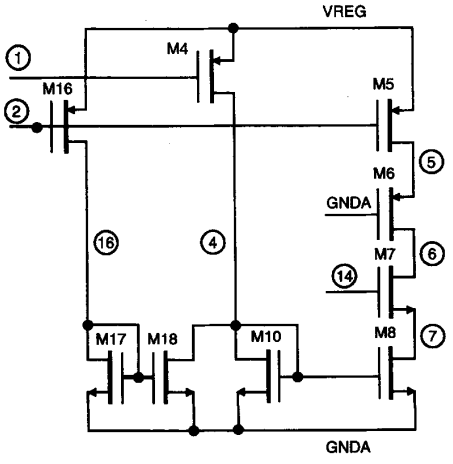

Fig. 3. Enhancement for further increasing PSRR.

The use of a cascode stage results in a large value for r_6, which results in a large value for i_{m9}.

The current variations in the other branches of the circuit resulting from the voltage variation at VREG also provide additional negative feedback. However, their contribution to the feedback gain is much smaller than i_{m9}. Thus, the loop gain can be approximately written as

$$A = \frac{i_{m9} r_{\text{reg}}}{v_{\text{reg}}} = g_{m5} g_{m9} r_6 r_{\text{reg}} \left(1 - \frac{1}{1/g_{m1} + R1 + re1} \right) \tag{9}$$

where r_{reg} is the resistance seen at node VREG.

The loopgain can be increased further by modifying the core amplifier circuit as shown in Fig. 3. Here, the voltage

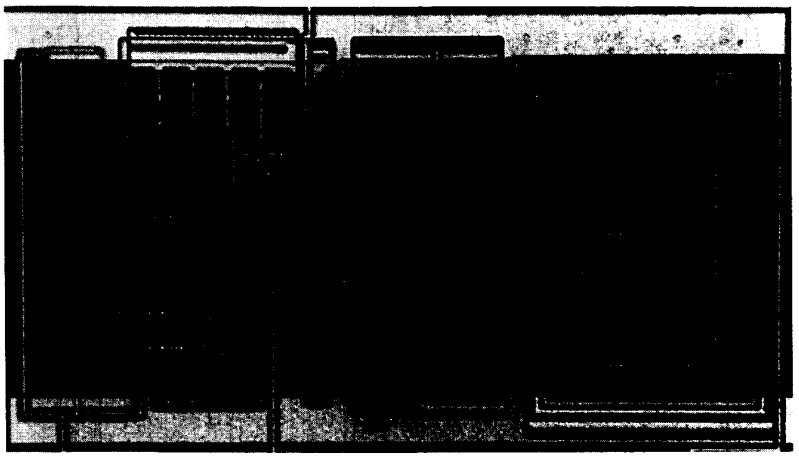

Fig. 4. Chip photomicrograph.

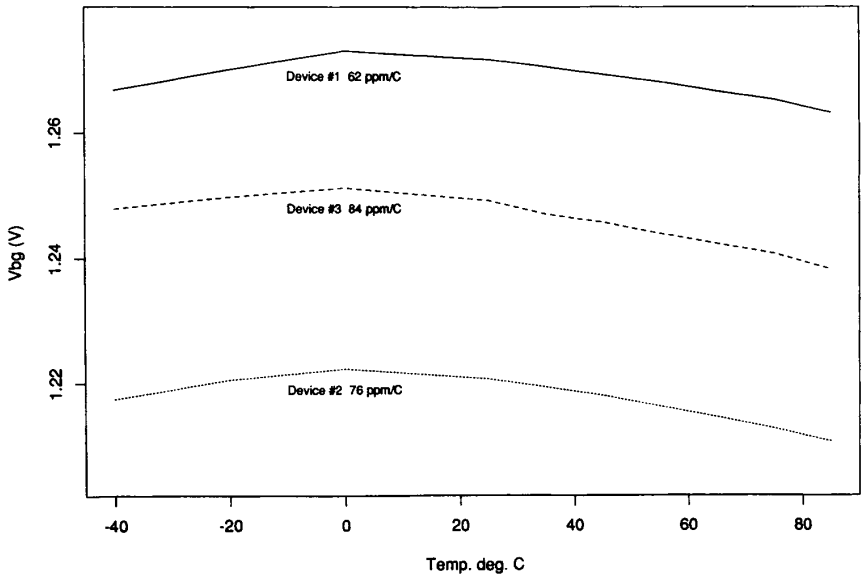

Fig. 5. Temperature dependence of bandgap output.

variations at node 2 are also sensed by $M16$ which produces a signal current component in $M8$ via the transistors $M17, M18$, and $M9$. This component aids the current produced by $M5$.

The core amplifier in Fig. 2 has a single high gain stage which forms the dominant pole. Other parasitics poles are typically high enough in frequency such that even with no compensation, the circuit is stable with wide bandwidth. However, the phase margin can be further improved by the addition of compensation capacitor $C1$ and resistor $R3$ (which can be a MOSFET resistor). The use of a simple amplifier structure allows the loop bandwidth to be high, resulting in a high PSRR over a wide frequency band. In the enchanced circuit of Fig. 3, the branch $M17, M18$ results in added parasitic poles, thus decreasing the usable loop bandwidth. This limits the extent to which the loopgain can be improved by this method. The larger we try to make the loopgain (by making the current gain in the mirror $M17$–$M18$ larger), the worse will be the stability of the circuit.

The current consumed by the entire circuit is directly proportional to the current that flows in the basic loop shown in Fig. 1. This current is in turn controlled by the value of $R1$. In practice the choice of the value of the current is governed by considerations of power consumption as well as the desired loop bandwidth.

IV. Sources of Error

The main sources of error in the value of the bandgap voltage are: the geometry mismatch between $Q1$ and $Q2$, the geometry and threshold mismatches between $M1, M2$, and

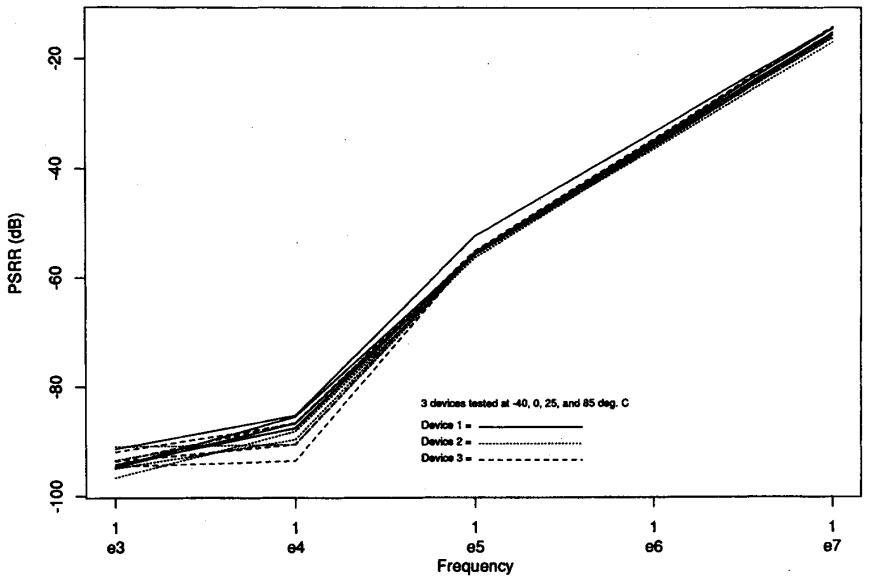

Fig. 6. Variation of PSRR with frequency.

$M3$, and the offset voltage of the amplifier. The mismatch between $Q1$ and $Q2$ as well as the mismatch between $M1$ and $M2$ affect the effective value of M. The mismatch between $M1$ and $M3$ affects the value of N. The amplifier offset can be represented by a voltage source in series with the gate terminal of $M4$. Denoting this as V_{os}, the expression for the bandgap voltage can be rewritten as

$$\text{VBG} = V_{BE2} + N\frac{R2}{R1}(V_T \ln[M(N+1)] + V_{os}). \quad (10)$$

In practice the values of M, N, and $R2/R1$ can be assured to be accurate within about 1%. It can be shown that their net rms contribution to the variation of the bandgap voltage can easily be limited about 10 mV. However, the amplifier offset voltage which is multiplied by the factor $N(R2/R1)$, can result in a significantly larger variation in VBG. There are two components in the offset voltage; a systematic component due to the channel length modulation in the current mirrors and a random component due to threshold and geometry mismatches between $M4$ and $M5$ and between $M10$ and $M8$. The systematic component can be minimized by using cascode mirrors. The random component can be minimized by making transistors $M8$ and $M10$ much smaller than $M4$ and $M5$ (this makes the latter pair the dominant contributors) and by careful layout. In applications where the absolute value of the voltage is very critical, a wafer level trim technique can be used. This is invariably done in most high precision analog circuits.

The main contributors to the noise in the bandgap voltage output are the thermal noise of $R1$ and $R2$ and the input referred noise of the amplifier. These can all be represented by a single noise voltage source that has exactly the same effect as V_{os} in (10). The noise performance of this circuit is similar to that of conventional bandgap voltage generators.

TABLE I
MEASURED PERFORMANCE OF BANDGAP CIRCUIT

Parameters	Measurement
Temperature(C)	-40 to 85
Power supply range(V)	2.7 to 5.5
Power dissipation(mW)	1.0
Mean Idd (uA)	300
Mean V_{BG}(V)	1.236
Standard deviation(mV)	20
Temperature coefficient(ppm/C)	85
PSRR(dB)	
@1KHz	-95
@10KHz	-80
@100KHz	-55
@1MHz	-40

V. EXPERIMENTAL RESULTS

The bandgap circuit (including the enhancement of Fig. 3) has been implemented in a 0.9 micron digital CMOS process. The photomicrograph of the device is shown in Fig. 4. It occupies an area of 0.07 mm^2 and consumes just 1 mW. Performance of 10 devices were measured over a range of power supply voltages and temperatures from 0–85°C. Three of the devices were characterized down to −40°C. The results are summarized in Table I. The bandgap voltage has a standard deviation of 20 mV with no trimming. The temperature dependence is shown graphically in Fig. 5. The typical temperature coefficient is 85 ppm/°C. The variation of PSRR with frequency is shown in Fig. 6. It can be seen that the PSRR is close to 95 dB at low frequencies and remains better than 40 dB up to 1 MHz.

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