An Unconditionally Stable Two-Stage CMOS Amplifier

Richard J. Reay and Gregory T. A. Kovacs

Abstract— **This paper describes a two-stage CMOS amplifier that is stable for any capacitive load. This is achieved through the use of an optimized cascoded compensation topology. A new level shifting technique allows independent optimization of drive capability, noise and systematic offset voltage. The circuit is 0.1 mm^2 in a 2 μm technology and has a quiescent current consumption of 110 μA.**

I. Introduction

In the last few years there has been an effort to integrate electrochemical instrumentation [1]–[3]. A critical component of such a system is an amplifier capable of driving a wide range of capacitive loads, typically from 10 pF to 100 nF. The amplifier must also drive resistive loads (>50 kΩ) with a low input referred offset voltage, and thus a single stage topology cannot be used. Since it is part of a larger system, the amplifier should also be power and area efficient. Many CMOS buffer designs have been reported, but most are not suitable for this application because of limited capability for driving large capacitive loads [4], small capacitive loads [5], or having high power dissipation [6]–[8], large area [9]–[11], or low gain [5], [12].

This paper presents an efficient two-stage amplifier that is stable for any capacitive load. By using cascoded compensation with optimized circuit parameters, the worst case phase margin of the amplifier can be controlled to acceptable values. In two-stage CMOS amplifiers, there is usually a trade-off among high output drive capability, low noise and low systematic offset voltage. This amplifier uses a level shifting circuit between the first and second gain stages to eliminate this compromise and allow independent optimization of these attributes.

The next section of this paper discusses the stability of a two-stage amplifier for varying capacitive loads and presents an approach for controlling the worst case phase margin. The trade-offs in two-stage amplifier design are then described in Section III, and the design of a level shifting circuit is presented in Section IV. The experimental results of the amplifier are summarized in Section V.

II. Optimizing Stability

Cascoded compensation is a common technique for compensating two-stage CMOS amplifiers [14]. Compared to simple RC compensation, cascoded compensation improves the capacitive load capability and power supply rejection. Fig. 1 shows a typical circuit configuration and its ac equivalent model. The open loop gain of the amplifier is given by (1) shown at the bottom of the next page assuming that g_{m3} is much larger than g_{m1} and g_{m2}. If that is not a valid assumption, there is also a zero at $s = -g_{m3}/C_c$ and a third high frequency pole, but these roots only complicate the equations and do not fundamentally alter the results and conclusions presented below. In the simplified model described by (1), the two poles are real and widely spaced. Their locations are approximately equal to

$$p_1 = -\frac{1}{R_1C_1 + R_2(C_C + C_L) + g_{m2}R_2R_1C_C} \tag{2}$$

$$p_2 = -\frac{R_1C_1 + R_2(C_C + C_L) + g_{m2}R_2R_1C_C}{R_1R_2C_1(C_C + C_L)}. \tag{3}$$

For small values of load capacitance, C_L, these equations simplify to the familiar values of

$$p_1 \approx -\frac{1}{g_{m2}R_2R_1C_C} \tag{4}$$

$$p_2 \approx -\frac{g_{m2}C_C}{C_1(C_C + C_L)}. \tag{5}$$

As C_L is increased, the nondominant pole decreases in frequency while the dominant pole remains fixed, thereby lowering the phase margin of the amplifier. If C_L is increased further, so that it is much larger than $g_{m2}R_1C_C$, the pole locations become

$$p_1 \approx -\frac{1}{R_2(C_C + C_L)} \tag{6}$$

$$p_2 \approx -\frac{1}{R_1C_1}. \tag{7}$$

Notice that as C_L increases, the nondominant pole becomes fixed and the dominant pole starts to decrease in frequency. As the distance between the poles increases, the phase margin of the amplifier improves and the amplifier becomes more stable. Therefore, for increasing capacitive load the amplifier phase margin initially decreases, reaches some minimum value, and then increases again. This is evident in Fig. 2, which shows a simulation of the phase margin versus C_L for the complete amplifier circuit described by this paper.

To predict the stability of the amplifier it is important to understand which circuit parameters determine the minimum phase margin. Consider a stability quality factor $S \equiv p_2/\mathrm{GBW}$, where GBW is the amplifier gain-bandwidth product. A large value of S corresponds to a large phase margin, and a small value of S corresponds to a small phase margin. The minimum amplifier phase margin will occur at the

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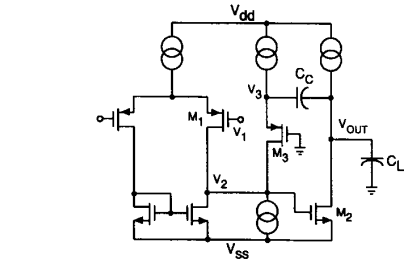
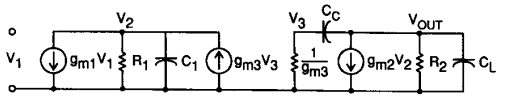


(a)



(b)

Fig. 1. (a) Typical implementation of cascoded compensation. (b) Equivalent ac circuit model.

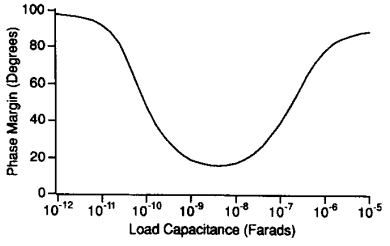


Fig. 2. Simulation of phase margin versus C_L for the circuit in Fig. 5.

minimum value of S which is calculated below:

$$\frac{\partial S}{\partial C_L} = \frac{\partial}{\partial C_L}\left[\frac{(R_1C_1 + R_2(C_C + C_L) + g_{m2}R_2R_1C_C)^2}{g_{m1}g_{m2}R_1^2R_2^2C_1(C_C + C_L)}\right] = 0. \tag{8}$$

Solving this for C_L^*, the load capacitance at S_{MIN}, gives

$$C_L^* \approx (g_{m2}R_1 - 1)C_C. \tag{9}$$

Substituting this back into the equation for S gives

$$S_{\text{MIN}} = \frac{4}{g_{m1}R_1}\frac{C_C}{C_1}. \tag{10}$$

For good amplifier performance over a wide range of C_L, S_{MIN} should be made as large as possible. One way to do this is to reduce the first stage gain of the amplifier. Unfortunately this also increases the amplifier's offset and noise and lowers the overall amplifier gain, so $g_{m1}R_1$ reduction is limited. The ratio C_C/C_1 on the other hand can be made quite large by minimizing C_1 in the layout and by increasing the compensation capacitance. In the latter case, the value of g_{m3} should also be increased to maintain

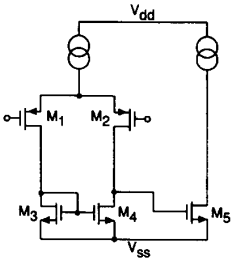


Fig. 3. Typical two-stage CMOS amplifier.

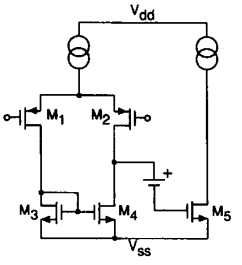


Fig. 4. Two-stage CMOS amplifier with level shifter.

a constant zero location. For the circuit simulated in Fig. 2, $g_{m1}R_1 \approx 160$ and $C_1 \approx 0.5$ pF.

This result was derived using a simplified two-pole model for the amplifier, but detailed simulations and experimental results show that the implications of (10) are valid for realistic circuits. By selecting proper component values it is possible to keep the phase margin above an arbitrary value for any capacitive load.

III. Two-Stage Amplifier Trade-Offs

A two-stage CMOS amplifier generally has the topology shown in Fig. 3. In order to have good output drive capability, g_{m5} needs to be made large, and thus the channel length of M_5 should be as small as possible. For good $1/f$ noise performance, the channel lengths of M_3 and M_4 should be fairly large, since the input referred $1/f$ noise of the amplifier is given by [15]

$$V_{1/f}^2 = \frac{2K_p}{W_1L_1C_{\text{ox}}}\left(1 + \frac{K_n\mu_n}{K_P\mu_P}\left(\frac{L_1}{L_4}\right)^2\right)\left(\frac{\partial f}{f}\right). \tag{11}$$

Unfortunately, if the channel lengths of M_4 and M_5 are widely different and their bias current densities are similar, V_{GS4} and V_{GS5} will have different nominal values, causing a systematic offset voltage. Therefore there is a fundamental trade-off among high capacitive load drive, low noise, and low offset voltage.

A solution that avoids compromising one of these three parameters is to add a level shifting circuit between the two

$$\frac{g_{m1}g_{m2}R_1R_2}{1 + s(R_1C_1 + R_2C_C + R_2C_L + g_{m2}R_2R_1C_C) + s^2R_1R_2C_1(C_C + C_L)} \tag{1}$$

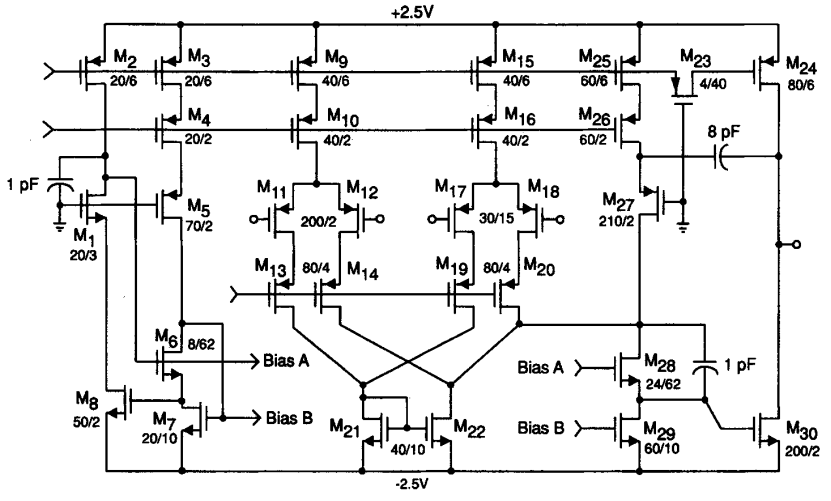


Fig. 5. Complete schematic of the amplifier.

stages, as shown in Fig. 4. The level shifter compensates for the different nominal values of V_{GS} that result from making L_5 small and L_4 large. The result is that the current densities in M_4 and M_5 have the proper ratio, and the systematic offset voltage is reduced. A concern with this technique is that the level shifter voltage must track the other circuit parameters over temperature and processing variations for good performance.

IV. Level Shifter Technique

The level shifter is realized with an n-channel device, M_{28}, biased in the linear region. It is incorporated into the stack of transistors used for cascoded compensation, as shown in Fig. 5. The bias for M_{28} is generated by a replica bias circuit, M_1 through M_8. Transistors M_2 to M_8 are scaled-down copies of the compensation and output transistors, M_{24} to M_{30}. Devices M_7, M_{22}, and M_{29} also are matched. The replica circuit adjusts the bias on the linear device M_6, so that the currents in M_2 and M_8 are equal. This also means that M_{28} is properly biased to make I_{DS24} and I_{DS30} nominally equal, making the systematic offset of the amplifier zero.

Due to the replica circuit, Bias A is automatically adjusted to the correct value over changes in temperature, supply voltage and processing. A 1 pF speed-up capacitor bypasses the level shifter at high frequencies to improve the amplifier phase margin. The amplifier has dual input stages for reducing charge-injection errors in a switched capacitor circuit [3], [16].

V. Experimental Results

The amplifier in Fig. 5 was fabricated in a commercial 2 μm CMOS process. The die area is 0.1 mm^2 and the supply current is 110 μA. Based on a sample of 12 parts, the systematic offset voltage is -150 μV, demonstrating the effectiveness of the level shifting circuit. As the capacitive load was increased, the measured phase margin initially decreased, reached a minimum value at about 1 nF and then increased again, as described in Section II. Fig. 6 shows the unity-gain closed loop step response for three different capacitive loads. For $C_L = 1$ nF, which gives the worst case phase margin, there is significant overshoot and ringing, but the amplifier settles within 5 μs. At $C_L = 100$ nF, there is no ringing, showing the improvement in stability, but positive slew-rate limiting due to the class-A output stage is noticeable. The noise of the amplifier is dominated by $1/f$ noise and is fairly high due to the poor $1/f$ noise of the process used.

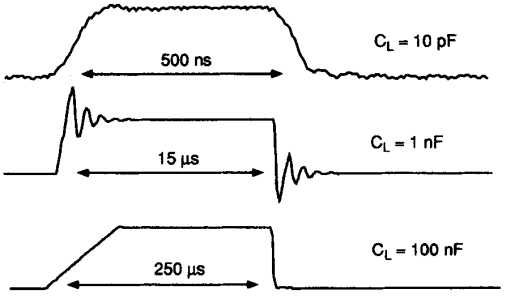


Fig. 6. Unity-gain step response for three values of C_L. The input pulse height in all cases is 50 mV.

This amplifier was optimized to be an integrator in electrochemical instrumentation applications, which are quite slow and can tolerate long settling times. Therefore, the minimum phase margin was designed to be 20°, and a simple class-A output stage was used. For higher speed applications, the settling time could be reduced by increasing the minimum phase margin, and the slew rate could be made symmetrical by using a class-AB output stage. The amplifier performance is summarized in Table I.

VI. Conclusion

The design of a two-stage CMOS amplifier that is stable for any capacitive load has been described. To achieve uncon-

TABLE I
SUMMARY OF AMPLIFIER PERFORMANCE.
$V_{DD} = +2.5$ V, $V_{SS} = -2.5$ V FIG. 1(a) AND (b)

Parameter	Measured Value
Input offset voltage, $\overline{\mu}$	-150 μV
Input offset voltage, σ	2.1 mV
Open-loop gain	80 dB
Unity-gain frequency	4.5 MHz, $C_L = 10$ pF 1.3 MHz, $C_L = 1$ nF 120 kHz, $C_L = 100$ nF
Phase margin	65°, $C_L = 50$ pF
Input noise density @ 1 kHz	158 nV/$\sqrt{\text{Hz}}$
DC power dissipation	550 μW

ditional stability, optimized cascoded compensation is used. The circuit parameters that determine the worst case amplifier stability were identified and optimized for the requirements of electrochemical instrumentation. A new level shifting topology eliminates the fundamental trade-off among high capacitive load drive, low noise, and low offset voltage in a two-stage amplifier.

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