Resistive Interpolation Biasing: A Technique for Compensating Linear Variation in an Array of MOS Current Sources

Srinagesh Satyanarayana and Ken Suyama

Abstract—**A new technique called resistive interpolation biasing for accurately biasing a large number of analog cells on a VLSI chip is presented. Variations in oxide thickness, mobility, doping concentration, etc., cause inaccuracies in current ratios of two identically biased transistors if they are placed sufficiently far apart on a chip. The proposed technique compensates for these inaccuracies without using any sampling or switching. The technique has been verified using a 2 μm n-well CMOS process. Measurements show a factor of 3 improvement in terms of current ratio accuracy when the resistive interpolation technique is used. The circuit can be implemented with a small chip area and low power dissipation. This technique finds applications where extensive current duplication over a large area is required (e.g., analog memories, D/A converters, continuous-time filters, imaging arrays, neural networks, and fuzzy logic systems).**

I. Introduction

A COMMON technique employed in most analog systems today is to take advantage of good matching between two identical transistors placed close to each other and biased similarly, for implementing current mirrors. However, when a large number of transistors have to carry the same current, it becomes impossible to take advantage of the matching by proximity of placement. One reason for the mismatch stems from process variations in MOSFET parameters (doping concentration, oxide thickness, mobility, etc.) [1], [2]. This is the problem addressed in this paper. The other problem is due to random fluctuations in the edges of the transistors which do not depend on the spacing between the transistors.

II. Existing Techniques

Several techniques for improving the accuracy of current mirrors have been suggested [3]–[8]. In the current calibration technique [4], [5] each bias transistor is first calibrated against a fixed reference and then used for biasing the analog cell. The disadvantage of such schemes is that frequent calibration is necessary and the circuit to be biased has to be taken off-line during calibration. Techniques to solve the latter problem have been developed by using an extra calibration cell [5], [6]. However, the need to switch the bias currents and to supply control signals to the switches and the op-amp feedback adds complexity and extra chip area. This technique can compensate any form of mismatch as long as an appropriate V_{GS} can be found for the desired value of current by the feedback configuration. When arbitrary ratios of a reference current have to be generated, the process of comparing it to the reference also becomes a problem. One solution commonly used is to employ a digital memory and a D/A converter to generate arbitrary values of reference current sources [9], [10]. A digital memory stores the values of the individual current source values (or the corresponding gate to source voltages). This solution is expensive in terms of chip area and circuit complexity.

A hierarchical current mirror scheme is sometimes used to generate accurate bias currents [3]. This technique restricts current mirroring to a small number of copies. When a current value has to be copied over large distances, a long wire carrying the suitable value of current is used to supply the reference. Although arbitrary current ratios can be generated by this technique, one individual wire must be routed from each current mirror pool to the reference current source, resulting in large chip area. This technique is only efficient for biasing a small number of current mirror pools distributed over a chip.

An extension of the popular cross coupling technique [11] used to minimize the input offsets in differential pairs of high gain opamps and comparators can also be utilized to improve matching in current mirrors. Extending the technique, several authors [5], [7], [8] have reported a technique to compensate for graded and symmetrical errors. Each current source required by the D/A converter is split into several parts depending on the value of the current. These individual parts are placed on either sides of the center of the row (or column) thereby improving the accuracy of the current matching.

III. Resistive Interpolation Biasing (RIB)

The resistive interpolation biasing (RIB) technique shown in Fig. 1 involves modifying the basic current mirror scheme [12] by adding two reference generators (M_{0A} and M_{0B}) and an interpolating resistor. The new circuit generates a pre-compensating bias voltage at the gate of each bias transistor (M_i) which is adequate to cancel the linear part of the variations in all the parameters that influence the drain current. A source follower is used at the gate of each reference transistor to ensure that interpolating resistor current is not drawn from the reference current sources.

Consider a row of transistors $(M_{0A}, \cdots, M_i, \cdots, M_{0B})$ placed at distances $x_A, \cdots, x_i, \cdots, x_B$ respectively from an arbitrary reference point as shown in Fig. 1. Since the MOS transistor parameters vary with distance along a chip, we can express each MOS parameter as a function of distance x_i.

Manuscript received July 16, 1994; revised December 15, 1994.

S. Satyanarayana is with Philips Laboratories, Briarcliff Manor, NY 10510 USA.

K. Suyama is a Research Scientist, Department of Electrical Engineering, Columbia University, New York, NY 10027 USA.

IEEE Log Number 9410187.

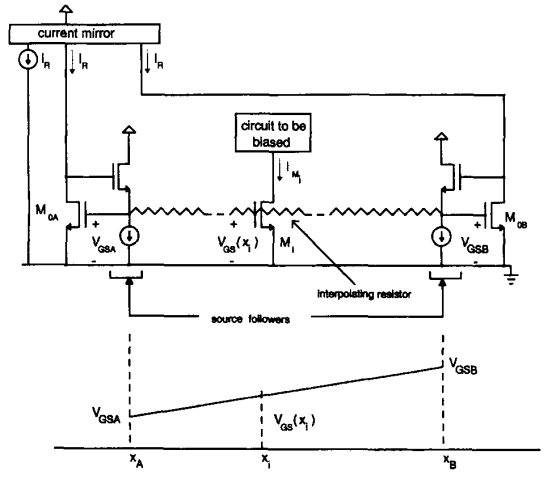

Fig. 1. Circuit realization of the RIB technique.

Since all the transistors in the circuit are along a row, we can ignore the variations in the direction perpendicular to x_i. For example the parameter ρ at a distance x_i from the arbitrary point of reference, can be expressed using Taylor's series as

$$\rho(x_i) = \rho(x_A)\left(1 + \frac{\partial \rho}{\partial x}(x_i - x_A) + \text{higher order terms}\right). \tag{1}$$

The currents in each of these transistors will depend on the value of the individual MOS parameters [13] at the location of the transistor. Hence we can express the current as a function of distance as follows

$$\begin{aligned} I_{M_i} &= I(x_i) \\ &= f[V_{\mathrm{GS}}(x_i), \mu_N(x_i), N_A(x_i), \cdots, V_T(x_i), C'_{\mathrm{ox}}(x_i)] \end{aligned} \tag{2}$$

where V_{GS} is the gate to source voltage, μ_N is the mobility, N_A is the doping, V_T is the threshold voltage, and C'_{ox} is the oxide capacitance per unit area. We assume that all the transistors have the same V_{DS}, and hence channel length modulation effects will not cause errors in the current mirrors. Implicit in the assumption is the fact that we are using long channel devices, and as a result, the variation in the early voltage parameter with distance is insignificant. In a later section we discuss the variation of the early voltage with distance for short channel devices. Ensuring that the V_{DS} is identical by using cascode techniques, provides increased current matching accuracy at the cost of decreased voltage swing for the current sources. The drain current at any point can be expressed as a function of the distance x using Taylor's series. Neglecting the higher order terms, the drain current can be expressed as

$$I(x) = I(x_A) + \frac{\partial I}{\partial x}(x - x_A) \tag{3}$$

where $I(x_A)$ is the current in transistor M_{0A} and $\partial I/\partial x$ is constant since we are neglecting the higher order terms. Differentiating (2) with respect to x we get

$$\begin{aligned} \frac{\partial I}{\partial x} = \frac{\partial I}{\partial V_{\mathrm{GS}}}\frac{\partial V_{\mathrm{GS}}}{\partial x} + \frac{\partial I}{\partial \mu_N}\frac{\partial \mu_N}{\partial x} + \frac{\partial I}{\partial N_A}\frac{\partial N_A}{\partial x} + \cdots \\ + \frac{\partial I}{\partial V_T}\frac{\partial V_T}{\partial x} + \frac{\partial I}{\partial C'_{\mathrm{ox}}}\frac{\partial C'_{\mathrm{ox}}}{\partial x}. \end{aligned} \tag{4}$$

The same reference current I_R is supplied to the two reference current sources M_{0A} and M_{0B},

$$I(x_A) = I_R \tag{5}$$

$$I(x_B) = I_R, \tag{6}$$

and the resulting V_{GS} values ($V_{\mathrm{GS}A}$ and $V_{\mathrm{GS}B}$) are fed to the ends of the interpolating resistor string. Since source follower buffers are used at each of the reference current sources, the resistor string can be viewed as having two voltage sources of value $V_{\mathrm{GS}A}$ and $V_{\mathrm{GS}B}$ at its ends. A linear gradient in V_{GS} is set up along the resistor string. The gradient can be expressed as

$$\frac{\partial V_{\mathrm{GS}}}{\partial x} = \frac{V_{\mathrm{GS}B} - V_{\mathrm{GS}A}}{x_B - x_A}. \tag{7}$$

Errors resulting from variations in the resistivity of the string are considered as second order effects and hence will be ignored in the following analysis. The current at the reference transistor M_{0B} can be expressed as

$$I(x_B) = I(x_A) + \frac{\partial I}{\partial x}(x_B - x_A). \tag{8}$$

Substituting (5) and (6) in (8) we get

$$\frac{\partial I}{\partial x} = 0. \tag{9}$$

Substituting (9) in (4) we get

$$\begin{aligned} \frac{\partial I}{\partial V_{\mathrm{GS}}}\frac{\partial V_{\mathrm{GS}}}{\partial x} = -\left[\frac{\partial I}{\partial \mu_N}\frac{\partial \mu_N}{\partial x} + \frac{\partial I}{\partial N_A}\frac{\partial N_A}{\partial x} + \cdots \right. \\ \left. + \frac{\partial I}{\partial V_T}\frac{\partial V_T}{\partial x} + \frac{\partial I}{\partial C'_{\mathrm{ox}}}\frac{\partial C'_{\mathrm{ox}}}{\partial x}\right]. \end{aligned} \tag{10}$$

Equation (10) implies that the value of $\partial V_{\mathrm{GS}}/\partial x$ obtained by forcing equal currents in M_{0A} and M_{0B} and feeding the resulting V_{GS} values to the ends of the interpolating resistor, cancels the linear variation in current due to all the remaining MOS parameters. Using (9) and (5) in (3) we obtain

$$I(x) = I_R.$$

For each bias transistor, the voltage at tap i of the resistor string represents the appropriate V_{GS} for exactly compensating the current mismatch caused by the linear parameter variation along the x direction.

In the above circuit long channel transistors were used and the channel length modulation was ignored. For short channel transistors this assumption is not valid. Hence the variation in the early voltage has to be considered. The gradient of current

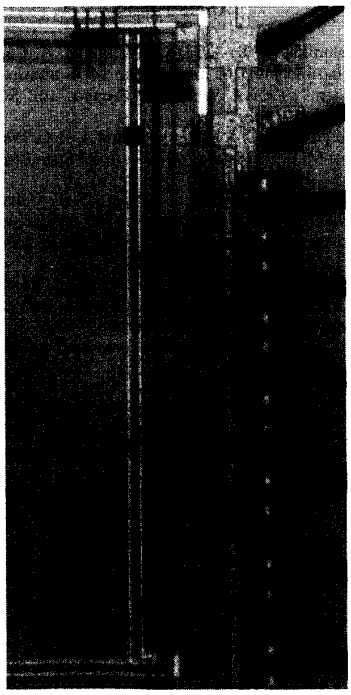

Fig. 2. Photomicrograph of the RIB circuit.

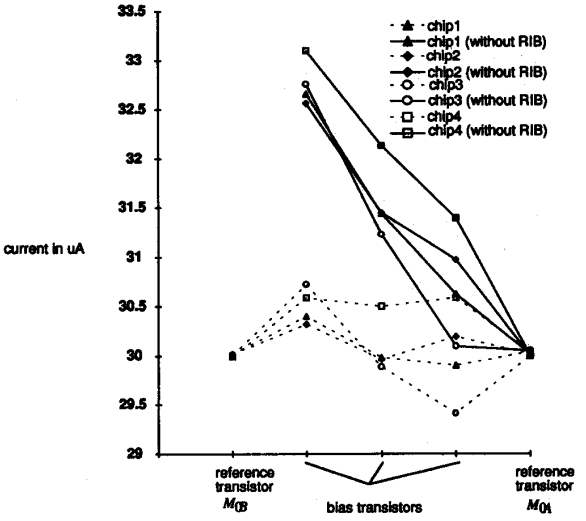

Fig. 3. Measured results on the chip with and without RIB. $W/L = 38.4\,\mu\text{m}/3.6\,\mu\text{m}$ for the bias transistors. $V_{\text{GS}} = 1.358$ V for M_{0A} and $V_{\text{GS}} = 1.336$ V for M_{0B}.

with respect to V_{DS} and the early voltage should be included in (2). If V_{DS} is forced to be the same for all transistors, one of the terms, namely, $\partial V_{\text{DS}}/\partial x$ becomes zero. Thus an error is introduced in the compensating voltages computed using (10). To overcome this problem, an intentional gradient can be introduced in V_{DS} using two reference generators and another interpolating resistor string.

IV. Implementation

A PMOS based RIB scheme was implemented on a chip to test the concept. Fig. 2 shows the photomicrograph of the chip. The resistor was implemented using a p-diffusion strip. Diffusion layer was chosen since it provides a reasonable value of sheet resistance (70 Ω per square). The resulting resistance for a 2.4 μm wide diffusion resistor string for 1000 μm's of length is approximately 30 kΩ. If the voltage mismatch between the reference sources is 300 mV, then the current in the diffusion wire will be less than 10 μA. If a lower resistivity material like poly or metal is used, the current in the resistor will be large and the source follower buffers have to be designed to handle the necessary current.

The two reference currents were supplied externally. Three bias transistors were placed with a spacing of 367 μm between adjacent bias transistors. After setting the currents in the reference transistors to identical values, the current in each bias transistor was measured. Drain voltages of all bias transistors were maintained at the same value as the drain voltage of the reference transistor M_{0A}. The experiment was repeated with and without the RIB scheme. The results are shown in Fig. 3. The bias currents are plotted with distance from one of the reference transistors. The error in the bias current decreased by a factor of 3 when the RIB circuit was activated.

V. Applications of the New Biasing Technique

This technique has potential applications when a large number of current sources with arbitrary values are needed, in applications where continuous-time operation is required, and when chip area and power dissipation are issues of concern. Current-mode D/A and A/D converters require a large number of current sources [7], [8] matched to certain degree (depending on resolution requirements) of accuracy. Although the current sources must be binary weighted, they are constructed from identical current sources.

In continuous-time filters [14] bias voltages are generated not by a reference current source but by a tuning loop and a reference filter/oscillator cell. Following the generation of these voltages, they are distributed to identical (in topology) filters which could be placed anywhere on the chip. Normally transistors being tuned in each cell are grouped together in one area of the chip. The RIB technique would make it possible to retain each transistor inside the filter/oscillator cell and hence simplify layout and reduce wiring area. It might also help in reducing crosstalk between cells.

Fig. 4 shows an application of the RIB technique to bias an array of cells. One application where an array of cells has to be biased with current sources of arbitrary values is a neural network [15]. A major issue in implementing neural networks is the realizations of synaptic weights [9]. In a neural network with fixed weights, the aspect ratios of the transistors in the synapse determine the weights. In the figure we show a transconductance synapse where the weight value is determined by the aspect ratio of M_{i1}. Each bias transistor M_{i1} in the synapse has to be biased with an appropriate voltage to generate a current for the respective synapse. The RIB technique is ideal for this application. Fig. 4 shows how

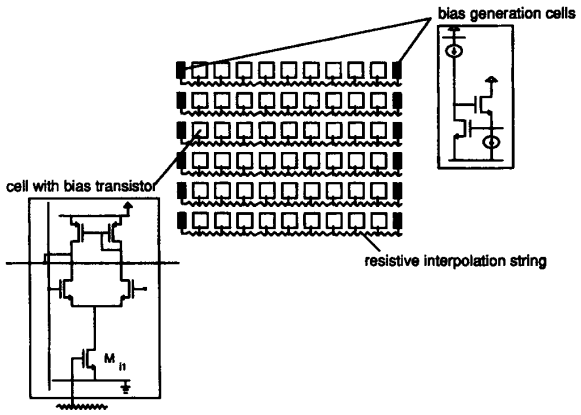

Fig. 4. Application of RIB to an array of analog cells.

the resistive string is passed through each synapse to provide the precompensated bias voltage. Similar applications can be found in analog memories [16], [17] fuzzy rule processors [18], and imaging arrays [19].

VI. Conclusion

A new technique has been developed for biasing circuits in VLSI chips where a large number of analog cells have to be biased accurately. This technique compensates for the current mismatch due to the linear gradient of all MOS parameters. While it is a very efficient technique to compensate for global variations over a chip, it cannot compensate for variations in devices placed close to each other. The technique does not involve an op-amp or any switching, and is area efficient. This technique is also applicable for generating arbitrary current mirror ratios that are usually necessary in applications like neural networks and analog memories.

Acknowledgment

The authors would like to thank Y. Tsividis for his constructive suggestions and comments. This project was supported by Philips Laboratories.

References

[1] K. R. Lakshmikumar, R. A. Hadaway, and M. A. Copeland, "Characterization and modeling of mismatch in MOS transistors for precision analog design," *IEEE J. Solid-State Circuits*, vol. SC-21, no. 6, pp. 1057–1066, Dec. 1986.

[2] M. J. M. Pelgrom, A. C. J. Duinmaijer, and A. P. G. Welbers, "Matching properties of MOS transistors," *IEEE J. Solid-State Circuits*, vol. 24, no. 5, pp. 1433–1440, Oct. 1989.

[3] C. A. Laber, C. F. Rahim, S. F. Dreyer, G. T. Uehara, P. T. Kwok, and P. R. Gray, "Design considerations for a high-performance 3-μm CMOS analog standard-cell library," *IEEE J. Solid-State Circuits*, vol. SC-22, no. 2, pp. 181–189. Apr. 1987.

[4] S. J. Daubert, D. Vallancourt, and Y. P. Tsividis, "Current copier cells," *Electron. Lett.*, vol. 24, no. 25, pp. 1560–1562, Dec. 8, 1988.

[5] H. J. Schouwenaars, D. W. J. Groeneveld, and H. A. H. Termeer, "A low-power stereo 16-bit CMOS D/A converter for digital audio," *IEEE J. Solid-State Circuits*, vol. 23, no. 6, pp. 1290–1297, Dec. 1988.

[6] C. Toumazou, F. J. Lidgey, and D. G. Haigh, *Analog IC Design: The Current-mode Approach*. U.K., Peter-Peregrinus, Ltd., 1990.

[7] Y. Nakamura, T. Miki, A. Maeda, H. Kondoh, and N. Yazawa, "A 10-b 70-MS/s CMOS D/A converter," *IEEE J. Solid-State Circuits*, vol. 26, no. 4, pp. 637–642, Apr. 1991.

[8] C. A. A. Bastiaansen, D. W. J. Groeneveld, H. J. Schouwenaars, and H. A. H. Termeer, "A 10-b 40-MHz 0.8-m CMOS current-output D/A converter," *IEEE J. Solid-State Circuits*, vol. 26, no. 7, pp. 917–921, July 1991.

[9] Y. Horio and S. Nakamura, "Analog memories for VLSI neurocomputing," in *Artificial Neural Networks Paradigms Applications and Hardware Implementations*. IEEE Press, 1992.

[10] Y. P. Tsividis and S. Satyanarayana, "Analogue circuits for variable-synapse electronic neural networks," *Electron. Lett.*, vol. 23, no. 24, pp. 1313–1314, 1987.

[11] R. L. Geiger, P. E. Allen, and N. R. Strader, *VLSI Design Techniques for Analog and Digital Circuits*. New York: McGraw-Hill, 1990.

[12] P. R. Gray and R. G. Meyer, *Analysis and Design of Analog Integrated Circuits*. New York: Wiley, 1984.

[13] Y. P. Tsividis, *Operation and Modeling of the MOS Transistor*. New York: McGraw-Hill, 1987.

[14] Y. P. Tsividis and J. O. Voorman, *Integrated Continuous-Time Filters: Principles, Design, and Applications*. IEEE Press, 1993.

[15] S. Satyanarayana, "Analog VLSI implementation of reconfigurable neural networks," Ph.D. dissertation, Columbia University, New York, NY, 1991.

[16] E. Franchi, M. Tartagni, R. Guerrieri, and G. Baccarani, "Random access analog memory for early vision," *IEEE J. Solid-State Circuits*, vol. 27, no. 7, pp. 1105–1109, July 1992.

[17] F. Goodenough, "IC holds 16 seconds of audio without power," *Electronic Design*, pp. 39–44, Jan. 31, 1991.

[18] T. Yamakawa, "A silicon inference engine in nonlinear analog mode and its application to a fuzzy logic control," *IEEE Trans. Neural Networks*, vol. 4, no. 3, pp. 496–522, May 1993.

[19] C. Mead, *Analog VLSI and Neural Systems*. Reading, MA: Addison-Wesley, 1989.