A Low-Voltage Switched-Current Delta-Sigma Modulator

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Abstract—**This paper presents the design of a fully differential switched-current delta-sigma modulator using a single 3.3-V power-supply voltage. At system level, we tailor the modulator structure considering the similarity and difference of switched-capacitor and switched-current realizations. At circuit level, we propose a new switched-current memory cell and integrator with improved common mode feedback, without which low power-supply-voltage operation would not be possible. The whole modulator was implemented in a 0.8-μm double-metal digital CMOS process. It occupies an active area of 0.53 $\times$ 0.48 mm^2 and consumes a current of 0.6 mA from a single 3.3-V power supply. The measured dynamic range is over 10 b.**

I. Introduction

SWITCHED-CURRENT (SI) delta-sigma (Δ-Σ) modulators are attractive to realize interfaces (analog-to-digital and digital-to-analog converters) for mixed analog/digital systems in standard digital CMOS process [1], [2], because SI Δ-Σ modulators take the advantages of both the Δ-Σ modulation [3] and the SI techniques [4].

A transistor-only current-mode Σ-Δ modulator has been proposed [5]. But the circuits utilized high-gain stages like in switched-capacitor (SC) circuits, thereby losing the power and area advantages of SI circuits. An SI sigma-delta modulator has also been proposed [6]. Since there were not delays in both integrators, the settling of the two integrators and the comparator coupled with each other. They had to settle within their final values during the same clock phase and thus the high-frequency operation degraded. Another drawback was that a *fully* differential structure was not employed. The differential realization was achieved only by hardware replica without common mode feedback (CMFB). The rejection of common-mode signals was poor. More recently, a second-order SI modulator by cascading two first-order stages was proposed [7], but its serious drawback was the requirement of matching between digital and analog circuits as pointed out in [3]. The SI modulator in [8] was not optimum since the two integrators had different ranges of signal swing.

In this paper, we present the design of a fully differential second-order SI Δ-Σ modulator using a single 3.3-V power-supply voltage. Following this introduction, Section II describes the modulator structure tailored for SI realization. Section III presents the fully differential SI memory cell and integrator with improved CMFB. Section IV outlines other modulator subcircuits and practical issues concerning SI design and implementation. Section V presents experimental results. Discussions and conclusions are given in Section VI.

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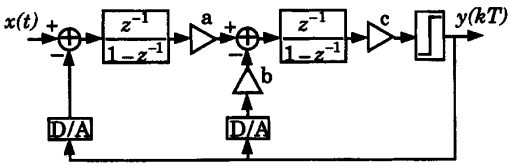


Fig. 1. Modulator structure.

II. Modulator Structure

The architecture of this delta-sigma modulator is based on former works [3], [9] that have documented the favorable stability and component tolerance characteristics of a second-order modulator. It consists of two discrete time integrators, a current quantization circuit, and a pair of current output D/A converters, as shown in Fig. 1. The integrator transfer function in this structure differs from those used in [6] by having delays from input to output. Thus, the two integrators and comparator do not settle during the same clock phase.

In an SC integrator, the scaling factor is directly realized by changing the ratio of the integration capacitor and the sampling capacitor. However, in an SI integrator, integration and scaling are done separately. Scaling can either precede or follow integration. A scaling factor before the first integrator only scales the input signal and the scaling before the second integrator is realized by changing parameters a and b. The factor c does not have any influence on the functionality because the current quantizer only detects the current direction.

In Fig. 2, we show the simulated histogram of the integrator outputs with $a = 0.5$ and $b = 1$. The input is a 1-kHz sinusoidal with an amplitude equal to half of the feedback current value and the clock frequency is 1.024 MHz. We see that both integrators have the same range of signal swing. The modulator (with $a = 0.5$ and $b = 1$) only requires a signal range in both integrators slightly larger than twice the full-scale input range (i.e., twice the output current value of the D/A converters). If we choose $a = 0.25$ and $b = 0.5$ as did in [8], the signal swing of the second integrator output will be as half as that of the first integrator. The signal range of the second integrator will not be utilized. If we choose $a = 1$ and $b = 2$ (this is exactly the case in [5], since the feedback to the second integrator is twice as large as that to the first integrator), the signal swing of the second integrator will be twice as large as that of the first integrator. The second integrator will call for a larger signal range. Therefore, the modulator with $a = 0.5$ and $b = 1$ gives the best performance concerning signal swing.

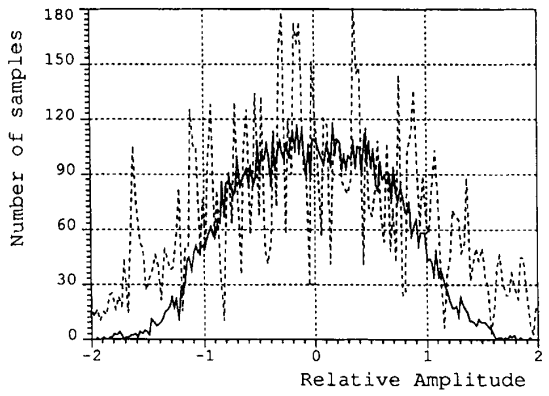


Fig. 2. Histogram of the integrator outputs. Dashed line—the first integrator output; Solid line—the second integrator output.

The choice of the scaling c has no effects on the signal swing within the integrators. It only has slight influence on the design of the current quantizer and on the output current mirror of the second integrator. Larger value of c simplifies the design of the current quantizer but needs larger current mirror. Smaller value of c means smaller current mirror as a load for the second integrator but requires better current quantizer since the input current to the quantizer is smaller. As a tradeoff, we choose $c = 1$.

III. Low-Voltage Fully Differential SI Circuits

A. Low-Voltage Memory Cell

In Fig. 3(a), we show a conventional fully differential SI memory cell [10], while in Fig. 3(b), we show the proposed low-voltage fully differential SI memory cell.

Grounded-gate amplifiers (GGA's) are used to create a "virtual ground" at the drain of the memory transistor, reducing the error introduced by finite input/output conductance ratio, and the fully differential structure reduces the clock feedthrough errors [4], [10]. The GGA consists of the grounded-gate transistor T_G and its biasing transistors. The main difference between the memory cells of Fig. 3(a) and (b) is the use of the level shifter in Fig. 3(b) consisting of a level shifting transistor T_L and its biasing transistors T_{LN} and T_{LP}. The gate voltages of the common-mode feedback transistors T_{N1} and T_{N2} are thus shifted by the value of V_{gsL} (where V_{gsL} is the gate-source voltage of T_L at the quiescent condition). Except for this difference, these two memory cells would be identical. Due to this very difference, significant improvements result.

To ensure proper operation, every transistor should operate in its saturation region. Referring to Fig. 3(a), the drain voltage of the biasing transistor T_{2J} is not set by its saturation voltage but the voltage necessary to turn on T_{N1} and T_{N2}. This larger than necessary drain voltage of T_{2J} eliminates the possibility of low-voltage operation. An inspect into the circuit of Fig. 3(a) reveals that the critical path setting the lower limit of the power supply voltage is through T_P, T_G, T, and T_N. The power supply voltage for the memory cell of Fig. 3(a) should be

$$V_{dd} \geq |(V_{gs} - V_T)_P| + |(V_{gs} - V_T)_G| + V_T + (V_{gs} - V_T)\sqrt{1 + m_i} + V_{TN} + (V_{gs} - V_T)_N\sqrt{1 + m_c} \quad (1)$$

where $(V_{gs} - V_T)_P$, $(V_{gs} - V_T)_G$, $(V_{gs} - V_T)$, and $(V_{gs} - V_T)_N$ are the quiescent saturation voltages of T_P, T_G, T, and T_N, respectively, V_T and V_{TN} are the threshold voltages of T and T_N, respectively, m_i is the differential signal modulation index (i/J) (J is the quiescent drain current of T), and m_c is the common-mode signal modulation index (i_{cm}/I_N) (I_N is the quiescent drain current of T_N).

Referring to Fig. 3(b), due to the use of the level shifter, the drain voltage of T_{2J} only needs to keep T_{2J} in the saturation region. The critical path limiting the power supply voltage is through T_P, T_G, T, and T_{2J}. The power supply voltage for the memory cell of Fig. 3(b) should be

$$V_{dd} \geq |(V_{gs} - V_T)_P| + |(V_{gs} - V_T)_G| + V_T + (V_{gs} - V_T)\sqrt{1 + m_i} + (V_{gs} - V_T)_{2J} \quad (2)$$

where $(V_{gs} - V_T)_P$, $(V_{gs} - V_T)_G$, $(V_{gs} - V_T)$, and $(V_{gs} - V_T)_{2J}$ are the quiescent saturation voltages of T_P, T_G, T, and T_{2J}, respectively, V_T is the threshold voltages of T, m_i is the differential signal modulation index (i/J).

Comparing formulas (1) and (2) it is seen that the lower limit of the power supply voltage is reduced approximately by the amount of the threshold voltage. Therefore low-voltage (3.3 V) operation is possible, given the threshold voltage about 0.8 V in standard digital CMOS process.

Due to the similarity of the two memory cells of Fig. 3(a) and (b), the design considerations of the low-voltage memory cell of Fig. 3(b) are the same as outlined in [8], [10].

B. Lossless Integrator

To construct the modulator of Fig. 1, only lossless integrators with both positive and negative integration functions are need. To save power and chip area, the GGA's and the level shifter are shared by the two memory cells. We show the lossless integrator in Fig. 4.

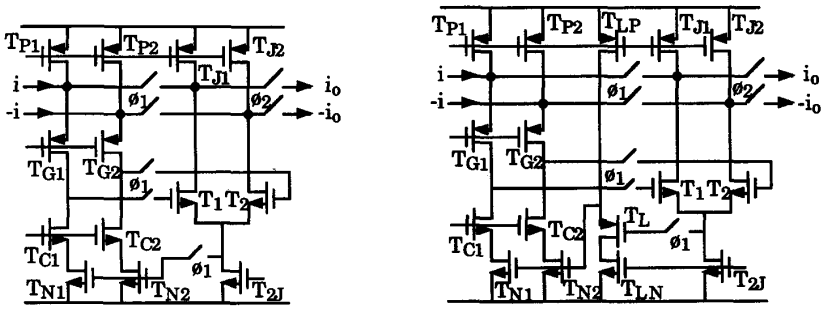
If the output current is sample during clock phase ϕ_1, the transfer function in the z-domain is given by

$$I_0(z) = \frac{\alpha_1 z^{-1}}{1 - z^{-1}} \cdot I_1(z) - \frac{\alpha_2 z^{-1/2}}{1 - z^{-1}} \cdot I_2(z). \quad (3)$$

IV. Other Modulator Subcircuits and Practical Issues

With 1-b quantization as used in this modulator, only the direction of current flow from the second integrator needs to be determined by the quantizer. A simple inverter can be used to detect the current flow direction as proposed in [6]. For fully differential current inputs, we use a two-stage voltage comparator with differential inputs as the current quantizer.

The currents from the second integrator charge or discharge the gate parasitic capacitance of the input transistors of the comparator depending on the direction of the currents. When



(a) (b)

Fig. 3. (a) Conventional fully differential SI memory cell and, (b) low-voltage fully differential SI memory cell.

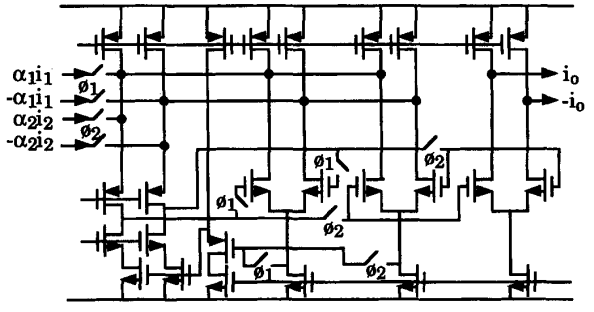


Fig. 4. Fully differential lossless integrator with CMFB.

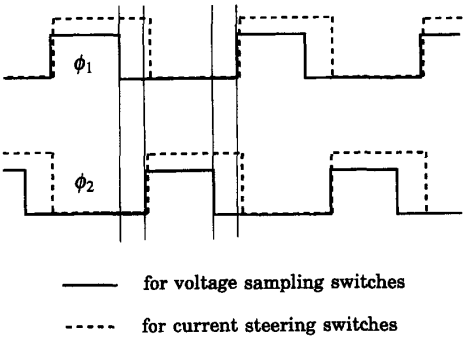


Fig. 5. Clocking strategy for SI circuits.

one branch of the differential outputs from the second integrator charges the gate parasitic capacitance of one input transistor, the other discharges the gate parasitic capacitance of the other input transistor. The voltages at the differential nodes ramp in opposite direction toward V_{dd} or zero, respectively. The differential voltage at the comparator inputs thus changes according to the direction of the current flows and the output is produced according to the differential voltage.

The D/A converters generate two equal-valued current outputs with different flowing direction according to the 1-b digital input. Current sources are the choice. Since the currents are fed to the integrators, the nodal voltages at the outputs are fixed due to the GGA's in the integrators. Thus the output currents are quite stable. Small dc offset current may exist due to process variation, but this offset does not present any serious problem for 1-b Δ-Σ modulators [3].

The use of nonoverlapping clock in second-generation SI circuits introduces circuit errors due to transient spikes [9]. A modified clocking strategy as shown in Fig. 5 can reduce transient spikes, thus minimizing the circuit errors [1], [2], [10]–[13].

Nonoverlapping phases are for voltage-sampling switches (sampling a voltage on the gate of the memory transistor) and overlapping phases are for current-steering switches (directing the current flow). And the overlapping phases (for current-steering switches) lag the nonoverlapping phases (for voltage-sampling switches). This means that current-steering switches always direct currents to low-impedance nodes formed by closing corresponding voltage-sampling switches a little bit earlier. This clocking strategy guarantees that during the circuit operation, no current will be directed to a high-impedance node. The transient spikes decrease significantly and the circuit errors due to the transient spikes are thus minimized.

To avoid open-circuiting current sources, during the clock phase when the output is not valid (not connected with following circuits), the output is connected to a low-impedance node (pseudo load). This helps reduce transient current spikes [1], [2].

V. Experimental Results

A test chip containing the SI Δ-Σ modulator of Fig. 1 was implemented in a 0.8 μ digital CMOS process. The test chip also contains a single-ended to fully differential converter at the modulator input. The photograph of the test chip is shown in Fig. 6. The whole modulator occupies an active area of 0.53 $\times$ 0.48 mm^2 and consumes a current of 0.6 mA from a single 3.3-V power supply.

To measure the performance, we use a data collector to collect data from the modulator and then use FFT to evaluate signal/noise ratio (SNR) and total harmonic distortion (THD). In Fig. 7, we show a measured power spectrum by performing a 64 K-point FFT using a blackman window. The clock frequency is 2.45 MHz and the input is a 2-kHz 3.5-μA (-5.4 dB) sinusoidal. The THD is -59 dB and the SNR is 57 dB with a band of 10 kHz.

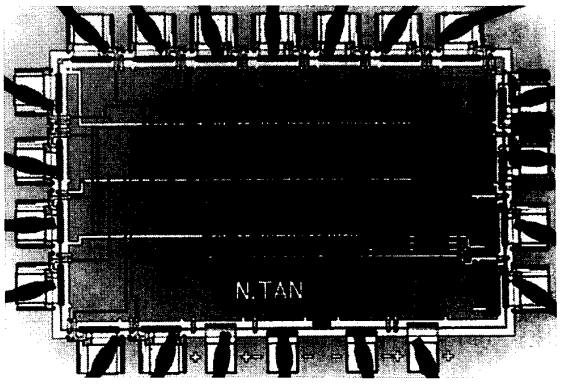


Fig. 6. The photograph of the test chip.

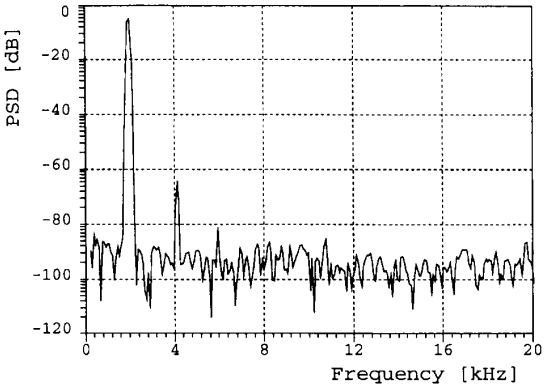


Fig. 7. Measured power spectrum. The clock frequency is 2.45 MHz and the input is a 2-kHz 3.5-μA (−5.4 dB) sinusoidal.

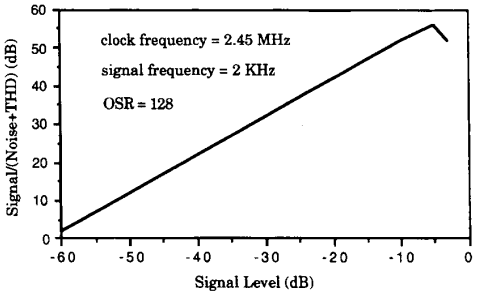


Fig. 8. Measured signal/(noise + THD) versus the input current. And the 0-dB signal level is 6.5 μA.

In Fig. 8, we show the measured signal/(noise + THD) versus the input current. The signal is a 2-kHz sinusoidal and the clock frequency is 2.45 MHz. The sinc^3 decimator with a decimation factor of 128 is used. And the 0-dB signal level is 6.5 μA. A summary of the measured results appears in Table I.

VI. Discussions and Conclusion

The dynamic range of the presented SI modulator is considerably lower than its SC counterparts. The main reason is the large thermal noise within SI circuits. The modulator would give a dynamic range about 70 dB from the calculation considering the thermal noise within the SI circuits. The 10-dB discrepancy is mainly due to the interface noise and process variation. To increase the dynamic range, we can either increase the storage capacitance to reduce the thermal noise (at the cost of speed), or increase the bias current to increase the largest input current (at the cost of power consumption). Nevertheless, the presented modulator was implemented in *standard* digital CMOS process, while SC modulators used double-poly CMOS process that is more expensive.

Compared with other SI designs, the presented modulator is outstanding. No measurement results were presented in [6]–[8] except in [5]. Though the SI modulator in [5] had a larger dynamic range, but the supply voltage was 5 V, and the power consumption was 38 times larger and the chip area was 5 times larger than the presented modulator. Therefore, considering process cost, power consumption, supply voltage, and dynamic range, the presented SI modulator is competitive. It is one of the reported low-voltage SI Δ-Σ modulators in standard digital CMOS process [1], demonstrating that the SI technique is an inexpensive alternative to the SC technique.

TABLE I
Measured SI Modulator Performance

Technology	0.8-μm digital CMOS
Active chip area	0.25 mm^2
Power supply voltage	3.3 V
Power consumption	2 mW
Clock frequency	2.45 MHz
Oversampling ratio	128
Signal bandwidth	9.6 kHz
0-dB level	6.5 μA
Dynamic range	> 10 b

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