Precise Final State Determination of Mismatched CMOS Latches

W. A. M. Van Noije, W. T. Liu, and J. Navarro S., Jr.

Abstract—**The effect on the metastability of mismatched FET parameters and load capacitances of CMOS latch/flip-flop is analyzed. Theoretical analysis based on small signal devices are provided. From this study we show that the final state depends on both initial voltages and latch mismatches. A novel method using state diagrams is proposed. On the state diagrams obtained by transient analysis of the latch, a straight line can be approximately drawn that defines two semi-planes. This straight line (the metastable line) determines precisely the final latch state, and gives a very good insight about the mismatches which exist in the latch. Several SPICE simulation results are shown for matched/mismatched flip-flops. They agree well with the theoretical ones.**

I. Introduction

LATCHES/FLIP-FLOPS have extensively been used in the implementation of synchronizers, sense amplifiers, comparators, etc. [1]–[4]. Their functions are to amplify, restore, and store voltage signals. The performance requirement of a latch/flip-flop and its design issues vary with applications. Metastability, for instance, is an important issue in any high speed circuit design. It affects the clock speed of VLSI design. Another important issue is to verify if the latch/flip-flop would settle in the correct final state.

Problems related to the metastable state in CMOS latch design have been studied by many researchers [5], [6]. Most papers show the effect of the circuit parameters and noise on the metastability by theoretical analysis based on the small signal model. To retain data, latches and flip-flops provide a regenerative configuration which are generally modeled as a pair of cross-coupled inverters, as shown in Fig. 1. The metastability effect could be better understood if we consider a perfect symmetrical balanced circuit in which two outputs of the inverters are initially equal. In a noise free environment, the circuit would stabilize and remain at the metastable state. Only when the initial output voltages have imbalanced values then the latch would eventually reach a normal state. The length of resolution time for the latch to escape from the metastable state depends on the initial imbalance, the gain, and the bandwidth of the latch. Either the metastable state remaining or unusually long resolution time will cause system failures, which should be avoided.

Parametric imbalance in the transconductances, conductances, parasitic capacitances, threshold voltage of the FET's, or in the load capacitances causes an undesirable effect: the latch/flip-flop may settle in a wrong state regardless of the initial imbalance voltage. Different solutions for this problem includes using differential amplifiers before latches or offset cancellation [3], limiting the number of cells connected in sensing amplifiers [7], etc.

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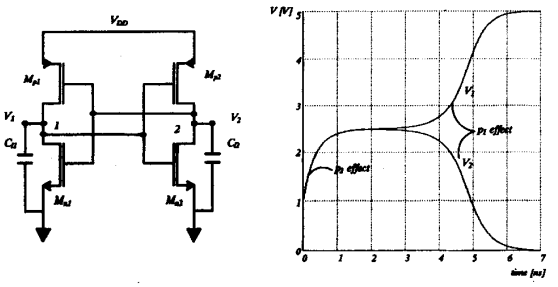


(a) (b)

Fig. 1. Latch composed of (a) two cross-coupled CMOS inverters and (b) its timing simulation. The initial difference $V_1 - V_2$ is 0.1 mV and the two inverters are matched.

The main subject of our work is the study of the behavior of cross-coupled latches due to mismatched parameters and initial conditions. Unfortunately in the available literature, the reports about mismatches in cross-coupled circuits are restricted to some sense amplifiers. Here a novel method, with state diagrams, is used to analyze the latch behavior [8].

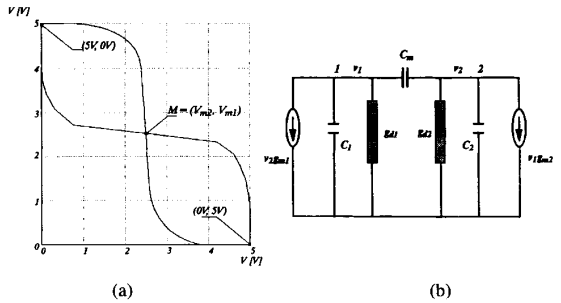
In Section II of this paper, the cross-coupled latch and its small signal model are studied. State description is used to characterize the behavior of it. Also the state equations are presented. Based on the assessment of Section II, the settlement analysis of a latch is done in Section III. Simulation results in term of state diagrams are provided to verify the theoretical derivations. On the state diagram, a straight line (metastable line) is traced and as it will be presented later, this line determines the states where the latch reaches precisely. Finally, in Section IV conclusions are given.

II. Theoretical Model

Fig. 1(a) shows the CMOS latch of our study. It is composed of two cross-coupled inverters. Such circuits are able to amplify the difference between output voltages V_1 and V_2. Fig. 1(b) shows, for symmetric inverters, how V_1 and V_2 are diverged along time.

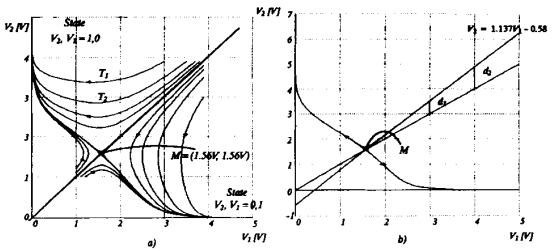
Two main problems associated with the latch operation are:

- **the metastability:** it is related to the decision speed and the capability of achieving some predefined minimum voltage values at the outputs in a certain time interval (see Fig. 1(b)). This problem has already been extensively studied [5], [6];
- **the mismatch:** the capability to provide a correct decision in the final state, when the transistors or the load capac-



(a) (b)

Fig. 2. Diagram with (a) the three equilibrium points of a latch and (b) its small signal model.



(a) (b)

Fig. 3. State diagram for a latch with $M_{p1} = M_{p2}$ ($W/L = 3.0\,\mu$m $/1.2\,\mu$m) and $M_{n1} = M_{n2}$ ($W/L = 6.0\,\mu$m $/1.2\,\mu$m): (a) $C_{l1} = C_{l2} = 200$ fF; (b) $C_{l1} = 200$ fF and $C_{l2} = 100$ fF.

itances are not matched (definition of a correct decision is given below). This problem has scarcely been studied and is the main subject of this paper.

Fig. 2 shows dc transfer curves of inverters of a latch and its small signal model. In the transfer curves, three equilibrium points are defined: when $(V_2, V_1) = (0\text{ V}, 5\text{ V})$, $(V_2, V_1) = (5\text{ V}, 0\text{ V})$, and $(V_2, V_1) = (V_{m2}, V_{m1})$. The first two points are stable and the third one, the metastable point, is unstable. It means that the circuit will be pushed out from the metastable point (V_{m2}, V_{m1}) by any interference, where the values V_{m1} and V_{m2} are the metastable voltages. Only the two stable points are allowed as the final state for correct operation.

A correct decision is made if the latch settles at the equilibrium point $(V_2, V_1) = (5\text{ V}, 0\text{ V})$ when V_2 is higher than V_1 at $t = 0$ s. Conversely, if V_1 is higher than V_2, the equilibrium point attained should be $(V_2, V_1) = (0\text{ V}, 5\text{ V})$. Otherwise, a mismatch in the input voltages exists in the latch.

A. State Description

The state description is used to study the behavior of the latch. On the studied latch voltages V_1 and V_2 are the chosen state variables.

In order to provide a better analysis on the metastability as well as on the mismatch problems, a novel method based on state diagrams is proposed. This method consists of conducting transient analysis (e.g., with SPICE) of the latch and tracing the transfer curves of V_2 versus V_1. This state diagram shows how the circuit state evolves from any initial point to the final state. It is important that the timing analysis must be long enough so that a stable state is reached. To construct a useful state diagram, several different initial conditions are applied and thus produce different corresponding trajectories. These trajectories would eventually settle at one of the equilibrium points.

If the latch is completely matched in both inverters and loads, the direction of (V_2, V_1) is a plain function of the initial condition. For example, if $V_2(t = 0) = V_2(0) > V_1(0) = V_1(t = 0)$ then (V_2, V_1) would always reach the state (5 V, 0 V) and vice versa. Fig. 3(a) shows the state diagram for a completely matched latch. Several trajectories are presented and the direction of each one is indicated by arrows. In this figure, a straight line, passing at (0 V, 0 V), with an angle of 45° defines two semi-planes for possible final latch states. This means that all initial conditions associated with a point below this line leads (V_2, V_1) to the logic state (0, 1), while any point above this line leads to (1, 0). It is worthwhile to point out that the state convergence is independent of relative position to the metastable point, indicated as M, with $V_{m1} = V_{m2} = 1.56$ V. The logical state (1, 0) means the state $(V_2, V_1) = (5\text{ V}, 0\text{ V})$; (0, 1) means (0 V, 5 V). This notation will be used hereafter.

The above mentioned line will be called "metastable line" and it can be defined as being the set of initial conditions which would drive the latch to the metastable point.

B. Small Signal Analysis

The small signal analysis for the latch, though is simple, can lead to understand the latch behavior. Such linearization can be done around any point (V_{2X}, V_{1X}). In consequence, the large signal solution $V_2(t)$, for any initial condition, might be obtained from the addition of the small signal result $v_2(t)$ with $V_{2X}(t)$, where $V_{2X}(t)$ is the solution of $V_2(t)$ for the initial condition (V_{2X}, V_{1X}). Similarly, the signal $V_1(t)$. For convenience the linearization is done around the metatable point where $V_{2X}(t)$ and $V_{1X}(t)$ are constant.

Fig. 2(b) presents the small signal model for the latch circuit. The circuit analysis gives

$$g_{m1}v_2 + g_{d1}v_1 + C_1\frac{dv_1}{dt} + C_m\frac{d(v_1 - v_2)}{dt} = 0$$

and

$$g_{m2}v_1 + g_{d2}v_2 + C_2\frac{dv_2}{dt} + C_m\frac{d(v_2 - v_1)}{dt} = 0 \qquad (1)$$

where: g_{m1}, g_{m2} are equivalent transconductances (of M_{p1}/M_{n1} and M_{p2}/M_{n2}, respectively); g_{d1}, g_{d2} are equivalent conductances; C_m is the coupling capacitance between the gate and drain of the FET's; C_1 and C_2 are the total node capacitances (including diffusion and routing one); $v_1(t) = V_1(t) - V_{m1}$ and $v_2(t) = V_2(t) - V_{m2}$ with $V_2(t)$ and $V_1(t)$ as the total node voltages; and V_{m2}, V_{m1} the metastable voltage values of node 1 and 2, respectively, (complete expressions for the small signal parameters can be found in [5]).

The signals v_1 and v_2 represent the small signal version of the state variables. For the convenience, $(v_2 - v_1)$ is chosen as

the output function. Applying the Laplace transforms with the initial conditions of $v_1(0\_)$ and $v_2(0\_)$, both the state transition and output function can be obtained:

$$\begin{aligned} v_j(t) = &\left\{ \frac{v_j(0\_)}{Q^{1/2}}[ap_1 + C_j g_{di} + C_m(g_{di} + g_{mj})] \right. \\ &\left. - \frac{v_i(0\_)}{Q^{1/2}}[C_i g_{mj} + C_m(g_{di} + g_{mj})] \right\} e^{p_1 t} \\ &- \left\{ \frac{v_j(0\_)}{Q^{1/2}}[ap_2 + C_j g_{di} + C_m(g_{di} + g_{mj})] \right. \\ &\left. - \frac{v_i(0\_)}{Q^{1/2}}[C_i g_{mj} + C_m(g_{di} + g_{mj})] \right\} e^{p_2 t} \end{aligned} \quad (2)$$

$$\begin{aligned} &v_2(t) - v_1(t) \\ &= \left\{ \frac{v_2(0\_)}{Q^{1/2}}[ap_1 + C_2(g_{d1} + g_{m1}) + C_m G] \right. \\ &\quad \left. - \frac{v_1(0\_)}{Q^{1/2}}[ap_1 + C_1(g_{d2} + g_{m2}) + C_m G] \right\} e^{p_1 t} \\ &\quad - \left\{ \frac{v_2(0\_)}{Q^{1/2}}[ap_2 + C_2(g_{d1} + g_{m1}) + C_m G] \right. \\ &\quad \left. - \frac{v_1(0\_)}{Q^{1/2}}[ap_2 + C_1(g_{d2} + g_{m2}) + C_m G] \right\} e^{p_2 t} \end{aligned} \quad (3)$$

where $i = 1$ and $j = 2$ is for $v_2(t)$ while $i = 2$ and $j = 1$ is for $v_1(t)$;

$$\begin{aligned} p_1 &= \frac{(-M + Q^{1/2})}{2a}; \quad p_2 = \frac{(-M - Q^{1/2})}{2a}; \\ a &= C_1 C_2 + C_m(C_1 + C_2); \\ M &= g_{d1} C_2 + g_{d2} C_1 + C_m G; \\ G &= g_{d1} + g_{d2} + g_{m1} + g_{m2}; \\ Q &= M^2 - 4a(g_{d1} g_{d2} - g_{m1} g_{m2}). \end{aligned}$$

In order to have a positive pole (necessary for latching), $g_{m1} g_{m2}$ must be greater than $g_{d1} g_{d2}$, therefore, $p_1 > 0$ and $p_2 < 0$. In such case the term $e^{p_2 t}$ goes more rapidly to zero and the other term $e^{p_1 t}$ will be responsible for the amplification. The effect of $e^{p_2 t}$ is to lead the voltages $V_1(t)$ and $V_2(t)$ closer to the metastable point and is better observed when the initial difference is small (i.e., $V_2(0\_)$ close to $V_1(0\_)$) (as pointed out in Fig. 1(b)).

III. Simulations and Discussions

Equation (3) of the output is useful in the study of the latch operation. Results based on (3) are derived and verified through SPICE simulations (level 3). It is important to point it out that until now no specific transistor model was used, therefore the results are always correct for any transistor model as far as it leads to the small signal circuit in Fig. 2(b). Later on we shall adopt a generic dc drain current model of the transistor in order to derive simpler expressions, but such relations are only drawn to easy the interpretation.

A. The Latch Final State and Metastable Line

Equation (3) indicates that the final state of the latch does not depend only on the initial conditions but also on the mismatching that exists in the latch (either parametric or load capacitance imbalance). This means that even for $V_2(0\_) > V_1(0\_)$ or $v_2(0\_) > v_1(0\_)$, the final state of V_2 can be logical "0." A special situation appears when the latch initial condition is that $v_2(0\_)$ is positive (or negative) and $v_1(0\_)$ is negative (or positive), then the final latch state will always be logical "1" (or always "0") i.e., $V_2 \rightarrow$ "1" (or "0") and $V_1 \rightarrow$ "0" (or "1"), respectively, regardless of the mismatching in the latch circuit. Note that $v_2(0\_)$ positive means that the value of $V_2(0\_)$ is greater than V_{m2}.

What (3) shows clearly is that the distances between V_2, V_1, and their metastable voltages are very important. Fig. 4(a) illustrates these results. The simulated latch presents $V_{m1} = 2.147$ V and $V_{m2} = 1.535$ V and $C_{l1} = C_{l2}$ (load capacitances at node 1 and 2, respectively). Here initial voltage V_2 is "just little above" V_{m2} and V_1 "just below" V_{m1}, and the final state is (1, 0). In Fig. 4(b) V_2 is below V_{m2} then leading to (0, 1).

The form of the metastable line as defined above can be drawn from (3). As explained previously, the term $e^{p_2 t}$ goes to zero when $t \gg 0$ (or more precisely when $t \gg |1/p_2|$). If the coefficient of the term $e^{p_1 t}$is zero, then the difference $(v_2(t) - v_1(t))$ is also led to zero together with $e^{p_2 t}$. The above condition is satisfied if the following relation, which is determined from (3), is observed:

$$\frac{v_2(0\_)}{v_1(0\_)} = \frac{[ap_1 + C_1(g_{d2} + g_{m2}) + C_m G]}{[ap_1 + C_2(g_{d1} + g_{m1}) + C_m G]} = \gamma \quad (4)$$

where γ is the metastable line slope.

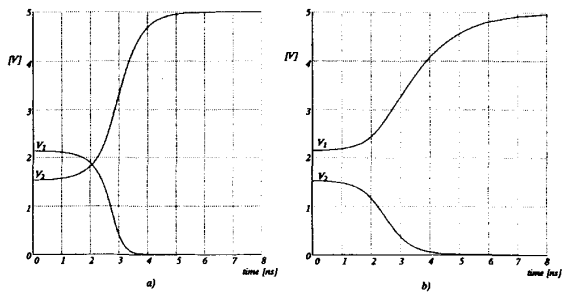
This rate between $v_2(0\_)$ and $v_1(0\_)$ causes that the $e^{p_1 t}$ term in (2) is zero too. It means that $V_1 \rightarrow V_{m1}$ and $V_2 \rightarrow V_{m2}$ when t increases. In consequence, the relation (4) can be used to describe the slope of metastable line. This line pass through the metastable point, which completes the line characterization.

B. State Diagrams

The utilization of state diagrams to the analysis of metastability is useful for observing the mismatching effects for all inputs. This dependence between mismatch errors and input voltages has first been reported in [8].

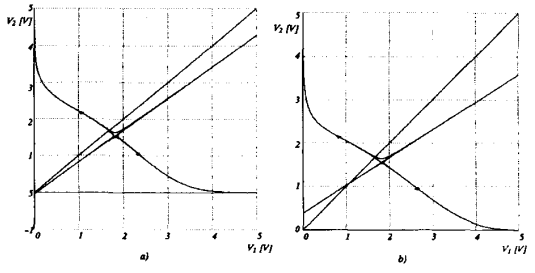
Fig. 3(b) shows a diagram example where only mismatch in the load capacitance exists ($C_{l1} = 200$ fF and $C_{l2} = 100$ fF). The metastable line is drawn together with the first quadrant bisectrix (which represents the metastable line for the full matched case). The metastable line is now given approximately by $\gamma V_1 + \beta$, with $\gamma = 1.367$ and $\beta = -0.577$ V. The distance between the two lines indicates how severe the mismatch effect is.

Note that the metastable voltages are equal for matched inverters because V_{m1} and V_{m2} are independent of the capacitances (either the transistors capacitances or load capacitances). Therefore the metastable line cross the bisectrix at the point M $(V_{m2} = V_{m1})$.



(a) (b)

Fig. 4. Timing simulation for an unmatched latch with $M_{p1} = (W/L = 3.0\,\mu\text{m}/1.2\,\mu\text{m})$, $M_{p2} = (W/L = 3.0\,\mu\text{m}/1.0\,\mu\text{m}$, $M_{n1} = (W/L = 6.0\,\mu\text{m}/1.2\,\mu\text{m})$, $M_{n2} = (W/L = 6.0\,\mu\text{m}/3.0\,\mu\text{m})$, $C_{l1} = C_{l2} = 200$ f ($V_{m1} = 2.147$ V and $V_{m2} = 1.535$ V). (a) Initial conditions $V_1(0\_) = 2.14$ V and $V_2(0\_) = 1.54$ V. (b) $V_1(0\_) = 2.155$ V and $V_2(0\_) = 1.53$ V.



(a) (b)

Fig. 5. State diagrams for an unmatched latch with $M_{p1} = M_{p2}$ $(W/L = 3.0\,\mu\text{m}/1.2\,\mu\text{m})$, $M_{n1} = (W/L = 6.0\,\mu\text{m}/1.2\,\mu\text{m})$ and $M_{n2} = (W/L = 6.0\,\mu\text{m}/2.0\,\mu\text{m})$: (a) $C_{l1} = C_{l2} = 200$ fF; (b) $C_{l1} = 100$ fF and $C_{l2} = 200$ fF.

The experimental metastable line has accurately been achieved by mean of simulations, which is automatically executed by a program called **Metaline**. This program was also used to produce the state diagram for mismatched inverters (thus $V_{m1} \neq V_{m2}$). Fig. 5(a) shows the result for balanced load capacitance. In Fig. 5(b), the load capacitances are different. Although in a careful design the mismatch will be smaller than illustrated in the example, those values were chosen to better visualize the effects.

The expression (4) may be used to predict the metastable line behavior. In this case it is only necessary to know if γ is greater or smaller than 1 (the bisectrix slope). This information together with the metastable point are used to verify if the error decreases or increases with the input voltages. Moreover, with $\gamma_1 = C_1(g_{d2} + g_{m2})/C_2(g_{d1} + g_{m1})$, it is easy to show that $\gamma_1 > 1$ if and only if $\gamma > 1$, and $\gamma_1 < 1$ if and only if $\gamma < 1$. Consequently the shorter γ_1 expression could be used.

In order to verify the correctness of the theoretical derivation, a simple but realistic transistor model is used in this section as presented in [9]. It is important to note that the transistors are operated in saturation mode in the neighbor of metastable voltage. The saturation current of a transistor is modeled by the relation as follows [9]:

$$I_D = \frac{WB}{L}(V_{GS} - V_T)^x \tag{5}$$

where: I_D is the drain current; B and x are constants which describe the short-channel effects in a empirical model; W, L, and V_T are as usually defined; and V_{GS} is the gate-source voltage.

The value of x is between 1 and 2, with $x = 2$ for transistors with long channel and x being close to 1 for short channel. Considering that the value of x is the same for both transistors (p and n transistors), and disregarding the channel modulation effect, it is possible to find a simplified expression for V_{m1} and V_{m2}. In consequence, the values of V_m's with the forms for g_{m1} and g_{m2} are handled to rewrite γ_1 ($g_{d1} = g_{d2} = 0$ from (5)):

$$\gamma_1 = \frac{C_1}{C_2}\left(\frac{V_{DD} - V_{Tn2} - |V_{Tp2}|}{V_{DD} - V_{Tn1} - |V_{Tp1}|}\right)^{x-1} \cdot \left(\frac{(W_{p2}B_{p2}L_{n2})^{1/x} + (W_{n2}B_{n2}L_{p2})^{1/x}}{(W_{p1}B_{p1}L_{n1})^{1/x} + (W_{n1}B_{n1}L_{p1})^{1/x}}\right)^{2-x} \cdot \left(\frac{W_{p2}B_{p2}W_{n2}B_{n2}}{W_{p1}B_{p1}W_{n1}B_{n1}}\right)^{1-(1/x)} \left(\frac{L_{p1}L_{n1}}{L_{p2}L_{n2}}\right)^{1/x} \tag{6}$$

where: the subscripts $\boldsymbol{ni}, \boldsymbol{pi}$ are related to transistors M_{ni} and M_{pi} with $i = 1$ or 2 (Fig. 1(a)); and V_{DD} is power supply voltage.

Now consider the diagram shown in Fig. 5(a). For simplification, we may suppose $C_1 \approx C_2$ since C_{l1} and C_{l2} are large. The fact that $L_{n1} = 1.2\,\mu\text{m} < 2.0\,\mu\text{m} = L_{n2}$ implies that both γ_1 and γ are less than 1. This result is in agreement to the diagram shown in Fig. 5(a). When C_l's are different and C_{l1} is reduced, γ_1 and γ will become smaller. Again the result is agreeable to the diagram in Fig. 5(b).

Theoretical analyses and SPICE simulations establish the dependence of latch final state on both the initial voltage conditions and the mismatches of transistor parameters. All these results are rather important in applications where a correct decision is expected to be reached in a small resolution time such as a comparator design. Finally, the analyses allow us to find a way of reducing the errors due to the input voltage mismatch.

IV. Conclusion

This paper investigates the metastability of latch/flip-flops due to mismatch of FET's parameters and load capacitances. Theoretical results in term of equations are derived by a small signal model for the latch. As a generic device model, the equations quantify the effect on the final latch state by the initial input voltages and the mismatches in the latch. The new concept of the metastable line was introduced, which represents the set of initial conditions that drives the latch to the metastable point. The equation for the metastable line was also obtained. Through the study of state diagrams for a latch circuit, a straight line could be approximately drawn that determines two semi-planes. These two semi-planes precisely define the final state of the latch for all initial conditions. SPICE simulations on matched or mismatched latches are provided to verify the theoretical results. The proposed state diagram analysis with the metastable line provide a good mechanism to give enough insights about the mismatches that exist in a latch.

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