A Static Power Saving TTL-to-CMOS Input Buffer

Changsik Yoo, Min-Kyu Kim, and Wonchan Kim

Abstract—**This paper describes a TTL-to-CMOS input buffer that has no static power consumption for the typical TTL voltage level. The input buffer utilizes a feedback configuration to eliminate static power consumption that renders hysteresis characteristic. The hysteresis characteristic is equivalent to that of a Schmitt trigger and thus provides good noise immunity. A prototype circuit was implemented in a 0.8 μm CMOS process, and the through current is measured to be only 8.9 μA and 11.7 μA for the input of 0.8 V and 2.2 V (the worst case TTL level), respectively. The input buffer gives full-swing output upto 170 MHz when driving a minimum sized inverter with the worst case TTL level according to SPICE simulation [1].**

I. Introduction

CMOS circuits are widely used for integrated systems to exploit their superior characteristics such as low power consumption, large noise margin and high level of integration. However, many systems still use TTL or ECL interface rather than CMOS interface for the compatibility with existing systems or high speed inter-chip communication. So input buffers are necessary for a CMOS system to get inputs of the TTL voltage levels which are to be converted into the CMOS voltage levels.

The most frequently used input buffer is a cascaded CMOS inverter chain whose logic threshold voltage is around the mid-value of the worst case TTL logic high (2.2 V) and TTL logic low (0.8 V). To locate the logic threshold voltage around 1.5 V, the pMOS and nMOS transistors are scaled as shown in Fig. 1. Although simple, it cannot avoid the problem of static power consumption since when the signal of the TTL high level is applied to the input of a CMOS inverter, both the pMOS and nMOS transistors turn on, and thus large through-current flows from V_{DD} to ground. As shown in Fig. 2, there exists static power consumption when the input lies between 0.8 V and 4 V.

To eliminate static power consumption, T. Kobayashi *et al.* proposed SPSIB (Static Power Saving Input Buffer), and shows its usefulness when used as an input buffer of SRAM [2], but Kobayashi's SPSIB requires depletion mode transistors to shift up the level of TTL high signal.

In this paper, we propose a new TTL-to-CMOS input buffer which utilizes a feedback configuration to eliminate static power consumption. This feedback configuration gives the input buffer hysteresis characteristic which improves its noise immunity.

Section II explains how static power consumption is eliminated and Section III analyzes the hysteresis characteristic of the input buffer based on some simplifying assumptions. Simulation and experimental results are given in Section IV, and Section V concludes this paper.

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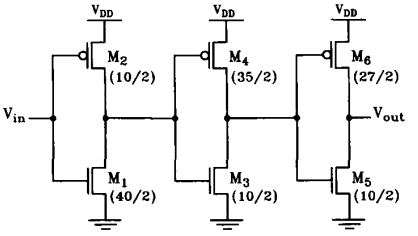

Fig. 1. Conventional TTL-to-CMOS input buffer. The (W/L) ratio of each transistor is shown in the parenthesis.

II. Elimination of Static Power Consumption

The circuit diagram of the proposed TTL-to-CMOS input buffer is shown in Fig. 3 with the (W/L) ratio of each transistor in the parenthesis. In the following, we explain how static power consumption is eliminated by considering the two cases, that is, when the input voltage is 3.4 V (typical voltage level of TTL logic high) and 0.3 V (typical voltage level of TTL logic low), respectively. The supply voltage is 5 V.

A. When the Input Voltage is 3.4 V

In this case, the transistor M_1 turns on and pulls down the output node. When the output node is lowered to about 4 V, M_5 turns on and begins to pull up the gate of M_2 toward 5 V, which causes M_2 to turn off completely. Since the source voltage of the pMOS transistor M_3 cannot be larger than $V_{DD} - V_{Tn4}$ (because of the body effect V_{Tn4} is larger than 1 V), $|V_{GS3}|$ is about only 0.5 V for the input voltage of 3.4 V. Thus the transistor M_3 remains off. It should be noted that the transistor M_4 is essential to turning M_3 off. Without the transistor M_4, $|V_{GS3}|$ would be about 1.6 V which is enough to turn M_3 on. By inserting the transistor M_4 between the transistors M_3 and M_5, static power consumption is eliminated for the input of the TTL high level.

B. When the Input Voltage is 0.3 V

In this case, both the transistors M_3 and M_4 turn on and pull down the gate of the transistor M_2. On the other hand, if the initial value of the output voltage is 0 V, the gate of the transistor M_2 is being pulled up by the transistor M_5. However since the current through the transistors M_3 and M_4 dominates that of the transistor M_5, the output node is pulled up to 5 V and the transistor M_5 turns completely off through

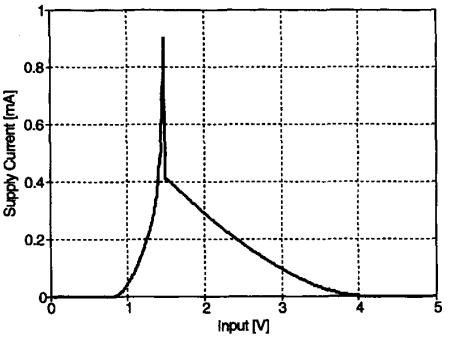

Fig. 2. Simulated through-current as a function of the input voltage of the conventional TTL-to-CMOS input buffer shown in Fig. 1. Through-current flows from V_{DD} to ground when the input lies between 0.8 V and 4 V, and thus there is large static power consumption.

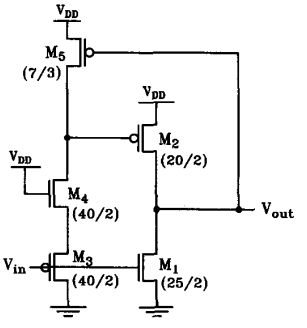

Fig. 3. The circuit diagram of the proposed TTL-to-CMOS input buffer. The (W/L) ratio of each transistor is shown in the parenthesis.

the positive feedback set by the transistors M_2 and M_5. Thus there is no static power consumption in this case either.

III. Analysis of the Hysteresis Characteristic

To get an insight how the two logic threshold voltages are determined, the hysteresis characteristic is analyzed with some simplifying assumptions. It is assumed that the drain current of MOS transistor has square-law characteristic in the saturation region of operation. We will denote the threshold voltages of pMOS transistors as absolute values for simplicity.

A. High-to-Low Logic Threshold Voltage

As V_{in} increases from 0 V to 5 V, we can assume $V_{G2} = V_{\text{in}} + V_{Tp3}$ until V_{out} becomes $V_{DD} - V_{Tp5}$ where the transistor M_5 turns on. When $V_{\text{out}} < V_{DD} - V_{Tp5}$, the transistor M_5 pulls up the gate of the transistor M_2 to 5 V. Then, the output node is suddenly pulled down to 0 V by the transistor M_1 since the transistor M_2 is completely turned off. Thus the input voltage when V_{out} is $V_{DD} - V_{Tp5}$ is the high-to-low logic threshold voltage. When V_{out} is $V_{DD} - V_{Tp5}$, the transistor M_1 is in the saturation region, and the transistor M_2 is in the linear region, and their drain currents are equal, thus the high-to-low logic threshold voltage V_{HL} is given by (1) shown at the bottom of the page where $\beta = \mu C_{\text{OX}}(\text{W/L})$.

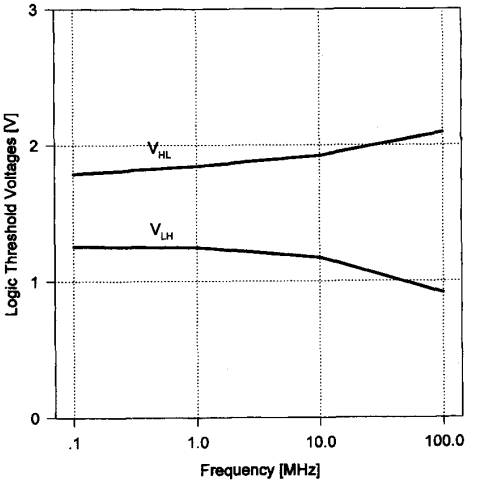

Fig. 4. The simulated dependency of the logic threshold voltages on the operating frequency.

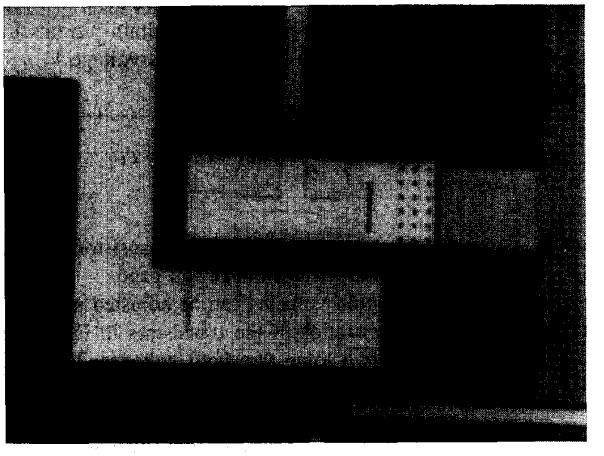

Fig. 5. The microphotograph of the fabricated prototype.

B. Low-to-High Logic Threshold Voltage

As V_{in} decreases from 5 V to 0 V, we can assume $V_{\text{out}} = 0$ V until V_{G2} becomes $V_{DD} - V_{Tp2}$ where the transistor M_2 turns on. When $V_{G2} < V_{DD} - V_{Tp2}$, the transistor M_2 pulls up the output node. As the output voltage increases, the transistor M_5 becomes less conductive and thus the pull-down of the gate of the transistor M_2 becomes faster which makes the

$$V_{HL} = V_{Tn1} - \frac{\beta_2}{\beta_1} V_{Tp5} + \sqrt{\frac{\beta_2}{\beta_1} V_{Tp5} \left\{ \left(\frac{\beta_2}{\beta_1} - 1 \right) V_{Tp5} + 2(V_{DD} - V_{Tp3} - V_{Tp2} - V_{Tn1}) \right\}}. \quad (1)$$

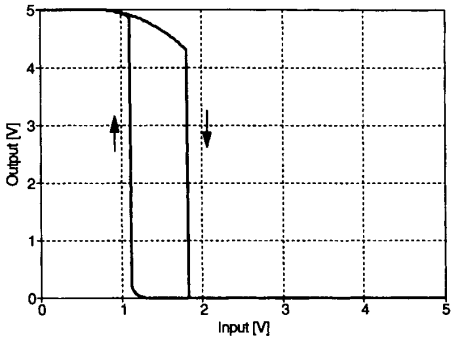

Fig. 6. The measured voltage transfer characteristic of the proposed input buffer shown in Fig. 3. The high-to-low and low-to-high logic threshold voltages are 1.83 and 1.11 V, respectively.

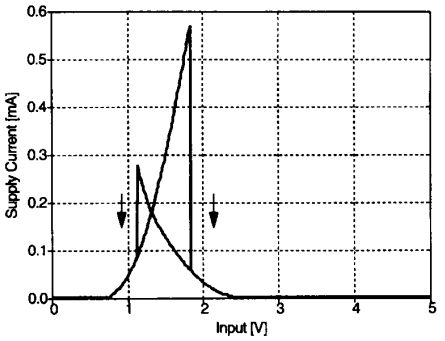

Fig. 7. Measured through-current as a function of the input voltage of the proposed input buffer. When the input voltage is larger than 2.4 V or smaller than 0.75 V, there is no through-current, and thus no static power consumption.

charging of the load capacitance faster. This is the positive feedback action.

In this case, the input voltage when V_{G2} is $V_{DD}-V_{Tp2}$ is the low-to-high logic threshold voltage. When V_{G2} is $V_{DD}-V_{Tp2}$, the transistor M_3 is in the saturation region, and the transistors M_4 and M_5 are in the linear region, and their drain currents are all equal, thus the low-to-high logic threshold voltage V_{LH} is given by

$$V_{LH} = V_{S4} - V_{Tp3} - \sqrt{\frac{2\beta_5}{\beta_3}V_{Tp2}\left(V_{DD} - V_{Tp5} - \frac{V_{Tp2}}{2}\right)} \tag{2}$$

where V_{S4} is the source node voltage of the transistor M_4 and is given by (3) shown at the bottom of the page.

The two logic threshold voltages can be adjusted using the (1) and (2). The (W/L) ratios of the transistors in Fig. 3 are chosen such that the two logic threshold voltages, V_{HL} and V_{LH}, are 1.8 V and 1.2 V, respectively.

C. Process Sensitivity of the Logic Threshold Voltages

As can be seen in the (1) and (2), the logic threshold voltages are directly dependent on the process parameters such as threshold voltage, carrier mobility, gate oxide thickness, and etc. Thus, Monte-Carlo simulation was performed with level 3 SPICE parameters to find how much the logic threshold voltages change as the process parameters fluctuate.

Threshold voltages of the transistors, carrier mobilities and gate oxide thickness are assumed to be independent Gaussian random variables which can vary from their nominal values as much as 10%, that is, 3σ = (nominal value of the parameter)/10. With these assumptions, 1000 samples are taken and the standard deviations of the logic threshold voltages are calculated to be 43.9 mV and 22.5 mV for V_{HL} and V_{LH}, respectively. These values are comparable to the standard deviation of the logic threshold voltage of the conventional TTL-to-CMOS input buffer shown in Fig. 1 which is 28.1 mV obtained from Monte-Carlo simulation with the same conditions as above.

D. The Logic Threshold Voltages as a Function of Frequency

The logic threshold voltages change as the operating frequency increases. This dependency is simulated and shown in Fig. 4. As can be seen in the figure, V_{HL} increases and V_{LH} decreases as the operating frequency increases. This is mainly due to the propagation delay from the input to the output. The hysteresis window remains within the worst case TTL level, that is, V_{HL} remains smaller than 2.2 V and V_{LH} remains larger than 0.8 V.

IV. Simulation and Experimental Results

The prototype circuit was implemented in a 0.8 μm CMOS process. Fig. 5 is the microphotograph of the fabricated prototype.

To verify the operation of the circuit, the voltage transfer characteristic and the through-current were measured using HP4145B and are shown in Fig. 6 and Fig. 7, respectively. Hysteresis characteristic can be observed in the figures. The measured high-to-low and low-to-high logic threshold voltages are 1.83 V and 1.11 V, respectively, and this result agrees well with the design targets of 1.8 V and 1.2 V. When the input voltage is larger than 2.4 V or smaller than 0.75 V, there is no current flowing from V_{DD} to ground, and thus no static power consumption.

The measured transient response of the input buffer is shown in Fig. 8 when the input signal is of the worst case TTL level, that is, 2.2 V for logic high and 0.8 V for logic low. High speed measurement was impossible since we did not include an output buffer which is to drive the large value of load capacitance (pad, pin and test equipment).

$$V_{S4} = V_{DD} - V_{Tn4} - \sqrt{(V_{Tp2} - V_{Tn4})^2 + \frac{2\beta_5}{\beta_4}V_{Tp2}\left(V_{DD} - V_{Tp5} - \frac{V_{Tp2}}{2}\right)}. \tag{3}$$

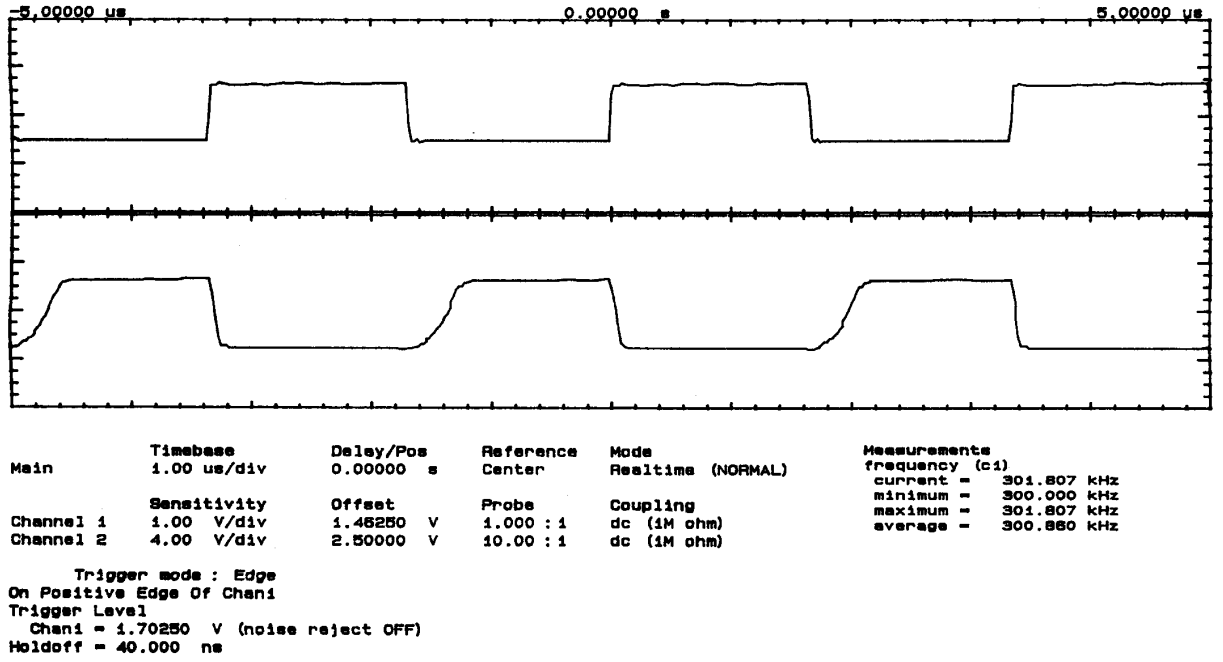

Fig. 8. Transient response of the input buffer; top trace—300 kHz square wave input signal with the worst case TTL level, i.e., 2.2 V for logic high and 0.8 V for logic low; bottom trace—output waveform.

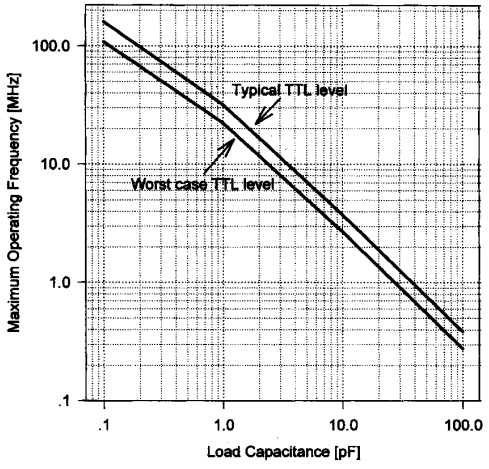

Fig. 9. Simulated dependency of the maximum operating frequency on the load capacitance.

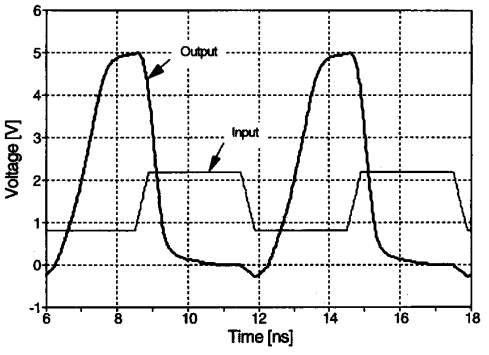

Fig. 10. Simulated transient response of the input buffer when driving a minimum sized inverter ($W_N = 2\ \mu$m, $W_P = 6\ \mu$m, $L = 2\ \mu$m) with the worst case TTL level; top trace—170 MHz input signal; bottom trace—output waveform.

The maximum speed of operation decreases as the load capacitance becomes large, and this dependency is simulated and shown in Fig. 9. When the load capacitance is 30 pF (estimated sum of parasitic capacitance of pad, pin and test equipment) the maximum operation speed is about only 880 kHz, but this does not impose a problem since the input buffer will not drive such a large load capacitor. The input buffer gives full-swing output upto 170 MHz when driving a minimum sized inverter ($W_N = 2\ \mu$m, $W_P = 6\ \mu$m, $L = 2\ \mu$m) with the worst case TTL levels of which simulation result is shown in Fig. 10 [1].

V. Conclusion

A new TTL-to-CMOS input buffer is described which has no static power consumption for the typical TTL output level, the hysteresis characteristic of the input buffer is analyzed, and simulation and experimental results of the prototype circuit are given. The experimental results show that there is no static power consumption when the input voltage is larger than 2.4 V or smaller than 0.75 V. The input buffer is noise-immune due to its hysteresis characteristic caused by the positive feedback.

The proposed input buffer can also be used to regenerate the degraded voltage levels of the signal into the CMOS levels which comes from an nMOS pass transistor without static

power consumption since the voltage level of the signal is very close to the typical TTL level.

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