A Class A/B Floating Buffer BiCMOS Power Op-Amp

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***Abstract*— A class A/B BiCMOS power op-amp designed to drive the L/R load of a disk drive head actuator is presented. The amplifier uses totem pole NMOS outputs instead of bipolar devices to avoid the high collector resistance in the simplified process used. A unique floating buffer technique regulates the quiescent totem pole current of the output devices and provides control for deep triode NMOS operation. The amplifier is capable of driving a load in all four *V-I* quadrants without a deadband during transition, and achieves a 0.25 A drive capacity into a 7.5-Ω load using a 5-V supply.**

I. Introduction

IN THIS PAPER we present a class A/B power op-amp that is capable of driving the inductive load of a disk drive head actuator motor. Because disk drives are essentially becoming a commodity in the personal computer market, it is desirable to use an inexpensive process with a high level of integration. Thus, the BiCMOS process used for the amplifier does not have a buried layer or sinker structure for the NPN transistors; this results in excessively high collector resistance. Therefore, instead of using bipolar devices, the power output structure is an NMOS totem pole. The circuitry that drives the NMOS devices must be able to provide the four quadrant *V-I* control needed for an inductive load while simultaneously regulating the quiescent current so that there are no deadbands during quadrant transitions. A previous driver method [1] uses source monitored sensfets to sense and control the power NMOS currents. Because a voltage is dropped across the source monitoring resistor, an error in current sense value results (since the NMOS output and sensfet are no longer acting strictly ratiometrically). Instead of using a source monitored sensfet, our topology provides NMOS control by using a replica bias scheme incorporated into a floating buffer circuit. The device serving as the replica has its gate and source voltage matched to that of the corresponding power output device during quiescent operation; thus source voltage error is avoided. Note that current monitoring within the op-amp is used for quiescent control and not to sense load current. The modular design approach of the chip that our op-amp is part of calls for a separate instrumentation amplifier block with its input coming from a small sense resistor in series with the load.

The paper is organized as follows. First, we derive the floating buffer circuit from the classical emitter follower. We then expand this concept and explain the amplifier system. An additional circuit is described that fine tunes the quiescent current variations in the NMOS totem pole caused by component random offsets. Results are presented showing a class A/B amplifier capable of providing 0.25 A drive capacity and 3.8 V swing into an inductive load, from a 5-V supply. The amplifier may be integrated with a twin to form a balanced H bridge topology, thus doubling the voltage swing across the load.

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II. Design

The NPN emitter follower ($I1$, $D1$, and $Q1$) in Fig. 1(a) has the following equation:

$$I2 = nI1 \exp\left(\frac{V_0' - V_0}{V_T}\right). \tag{1}$$

This circuit effectively has two inputs, $I1$ and $V' - V_0$. The first sets the emitter quiescent current $nI1$, which is taken up by the PNP circuitry below when the output of the follower combination is neither sourcing nor sinking. The second input exponentially multiplies the quiescent current in response to a voltage difference when the follower is called upon to source current. Thus, the follower can be considered a local current servo that simultaneously sets a quiescent current for class A/B operation. The NMOS follower of Fig. 1(b) is similar to the NPN circuit discussed above, but has an additional region of operation that needs to be addressed (i.e., the triode mode). First, we look at the follower in saturation.

$$I_{d4} = nI1\left[\frac{(V_0' - V_0) + V_E}{V_{DSAT8A}} + 1\right]^2. \tag{2}$$

In (2) consider that $V_E = 0$ initially and that there is a bottom half circuit in Fig. 1(b) that acts similarly to the top half. Note that when the circuit is in quiescent state, current $nI1$ is absorbed by the bottom half circuit. During current sourcing, the current multiplication caused by the increase of $V_0' - V_0$ is not as dramatic as the exponential function in (1). If $V_0' - V_0$ is augmented by controlled voltage source V_E such that $V_E = A_V(V_0' - V_0)$, the weakness of (2) can be compensated for. In addition, this augmentation provides a means for the gate voltage to be raised above the drain supply (by $V_g \gg V_{DD} + V_T$) so that the follower may be operated in the deep triode region, a mode where high sourcing currents may be obtained with a small V_{DS} drop and the NMOS device size can be minimized. Fig. 1(c) shows the floating buffer scheme used to provide augmentation voltage V_E. Note that an on chip boost regulator will supply 15 V to the buffer so

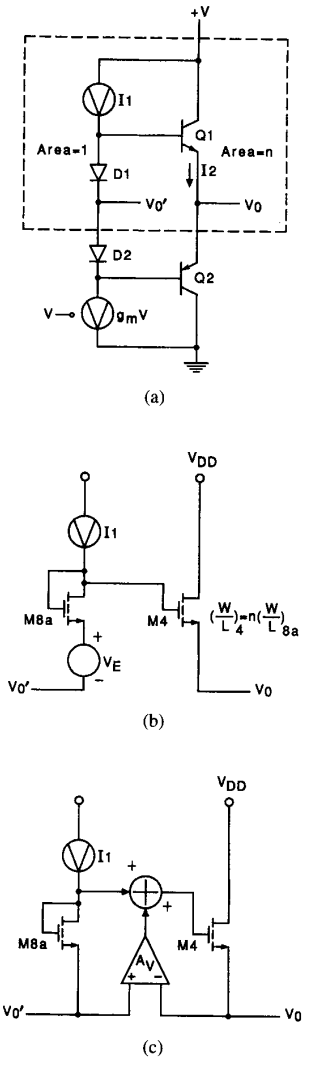

Fig. 1. Floating buffer derivation.

that the NMOS gate can be raised above $V_{DD} = 5$ V. The buffer gain is A_V and $M8a$ is a scaled down floating replica of $M4$. The transistor in triode mode can be modeled as a resistor of value

$$R \approx \frac{L_4}{2K'W_4(1 + A_V)(V_0' - V_0)}. \tag{3}$$

The V_{DSAT} of the floating replica does not appear in (3) since it is a small component of the gate drive. Also, (3) becomes more accurate when V_0 is at maximum source voltage. In fact when $V_0' = V_{DD} = 5$ V, the maximum source voltage, $V_0 = V_{0\mathrm{MAX}}$, relates the maximum gate drive voltage $V_{G\mathrm{MAX}}$ to A_V.

$$A_V = \frac{V_{G\mathrm{MAX}} - V_0' - V_{GS8a}}{V_0' - V_0}. \tag{4}$$

The buffer gain is sized to provide slightly more than the maximum gate drive needed by inflating A_V to account for process and temperature spread (i.e., put $A_V =$

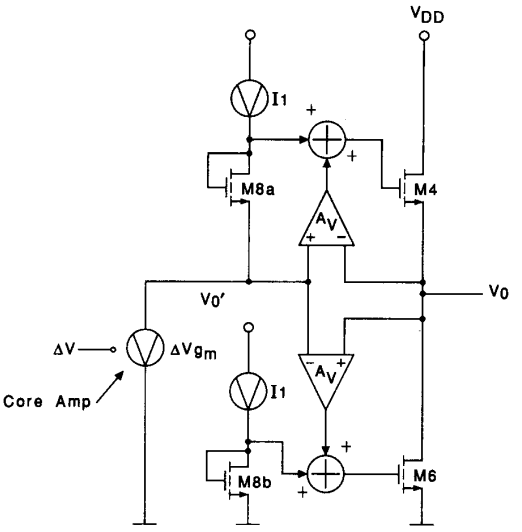

Fig. 2. Simplified amplifier.

g_m (minimum) $\times$ r_o (minimum) so that nomimal g_m and r_o yield a somewhat larger gain than required). Excessive gain will increase error voltage on the gate of the NMOS output created by random offsets in the buffer circuit. We will deal with this more later. The maximum source current is used to calculate the minimum R during $V_{0\mathrm{MAX}}$ and W_4/L_4 is calculated without difficulty using (3).

Referring to Fig. 2, the floating replica source follower can be seen embedded in a simplified diagram of the complete op-amp. Re-arranging the components of the floating replica system creates the common source output sink using $M6$. The quiescent current in $M6$ matches that of $M4$. Since the common source circuit is similar to that in the literature, [2] we limit the discussion. The core amp transconductor equivalent shown in Fig. 2 gives the circuit its op-amp characteristics; more detail will be given later. Fig. 3 is the detailed system level diagram of the amplifier that contains the buffer and core cells with other related circuitry that will be discussed.

The detailed buffer cell (or circuit) of Fig. 4 contains the following elements depicted in Fig. 2: A buffer amplifier (A_V), a replica device ($M8$), a current source to bias the replica device ($I1$) and a voltage summer. As in Fig. 2, the two inputs to the summer are always the output of the buffer amp and the gate/drain of the replica device; thus this functionality is fixed in the detailed buffer circuit of Fig. 4. The inputs to the buffer amp are $V_{IN}+$ and $V_{IN}-$. The connection of the source of the replica is node R. When the buffer circuit is floating so as to drive the NMOS source follower, R is connected to the output of the core amp. For the second buffer circuit used to control the bottom NMOS common source output, R is connected to ground. The output voltage at the emitter of $Q22$ matches the voltage at the drain of the replica device $M8$ when the positive and negative inputs of the buffer are equal. This is because there is no voltage drop across the loop consisting of $Q80$, $R1$, $Q82$, $Q84$, $R2$, and $Q22$. A base current compensation circuit, in Fig. 4, having an output at

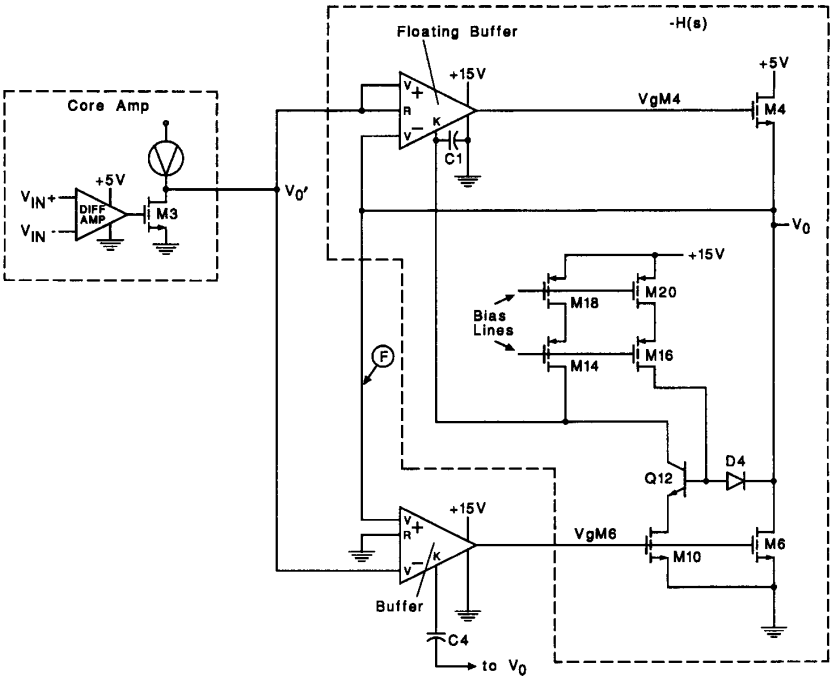

Fig. 3. Detailed amplifier system.

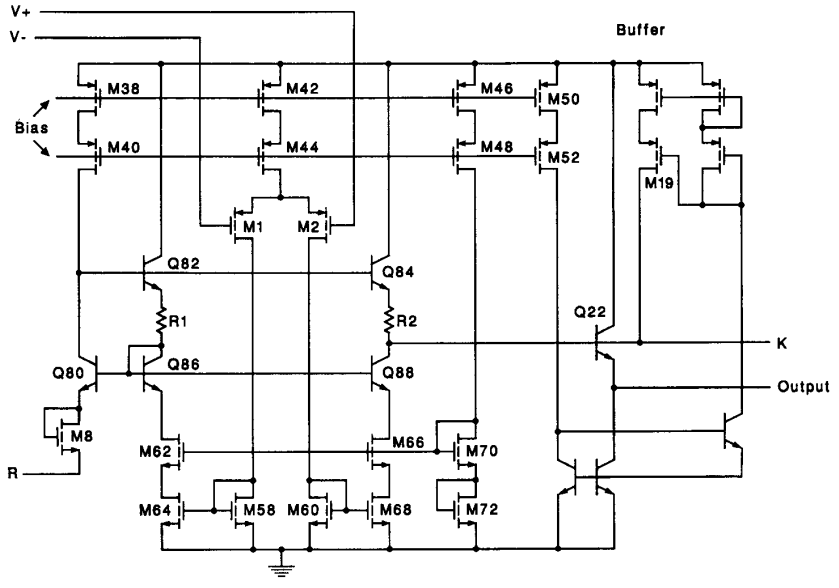

Fig. 4. Buffer.

the drain of $M19$ equalizes the base load of $Q22$ to $Q80$. The amplifier within the detailed buffer circuit has a gain of $g_{m1}R1$, assuming $M1$ matches $M2$ and $R1$ matches $R2$. Note that the summation of the replica voltage with the amplifier takes place because of superposition. The full ac voltage gain is realized at high impedance node K. Compensation of the upper buffer is accomplished by $C1$ tied to ground and K. For the lower buffer, $C4$ is tied between K and the drain of the lower power NMOS device. This is done because the gm of that device varies with the current it is sinking through the load inductor and pole splitting compensation maintains a constant GBP = 10 MHz (the top buffer also has GBP $\approx$ 10 MHz). In order for the power output to slew at 1 V/μs, as determined by the core amp, both upper and lower buffers need to slew the power gates at $\approx$20 V/μs when in deep triode operation. If the core were able to call for a greater slew rate, cross conduction

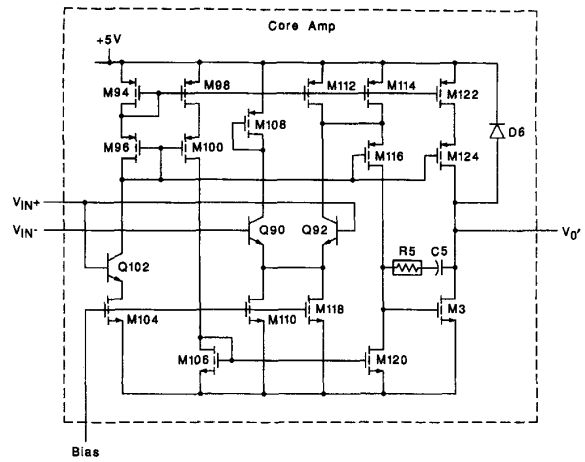

Fig. 5. Core amp.

in the NMOS totem pole would result. For example assume the top NMOS device was initially sourcing maximum current at maximum voltage to the load and that the bottom NMOS device was starting to be called upon to sink load current. If the corresponding high gate voltage of the top NMOS device did not come down sufficiently fast, the bottom NMOS/buffer circuit would pull current not only from the load, but also the top NMOS device. This would result in a large pulse of cross current lasting until the top NMOS gate reached a low enough level. Limiting the slew rate of the core prevents the bottom device from calling for current too quickly. The ratio of the buffer to core slew rate is found by calculating the dV_G/dV_S of the top NMOS output at the initial operating point mentioned above. Similar arguments are applied to the slewing considerations of the bottom NMOS/buffer circuit.

The core amp is shown in Fig. 5. Half the gain of the folded cascode topology is sacrificed to eliminate some high frequency poles. The second stage gain transistor $M3$ is loaded by the "R" input of the top floating buffer [Figs. 4 and 3] and $M122, 124$. The latter devices enhance the gm of $M3$ so that the core has a net phase margin $= 85°$ at GBP $=$ 3 MHz. Thus, the phase margin of the complete op amp is $85° - \tan^{-1}$ [GBPcore/GBPbuffer] $= 70°$.

We return to the control of quiescent current in the NMOS power totem pole. It is desired to set the quiescent current to be nominally at 1% of the amplifier's maximum current sourcing/sinking capacity so that the totem pole power loss is low, yet true class A/B operation is maintained. The acceptable quiescent current range is 1 mA < 2.5 mA < 5 mA. The feed-forward bias action of the replica devices will systematically fix the quiescent totem pole current across process and temperature. Random component effects however will cause voltage variations that are scaled up by the buffer gain (depending on component position within the circuit). When the buffer gain is limited according to the conditions mentioned earlier in the paper, the quiescent current spread is about five times the desired range. Hence, in addition to the dominant feed-forward replica control, some feedback is needed to fine tune out the random effects. We have devised a cross current feedback control circuit similar to [3], but with a shorter signal path to overcome potential restrictions on the feedback loop coefficient. The cross current loop is embedded within the lower buffers pole split loop. A discussion of the stability issues is deferred to the appendix, but we proceed with a general description of the loop.

Referring to Fig. 3, the cross current circuit consists of devices $M10$, $Q12$, $D4$, $M16$, $M20$, $M14$, and $M18$. The net voltage drops of $Vbe12$ and the voltage across $D4$ cause the drain voltages of $M6$ and $M10$ to be nearly equal. Thus, regardless of operating region, $M10$ provides a scaled down drain current to that of power device $M6$. Current $ID10$ passes through $Q12$ and finally reaches high impedance node K of the top buffer. Normally, $ID10$ is precisely balanced at node K by current source $M14$ and $M18$. However, an increase in quiescent current through $M6$ caused by random component mismatch will upset the $ID10$ current balance. This causes the voltage on node K to drop, causing a decrease in source follower voltage $M4$. Thus, a small negative feedback loop finely regulates the totem pole current. If $M4$ is sourcing or $M6$ is sinking current from an external load, the cross current circuit has negligible effect.

III. Results

The power amplifier described in this paper is within a highly integrated disk drive servo control chip. In taking measurements of this first silicon prototype, we endeavored to isolate the amplifier from other circuit blocks of the chip. For example, since the 15 V boost supply was functional but much noisier than expected, we furnished an external 15 V source to the amplifier. In addition, resistor $R1$ within the bottom buffer cell (Figs. 3 and 4) forms a distributed RC transmission line having excess phase delay within the double to single ended converter loop ($Q82$, $R1$, $Q86$, $Q80$). We corrected this local parasitic effect so as to have no effective performance difference on the rest of the op-amp. During measurement, a 1.5 pF feedforward capacitor was probed in across $R1$ as confirmed by simulation. This is easily integratable in the final chip.

Figs. 6 and 7 are photos of amplifier wave forms when the circuit is driven near maximum slew rate at full amplitude with a 20 kHz sine wave. Fig. 6 corresponds to a resistive load and Fig. 7, an inductive load. Both loads are tied to $1/2V_{DD}$ and are using maximum current. The top trace is output voltage, the next trace is output current, then the gate voltage of the NMOS follower, and the bottom is the gate drive of the NMOS common source. At lower slew rates, cross over distortion is invisible; with the high slew rates shown, the distortion is barely visible. The odd shape of the gate wave forms (especially that of the follower) is due to triode operation of the output devices. Note that the photos depict waveforms far more aggressive than would normally be encountered in a disk drive actuator. Fig. 8 illustrates that the class A/B ciruitry supresses inductor free-wheeling under unrealistically severe operating conditions. The 25 kHz square wave response is shown with the load passing ±250 mA (top trace). Note that nonlinearities and quadrant transitioning are visible on the lower output voltage trace, yet overshoot is well controlled; there is no concern for the output voltage exceeding the supply

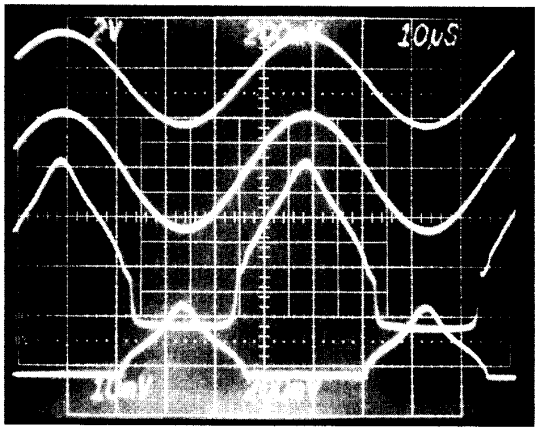

Fig. 6. Resistor load traces.

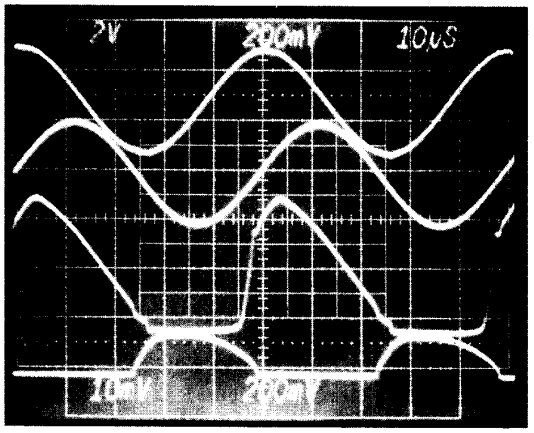

Fig. 7. Inductor load traces.

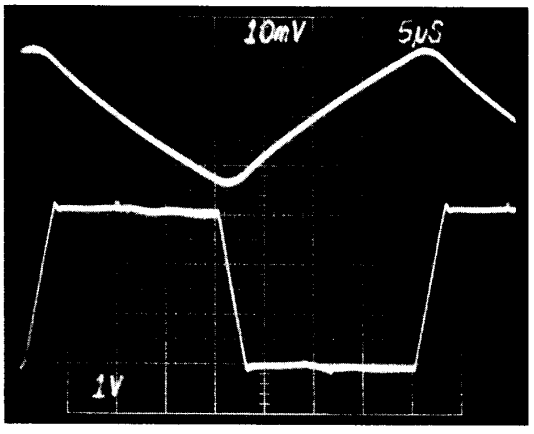

Fig. 8. High frequency square wave response with inductor.

rails. Table I gives some measured parameters of the power op-amp. When a second indentical on chip op-amp is used in a balanced H bridge configuration, the voltage swing across the load is doubled. A power of 0.5 Wrms can be supplied to the load in this fashion. Fig. 9 is a die photo of a single power op-amp.

TABLE I
CIRCUIT PARAMETERS

Item	Value	Comments
Process		$3\,\mu$ BiCMOS
Size	$1850\,\text{mil}^2$	
V_{DD}	5 V	Note: Calculated Core Amp IDD $= 165\,\mu$A
V_{BOOST}	15 V @ 1.45 mA (calculated)	Buffer Supply
$V_{DD} - V_{0\text{MAX}}$	540 mV	Source 250 mA
$V_{0\text{MIN}}$	632 mV	Sink 250 mA
Slew Rate	1 V per μs	
GBP	3.3 MHz*	
THD	0.5%*	3.4 V $p-p$ into $7.5\,\Omega$
$I_{\text{TOTEM POLE}}$	$\approx$1 mA	

*Extrapolated from preliminary measurements

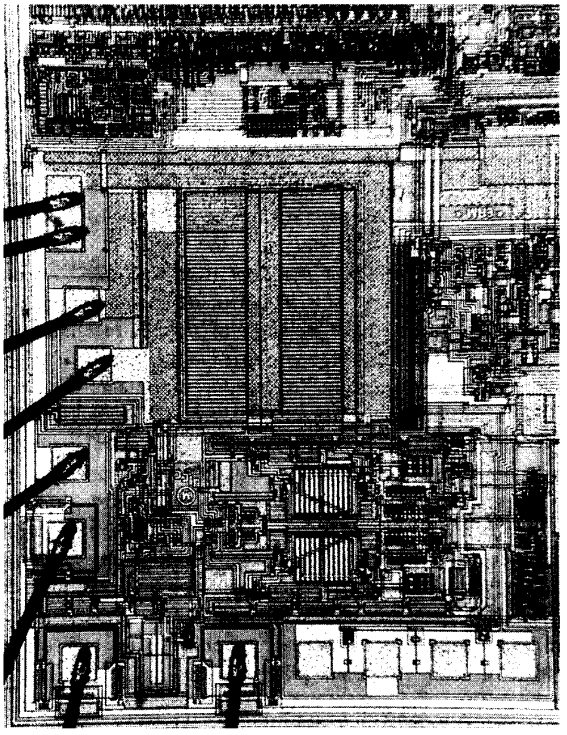

Fig. 9. Die photo.

IV. CONCLUSION

In this paper we have presented a power op-amp designed to drive the L-R load of a disk drive head actuator. Because the NPN devices in the simplified BiCMOS process have high collector resistance, the amplifier's power output structure is an NMOS totem pole. A unique floating buffer circuit controls the totem pole's quiescent current while simultaneously providing gate drive necessary for deep triode operation. Thus, the four V-I quadrants encountered when powering an inductive load are transitioned without a deadband. While the systematic quiescent current is set by replica scaled down power devices embedded within the floating buffer (and fixed bottom buffer), variation in quiescent current caused by random component mismatch is fine tuned by a cross current feedback circuit.

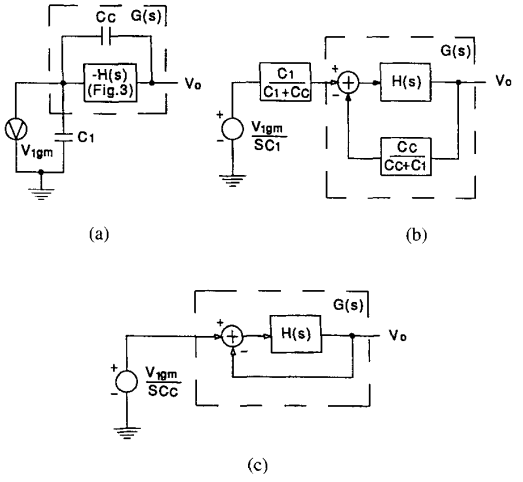

Fig. 10. Pole split derivation.

The results presented show that a high performance power op-amp is practical in a simplified BiCMOS process.

APPENDIX

As mentioned in the main text, the cross current loop is embedded within the pole split loop of the lower buffer circuit. This can be analyzed as an arbitrary transfer function within a pole split loop by creating a very simple intuitive model. Fig. 10(a) shows a pole split loop formed around function $-H(s)$ by compensation capacitor C_C. We assume that the resistive impedance of the first stage is infinitely high and the output of the second stage is zero impedance. By using simple Thevenin equivalent modeling, Fig. 10(a) may be mapped into Fig. 10(b). Thus, the pole split circuit is viewed as a classical feedback system. When $C_C \gg C1, C_C/(C_C + C1) = 1$. This allows Fig. 10(b) to be further reduced to Fig. 10(c). Note that all the assumptions mentioned are applicable to the cross current circuit; some accuracy is sacrificed to gain insight.

The circuitry enclosed by the dashed outer polygon labeled $-H(s)$ in Fig. 3 corresponds to the $H(s)$ of Fig. 10(c). The dominant pole and zero of $H(s)$ is shown in Fig. 11(a) along with their related expressions. gm is the transconductance of $M4$ and $M6$, $gm1$ is the transconductance of each of the buffer input transistors, C is the value of the compensation capacitors for both buffers, $R2$ is the buffer load resistor (see Fig. 4), and variable K is the ratio of $M10$ to $M6$ (see Fig. 3). Closing the loop around $H(s)$ yields $G(s)$ as shown in Fig. 10(c). This, of course, moves the pole of $H(s)$ towards the zero. Fig. 11(b) depicts this along with the integrator pole added by the controlled voltage source of Fig. 10(c). The Bode plot of Fig. 11(c) contains the poles and zero of Fig. 11(b). To complete the cross current loop analysis, $V1$ is made equal to V_0 of Fig. 10(c) by the connection of branch F as shown in Fig. 3. Thus, $G(s)$ is nested within a larger loop that is easily analyzed with the Bode plot. The cross current feedback coefficient corresponding to Fig. 11(c) is 1.66 and is proportional to the variable K. Clearly, this loop is stable.

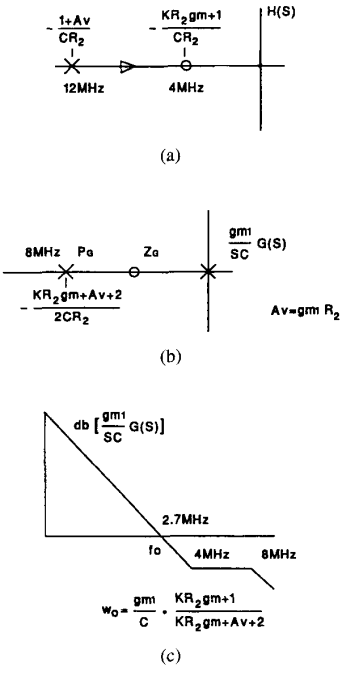

Fig. 11. Current analysis.

To understand the effect of increasing the cross current feedback coefficient, we refer again to Fig. 11. At $K = 0.0017$, $|Zg| < |Pg|$; this is where our circuit is set. As K is increased, the $|Zg|$ will pass $|Pg|$in frequency. The Bode plot would then have a -40 db/decade section in it occurring beyond $|Pg|$. But since $|Pg| > w_o$ when the zero passing occurs, the -40 db section is below the 0 db line and stability is assured. Interestingly, with the parameters $R2$, gm, and $gm1$ used in the circuit, $|Pg|$ will always exceed w_o for K being arbitrarily large, and w_o will not exceed the GBP of the buffers. There are other effects not covered in this simplified explanation (i.e., nonlinearities, loading, etc.) but simulations have worked with K being 10 times the value used in our circuit. This corresponds to K being 2.5 times where the zero passes the pole.

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Mr. Lish holds eight patents and has published several IEEE papers.