High-Speed Low-Power Cross-Coupled Active-Pull-Down ECL Circuit

C. T. Chuang, B. Wu, and C. J. Anderson

Abstract— **This paper presents a high-speed low-power cross-coupled active-pull-down ECL (CC-APD-ECL) circuit. The circuit features a cross-coupled active-pull-down scheme to improve the power-delay of the emitter-follower stage. The cross-coupled biasing scheme preserves the emitter-dotting capability and requires no extra biasing circuit branch and power for the active-pull-down transistor. Based on a 0.8 μm double-poly self-aligned bipolar technology at a power consumption of 1.0 mW/gate, the circuit offers 1.7× improvement in the loaded (FI/FO = 3, C_L = 0.3 pF) delay, 2.1× improvement in the load driving capability, and 3.5× improvement in the dotting delay penalty compared with the conventional ECL circuit. The design considerations of the circuit are discussed.**

I. Introduction

THE power dissipation of high-speed bipolar ECL circuits (Fig. 1(a)) has long been known to limit their VLSI applications. Recently, various active-pull-down schemes [1]–[4] have been actively pursued to reduce the power consumption and improve the delay of the emitter-follower stage in high-speed ECL circuit. These schemes, however, have the following drawbacks: 1) special element, such as capacitor [1]–[3] or charge storage diode [4] is used to couple the signal from the logic stage to the base of the pull-down n-p-n transistor, 2) additional devices are needed to implement the biasing circuit for the active-pull-down transistor, 3) the power consumption for the biasing circuit is wasted, and 4) emitter-dotting is prohibited, thus limiting the application of these schemes.

This paper presents a cross-coupled active-pull-down ECL (CC-APD-ECL) circuit (Fig. 1(b)). The scheme utilizes both output phases of the ECL circuit to achieve cross-couple-biased emitter-follower stages. This circuit scheme provides a large dynamic current during the switching transient, and requires no extra biasing circuit branch and power for the active-pull-down transistors. Furthermore, the emitter-dotting capability is preserved, and the scheme can be applied to series-gating circuitries as well. The circuit, therefore, is capable of providing all the logic functions/capability of dual-phase ECL circuit and can serve as a direct replacement for the latter.

II. Circuit Configuration and Operation

The present circuit scheme (Fig. 1(b)) utilizes a (dc) cross-coupled transistor pair ($Q_{D,L}$ and $Q_{D,R}$) as the active-pull-down devices. Resistors $R_{D,L}$ and $R_{D,R}$ are used to set the steady-state biasing currents for the emitter-follower stages. Capacitors $C_{D,L}$ and $C_{D,R}$ are the speed-up capacitors if desired. When the input is at "High," the output voltage V_{OUT} is at "Low" and $Q_{D,R}$ is biased at cut-in condition (barely on with essentially no current). On the other hand, $V_{\overline{\mathrm{OUT}}}$ is at "High" and thus there is a steady-state current through $Q_{D,L}$. As the current switch switches, the output node rises to "High," providing a very strong base drive to turn $Q_{D,R}$ on heavily. The resulting large dynamic current from $Q_{D,R}$ not only pulls $V_{\overline{\mathrm{OUT}}}$ down very quickly but also helps to turn off $Q_{D,L}$, thus improves the pull-up of V_{OUT} as well.

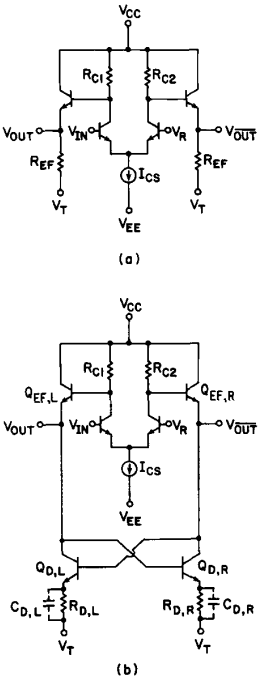

Fig. 1. Schematics of (a) conventional dual-phase ECL circuit, and (b) cross-coupled active-pull-down ECL (CC-APD-ECL) circuit.

Notice that in the conventional ECL circuit, both emitter-follower branches are conducting and consume power. In the present scheme, only one emitter-follower branch is conducting in the steady-state, thus further reducing the power consumption. Also, for the conventional ECL circuit in the steady state, the emitter-follower branch with its output at "High" level conducts more current than the other emitter-follower branch. In the present circuit, due to the cross-coupled biasing scheme, the emitter-follower branch with its output at "High" level conducts much less current (it basically conducts only the base current for the pull-down transistor of the other branch) than the other emitter-follower branch in the steady state.

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The authors are with IBM Research Division, T. J. Watson Research Center, Yorktown Heights, NY 10598 USA.

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TABLE I
TYPICAL PARAMETERS OF THE NPN TRANSISTOR AT 0.8 μm AND 0.5 μm DESIGN RULES

Design Rule	0.80 μm	0.50 μm
A_E (Wafer)	0.4 x 4.0 μm^2	0.25 x 2.0 μm^2
H_{FE}	100	120
Base Transit Time	6.0 ps	3.0 ps
C_{EB}	7.54 fF	5.96 fF
C_{CB}	3.80 fF	2.37 fF
C_{CS}	6.52 fF	4.82 fF
R_E	17.5 Ω	56 Ω
R_{BX}	164 Ω	200 Ω

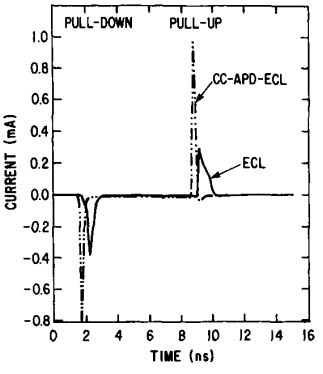

Fig. 2. Net pull-up and pull-down currents during the switching transient for the conventional ECL circuit and the CC-APD-ECL circuit. (0.8 μm design rule, FI/FO = 3, C_L = 0.3 pF, 1.0 mW/gate).

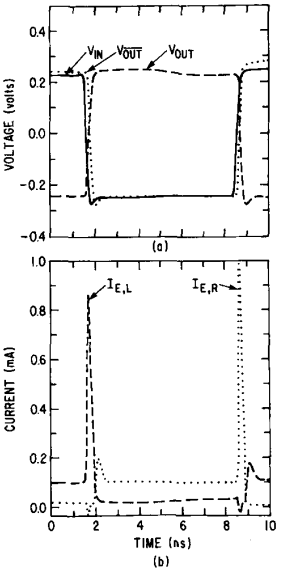

Fig. 3. Pertinent waveforms during the switching transient for the CC-APD-ECL circuit (refer to Fig. 1(b)): (a) voltage waveforms: $V_{\rm IN}$ is the input voltage, $V_{\rm OUT}$ and $V_{\overline{\rm OUT}}$ are the out-of-phase and in-phase output voltage, respectively, and (b) current waveforms: $I_{E,L}$ and $I_{E,R}$ are the currents through the the emitter-follower transistors $Q_{EF,L}$ and $Q_{EF,R}$, respectively. (0.8 μm design rule, FI/FO = 3, C_L = 0.3 pF, 1.0 mW/gate).

Since the coupling to the active-pull-down transistors are derived from the emitter nodes of the emitter-follower transistors, the emitter-dotting capability and any logic function performed prior to the emitter-follower stage in the dual-phase ECL circuit (such as collector-dotting and series gating) are preserved. The circuit, therefore, can serve as a direct replacement for the dual-phase ECL circuit.

Fig. 2 compares the net pull-up and pull-down currents of the present circuit with those for the conventional ECL circuit during the switching transient at a power consumption of 1.0 mW/gate with FI/FO = 3 and C_L = 0.3 pF. These waveforms are based on a 0.8 μm double-poly self-aligned bipolar technology [5], [6] with pertinent measured device parameters listed in Table I. The device parameters and models have been calibrated against the ECL circuit, as well as the static frequency divider performance. Clearly, the present circuit not only offers a much larger, sharper pull-down current but also improves the pull-up current of the other phase by quickly (and completely) shutting off its corresponding pull-down transistor during the switching transient. (Notice that the pull-up current for the present circuit is much sharper and larger than that for the conventional ECL circuit.) The speed in this case is 260 ps for the conventional ECL circuit, and 152 ps for the present circuit. The pertinent waveforms during the switching transient are shown in Fig. 3. One can see that in steady-state only one emitter-follower branch is conducting. The dynamic current during the switching transient ($\simeq$0.9 mA) is much larger than the standby current ($\simeq$0.1 mA for the conducting branch). The inverse relationship between the emitter-follower output voltage and current in the steady-state mentioned previously can also be seen clearly.

III. CIRCUIT PERFORMANCE

The power-delay characteristics for the conventional ECL circuit and the present ECL circuit at 0.8 μm design rule (see Table I) are shown in Fig. 4. For the unloaded case (FI/FO = 1, Fig. 4(a)), the speed improvement is about 22% (40 ps versus 51 ps) at 1.0 mW/gate and 23% (26 ps versus 34 ps) at 3.0 mW/gate. For the loaded case (FI/FO = 3, C_L = 0.3 pF, Fig. 4(b)), speed improvements of 1.7× (152 ps versus 260 ps) at 1.0 mW/gate and 1.3× (92 ps versus 118 ps) at 3.0 mW/gate are obtained compared with the conventional ECL circuit. Scaled performance of the conventional ECL circuit and the present circuit at 0.5 μm design rules are shown in Fig. 5.

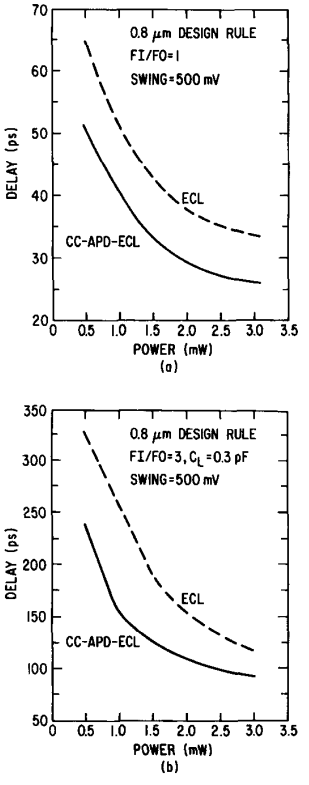

Fig. 4. (a) Unloaded (FI/FO = 1) power-delay characteristics, and (b) loaded (FI/FO = 3, C_L = 0.3 pF) power-delay characteristics for the conventional ECL circuit and the CC-APD-ECL circuit at 0.8 μm design rule.

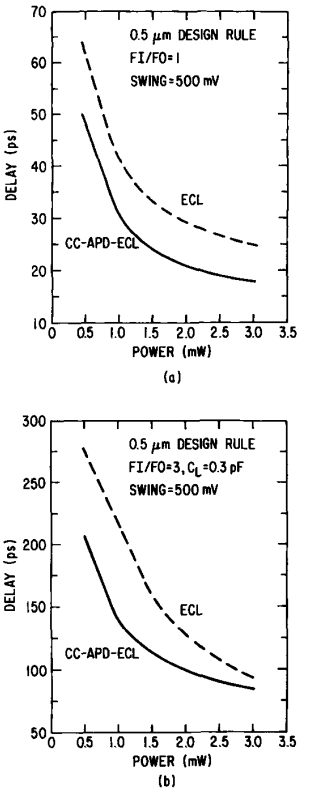

Fig. 5. (a) Unloaded (FI/FO = 1) power-delay characteristics, and (b) loaded (FI/FO = 3, C_L = 0.3 pF) power-delay characteristics for the conventional ECL circuit and the CC-APD-ECL circuit at 0.5 μm design rule.

For the unloaded case (FI/FO = 1, Fig. 5(a)), the present circuit achieves delays of 30 ps at 1.0 mW/gate and 17.7 ps at 3.0 mW/gate, respectively. For the loaded case (FI/FO = 3, C_L = 0.3 pF, Fig. 5(b)), the delays are 137 ps at 1.0 mW/gate and 84 ps at 3.0 mW/gate.

The superior load driving capability of the present circuit is shown in Fig. 6. At 0.8 μm design rule with FI/FO = 3 and 1.0 mW/gate, the circuit achieves a driving capability of 260 ps/pF, a 2.1× improvement over the 540 ps/pF for the conventional ECL circuit. Fig. 7(a) shows the schematics of 2-way output OR (emitter) dot using the present circuit. The superior dotting capability of the present circuit is illustrated in Fig. 7(b). The present circuit achieves a delay penalty of 22 ps/dot, a 3.5× improvement over the 77 ps/dot for the conventional ECL circuit.

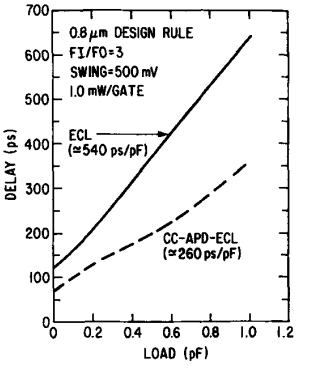

Fig. 6. Delay versus capacitive loading for the conventional ECL circuit and the CC-APD-ECL circuit. (0.8 μm design rule, FI/FO = 3, 1.0 mW/gate).

IV. Discussion

While the present circuit scheme is most effective in improving the power-delay of dual-phase ECL circuit, it can still offer significant power-delay improvement over the single-ended ECL circuit (≃20–25% improvement for a loaded gate at 1.0 mW/gate with 0.8 μm design rule). This is because there is only one emitter-follower branch conducting current in the steady-state in the present circuit. The circuit, therefore, does not add any current conducting (and hence power-consuming) branch to the single-ended ECL circuit while offering the advantage of active-pull-down.

Notice also that in the steady-state, the voltages at the base and collector of the individual active-pull-down transistor ($Q_{D,L}$ and $Q_{D,R}$) are either V_{OUT} and $V_{\overline{\mathrm{OUT}}}$ or vice versa. Hence, the "ON" pull-down transistor has its base-collector junction forward biased by a voltage equal to the signal swing of the circuit, while the "OFF" pull-down transistor has its

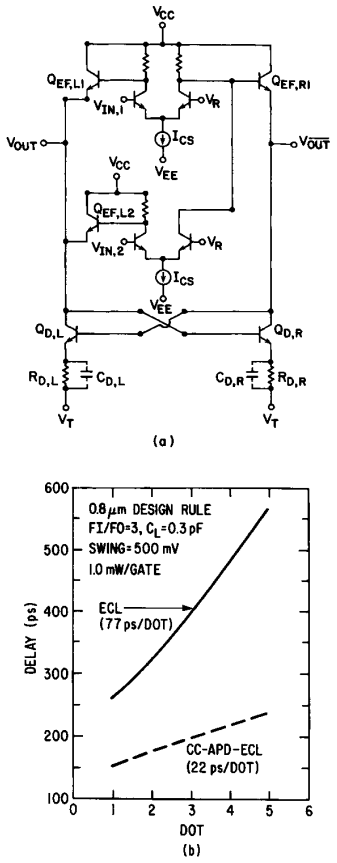

Fig. 7. (a) Schematics of 2-way output OR (emitter) dot using the CC-APD-ECL circuit, and (b) delay versus dot for the conventional ECL circuit and the CC-APD-ECL circuit. Notice that Dot = 1 equals no dotting. (0.8 μm design rule, FI/FO = 3, 1.0 mW/gate).

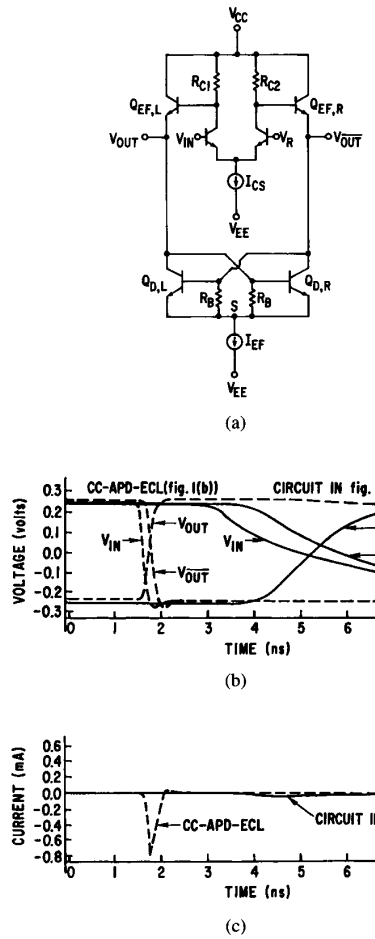

Fig. 8. (a) A cross-coupled active-pull-down ECL circuit with the emitters of the active-pull-down transistors ($Q_{D,L}$ and $Q_{D,R}$) tied together to a current source (I_{EF}) ([7]), and (b) pertinent waveforms during the switching transient for the CC-APD-ECL circuit and the circuit in Fig. 8(a) (waveforms are taken from a middle stage in a chain of similar gates), and (c) net pull-down current during the switching transient for the CC-APD-ECL circuit and the circuit in Fig. 8(a) (R_B = 10 KΩ in Fig. 8(a)). (0.8 μm design rule, FI/FO = 3, C_L = 0.3 pF, 1.0 mW/gate).

base-collector junction reverse biased by the same magnitude of voltage. As long as the signal swing remains smaller than, say, 2/3 of V_{BE} of the "ON" transistor, the pull-down transistors will be kept out from operating in the saturation region.

The value of the speed-up capacitors, $C_{D,L}$ and $C_{D,R}$, are chosen according to the loading condition to optimize performance. The capacitance value should be comparable to the loading capacitance (typically several tenths of a pF) at the output node to have significant speed-up effect.

It is also worthwhile to point out that while "similar" cross-coupled active-pull-down scheme, in which the emitters of the pull-down transistors are tied together to a current source (Fig. 8(a)) has been proposed [7], the separation of the emitters of the active-pull-down transistors in the present CC-APD-ECL circuit has very important implications and results in very significant performance enhancements as discussed below.

1) In the present CC-APD-ECL circuit, the emitter-follower branches can be terminated at a lower (magnitude vice) voltage. For the circuit in Fig. 8(a), because of the stacking of the active-pull-down transistors and the current source, larger supply voltage has to be used to terminate the emitter-follower branches (V_{EE} in Fig. 8(a)), thus increasing the power consumption.
2) In the present CC-APD-ECL circuit, the "OFF" emitter-follower branch is actually "conducting" a very small current with its corresponding pull-down transistor at "cut-in" condition. For the circuit in Fig. 8(a), the "OFF" side pull-down transistor is completely off, thus degrading the switching speed.
3) In the present CC-APD-ECL circuit, speed-up capacitors ($C_{D,L}$ and $C_{D,R}$ in Fig. 1(b)) can be easily introduced to provide a large dynamic current during the switching transient to enhance the power-delay performance. For the circuit in Fig. 8(a), although a speed-up capacitor can conceivably be introduced between Node S and V_{EE}, its speed-up effect will be limited (due to the reason

discussed below) and it also tends to skew the pull-up and pull-down delays.

4) Most fundamental, and probably most important as well, is the difference in the available pull-down current during the switching transient and the resulting performance difference between the two circuits.

Consider the case when the input V_{IN} switches from "High" to "Low" (Fig. 8(b)). For the present CC-APD-ECL circuit, once the current switch switches, the voltage at the output node V_{OUT} rises to "High," and this immediately provides a very strong base drive to turn on $Q_{D,R}$, resulting in a large dynamic current to pull-down $V_{\overline{\mathrm{OUT}}}$ as shown in Fig. 8(c). The large dynamic current also helps to turn off $Q_{D,L}$ and improve the pull-up of V_{OUT}.

For the circuit in Fig. 8(a), although V_{OUT} starts to rise to "High," the current from the current source I_{EF} continues to flow through $Q_{D,L}$ until V_{OUT} and $V_{\overline{\mathrm{OUT}}}$ cross each other. The only currents available to pull-down $V_{\overline{\mathrm{OUT}}}$ during this transition period are the base current of $Q_{D,L}$ and the (very small) current through the bleeding resistor R_B. The current from the current source I_{EF} will be available for pulling-down $V_{\overline{\mathrm{OUT}}}$ only after the crossing of V_{OUT} and $V_{\overline{\mathrm{OUT}}}$, and therefore does not help the switching at all. Even after V_{OUT} and $V_{\overline{\mathrm{OUT}}}$ cross each other, the maximum current available is still limited by I_{EF}. The continual flow of I_{EF} through $Q_{D,L}$ before the crossing of V_{OUT} and $V_{\overline{\mathrm{OUT}}}$ also severely degrades the pull-up of V_{OUT}. In Fig. 8(b) and Fig. 8(c), the slow pull-up and pull-down, as well as the small net pull-down current during the switching transient, can clearly be seen. Extensive simulations indicate that the circuit in Fig. 8(a) is about 3–5 times slower than the present CC-APD-ECL circuit under high loading and low power conditions. Finally, introduction of a speed-up capacitor between Node S and V_{EE} will not significantly improve the performance since the current from the speed-up capacitor will not be available until after the crossing of V_{OUT} and $V_{\overline{\mathrm{OUT}}}$.

V. Conclusion

In summary, we have described a new high-speed low-power ECL circuit featuring cross-coupled active-pull-down emitter-follower stages with the following advantages.

1) Cross-coupled biasing eliminates the extra biasing branches and power for the active-pull-down transistors.
2) Cross-coupled active-pull-down scheme provides a large dynamic current to improve the pull-down delay as well as the pull-up delay of the other output phase.
3) In the steady-state, only one emitter-follower branch is conducting, thus minimizing the power consumption.
4) Emitter dotting and series gating capability are preserved.

The superior power-delay performance, load driving capability, and emitter-dotting capability of the circuit were illustrated and key aspects of the circuit discussed.

References

[1] K. Y. Toh, C. T. Chuang, T. C. Chen, J. Warnock, G. P. Li, K. Chin, and T. H. Ning, "A 23 ps/2.1 mW ECL gate," *Dig. Tech. Papers, 1989 ISSCC*, pp. 224–225.

[2] K. Y. Toh, C. T. Chuang, T. C. Chen, and J. D. Warnock, "A 23 ps/2.1 mW ECL gate with an ac-coupled active-pull-down emitter-follower stage," *IEEE J. Solid-State Circuits*, vol. 24, no. 5, pp. 1301–1306, Oct. 1989.

[3] H. Itoh, T. Saitoh, T. Yamada, M. Yamamoto, and A. Masaki, "Advanced ECL with new active pull-down emitter-followers," in *Proc. 1988 IEEE Bipolar Circuits and Technology Meeting*, pp. 23–25.

[4] C. T. Chuang and K. Chin, "A high-speed low-power charge-buffered active-pull-down ECL circuit," in *Proc. 1990 IEEE Bipolar Circuits and Technology Meeting*, pp. 132–135.

[5] T. C. Chen, J. D. Cressler, K. Y. Toh, J. Warnock, P. F. Lu, K. A. Jenkins, S. Basavaiah, M. P. Manny, H. Y. Ng, D. D. Tang, G. P. Li, C. T. Chuang, M. R. Polcari, M. B. Ketchen, and T. H. Ning, "A submicron high performance bipolar technology," in *Dig. Tech. Papers, Symp. VLSI Tech.*, 1989, pp. 87–88.

[6] T. C. Chen, K. Y. Toh, J. D. Cressler, J. Warnock, P. F. Lu, D. D. Tang, G. P. Li, C. T. Chuang, and T. H. Ning, "A submicrometer high-performance bipolar technology," *IEEE Electron Device Lett.*, vol. 10, no. 8, pp. 364–366, Aug. 1989.

[7] P. Rydval, "Monolithic digital semiconductor circuit comprising a plurality of bipolar transistors," U.S. Patent 4 276 485, June 30, 1981.