Programmable CMOS Switched-Capacitor Biquad Using Quasi-Passive Algorithmic DAC's

Nuno Paulino, José E. Franca, and F. P. Martins

Abstract—**This paper describes an electrically programmable switched-capacitor (SC) biquad using quasi-passive algorithmic digital-to-analog converters (DAC's). Since only two equal-valued capacitors are needed for programming each capacitance value, the proposed technique offers compact, cost-effective programmability when compared to traditional programming techniques employing binary-weighted capacitor-arrays (C-arrays). A demonstration prototype chip realized in a 1.2 μm CMOS double-metal double-poly technology, and which implements an 8 b programmable SC biquad giving a wide range of lowpass, bandpass and highpass filtering functions, occupies an active area of only 0.38 mm^2.**

I. Introduction

FIELD programmable IC's are receiving increased attention prompted by the need of realizing with the shortest possible delay time a variety of dedicated functions in custom specific IC applications [1]. Current research efforts have been primarily directed towards producing field programmable digital IC's with increased functionality and efficiency, but it is envisaged this trend will also expand into the area of field programmable analog IC's [2]. Although SC circuits are particularly advantageous for programming analog functions on-chip, previous implementations employing digitally controlled binary-weighted C-arrays (e.g., [3]–[5]) have required large areas of silicon and hence high cost of manufacturing.

In this paper a new technique is proposed for electrical programmability of SC biquads. It is based on the concept of *charge-programmability* realized using quasi-passive algorithmic digital-analog converters (DAC's), and leads to a significant reduction of the overall capacitor area needed for IC implementation and thus lower cost of manufacturing. Besides this introduction, the paper comprises five additional sections. Section II looks at the capacitance programming techniques of SC branches from the viewpoint of digital-to-analog converters, in particular the traditional binary-weighted C-array multiplying DAC as well as the proposed cost-effective algorithmic quasi-passive DAC. Section III describes the architecture of the programmable SC biquad using quasi-passive DAC's, and presents the systematic design methodology yielding the digitized coefficients needed for digital programming of each relevant SC branch. The design and experimental characterization of an 8-b programmable SC biquad realized using a 1.2 μm CMOS technology are given in Section IV. The conclusions are drawn in Section V.

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II. Electrically Programmable SC Branches

The traditional solution for electrical programmability of SC branches consists of replacing the associated capacitor by a binary-weighted C-array which can be programmed to a resolution of N-bits. In an SC network with K capacitors, a total of $K \times 2^N$ capacitors and $K \times N$ digital lines are required to program independently every capacitor and thus achieve full programmability of the SC network. Despite its simplicity, this solution needs high component count (both of capacitors and switches) and the number of control signals increases proportionately to the resolution of the C-arrays.

In order to reduce the capacitance spread as well as the number of capacitors and switches associated with the binary-weighted C-arrays we can utilize instead the quasi-passive algorithmic DAC illustrated in Fig. 1(top), with positive gain [6]–[8]. In the timing diagram represented in Fig. 1(bottom) each one of the switching waveforms S and T have N pulses synchronized with the N bits of the programming digital word where b_{N-1} is the most significant bit (MSB) and b_0 is the least significant bit (LSB). The pulses *SOC* (start of conversion) and *EOC* (end of conversion), respectively, determine the duration of the conversion process. For each sample of the input signal V_i, the conversion starts by resetting capacitor C_{1b} with pulse *SOC*. Then, if the LSB of the programming digital word is $b_0 = 1$, the first S pulse connects capacitor C_{1a} to V_i; in the subsequent T pulse, capacitor C_{1a} is connected in parallel with C_{1b} such that the charge $q_a = C_{1a}V_i$ divides between both capacitors and yields $q_b = (C_{1a}/2)\,V_i$. If $b_0 = 0$, then capacitor C_{1a} samples ground during the first S pulse and hence during the subsequent T pulse no charge flows into capacitor C_{1b}, i.e., $q_b = 0$. By repeating similar operations during the next S and T pulses capacitor C_{1b} accumulates the results of consecutive divisions by two of the charge sampled into C_{1a}. After all bits have been processed pulse *EOC* forces the final charge accumulated into capacitor C_{1b} to be transferred to the integrating feedback capacitor C_2 to produce an output voltage.

For simplicity, we designate $X = C_{1a} = C_{1b}$ as the equivalent capacitance value of the programmable SC branch. Hence, for a given N-bit programming digital word W_x, the effective multiplying capacitance value is given by

$$X[W_x] = \sum_{n=0}^{N-1} (b_n 2^{n-N}) X. \tag{1}$$

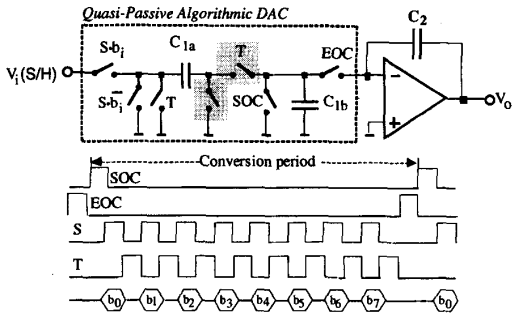

Fig. 1. (top) SC integrator employing a programmable positive SC branch with quasi-passive algorithmic DAC. (bottom) Switch timing.

Although N-bit resolution requires N clock cycles, the cycle period is short due to the inherent quasi-passive nature of the circuit [9]. Besides, since each programmable SC branch employs only two equal-valued capacitors it is rather practical for IC implementation, even for high-order SC filters with a rather large number of SC branches.

The complementary negative SC integrator is obtained from the circuit of Fig. 1 simply by interchanging switching waveforms S and T of the programmable quasi-passive DAC. In this circuit the serial D/A conversion also starts from the LSB to the MSB of the programming digital word but, unlike in the circuit of Fig. 1, the division by two is now performed during the S pulses when capacitors C_{1a} and C_{1b} are serially connected to the input terminal. During the T pulses, capacitor C_{1a} is discharged to ground while capacitor C_{1b} holds the result for accumulating with the next division.

The symbols shown in Fig. 2(a) and (b) are used to represent, respectively, a positive and a negative programmable SC branch. As indicated before, the letter X designates the equivalent capacitance value of that branch, i.e., $X = C_{1a} = C_{1b}$, whereas W_X represents the associated programming digital word. For an N-bit resolution the effective multiplying capacitance values for the most and the least significant bits are, respectively, $X/2$ and $X/2^N$.

III. Charge-Programmable SC Biquad

Based on the two-integrator loop topology [10] we derive the SC biquad of Fig. 3, which operates with the switching waveforms indicated in Fig. 1(b). Besides the programmable SC branches described before, we have also made the integrating capacitor B programmable using a 3-b binary-weighted C-array in parallel with a fixed capacitor. This allows some

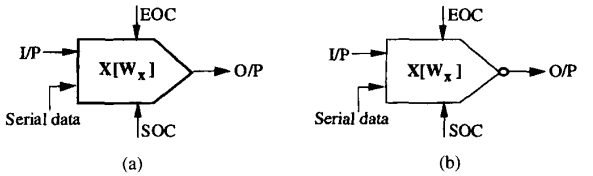

Fig. 2. Symbols representing the programmable (a) positive and (b) negative SC branches with quasi-passive algorithmic DAC's.

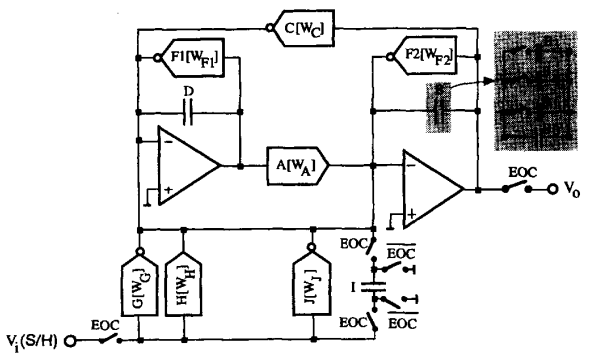

Fig. 3. Schematic diagram of the programmable SC biquad with quasi-passive algorithmic DAC's.

additional controllability of the voltage scaling at the output of the biquad. Both the integrating capacitor D as well as the input SC branch I have fixed capacitance values. For a sampled-and-held input signal, this biquad can be described by the z-transfer function shown in (2) at the bottom of the page.

To maximize the number of realizable transfer functions, we studied a variety of filtering functions to determine the varying ranges of the capacitance values and establish the appropriate design conditions for each programmable SC branch. Table I gives the equivalent capacitance values X, normalized to the unit capacitance value C_u, which are used in (1) to obtain the effective multiplying capacitance values for the associated programming digital words. The normalized capacitance values for the remaining capacitors B, D, and I in the biquad are also included in Table I.

The design equations of the programmable SC biquad are determined by equating the z-transfer function (2) to the general biquadratic function

$$H(z) = K \times \frac{1 + a_1 z^{-1} + a_2 z^{-2}}{1 - b_1 z^{-1} + b_2 z^{-2}}. \tag{3}$$

$$H(z) = -\frac{1}{B(W_B)} \times \frac{I - \left\{ I - I\frac{F_1(W_{F_1})}{D} + [H(W_H) - J(W_J)] \right\} z^{-1} + \left\{ G(W_G)\frac{A(W_A)}{D} + \left[1 - \frac{F_1(W_{F_1})}{D}\right][H(W_H) - J(W_J)] \right\} z^{-2}}{1 - \left\{ \left[1 - \frac{F_1(W_{F_1})}{D}\right] + \left[1 - \frac{F_2(W_{F_2})}{B(W_B)}\right] \right\} z^{-1} + \left\{ \frac{A(W_A)C(W_C)}{B(W_B)D} + \left[1 - \frac{F_1(W_{F_1})}{D}\right]\left[1 - \frac{F_2(W_{F_2})}{B(W_B)}\right] \right\} z^{-2}} \tag{2}$$

TABLE I
NOMINAL CAPACITANCE VALUES OF THE SC BIQUAD

$A = 14\,C_u$	$C = 3\,C_u$	$D = C_u$
$F_1 = 3\,C_u$	$F_2 = 6\,C_u$	$G = 7\,C_u$
$H = 4\,C_u$	$I = C_u$	$J = 3\,C_u$
$B = C_u$ to $15C_u$, with increments of $2C_u$		

To establish a unique set of programmable capacitance values for each set of coefficients K, a_1, a_2, b_1, and b_2, we have pre-determined a few preferred default values that give a first-cut design solution covering a wide coverage of filtering specifications. From Table I, and assuming $C_u = 1$, we obtain the following design equations

$$B = 1/K \tag{4a}$$

$$A = \{0.5 \text{ or } 1 \text{ or } 2\} \tag{4b}$$

$$F_1 = \{0 \text{ or } (1 = b_1 + 0.3) \text{ or } (2 - b_1 - 0.1\} \tag{4c}$$

$$J = \{0 \text{ if } (1 = F_1 + a_1) < 0 \text{ or } (1 = F_1 + a_1) \text{ otherwise } \} \tag{4d}$$

$$H = \{0 \text{ if } (1 - F + 1 + a_1) > 0 \text{ or } (1 - F_1 + a_1) \text{ otherwise } \} \tag{4e}$$

$$G = [(J - H)(1 - F_1) + a_2]/A \tag{4f}$$

$$F_2 = (2 - F_1 - b_1)B \tag{4g}$$

$$C = [(b_2 - (1 - F_1)(1 - F_2/B)]B/A. \tag{4h}$$

By computer simulations, we determine from the above calculated normalized capacitance values the resulting voltage swing at the output of the amplifiers and, whenever necessary, scale the appropriate capacitance values in order to achieve the required signal handling capability [13]. Once this is accomplished, the complete set of capacitance values thereby obtained can be readily digitized.

IV. INTEGRATED CIRCUIT IMPLEMENTATION AND RESULTS

A. Prototype CMOS IC

The classical folded cascode transconductance amplifier is used for the prototype IC realization of the above programmable SC biquad [11]. A single bias circuit is shared by both amplifiers needed in the SC biquad.

It is known that the quasi-passive algorithmic DAC's employed in the above programmable SC biquad are not fully insensitive to grounded parasitic capacitances [9], [12], but their effect can be reduced to negligible levels by ensuring the relevant grounded parasitic capacitances are ideally the same. Essentially, this can be achieved using a symmetric layout for capacitors C_{1a} and C_{1b} in Fig. 1. The schematic representation of the layout plan adopted for the two nominally equal capacitors of all quasi-passive programmable SC branches in the biquad is illustrated in Fig. 4.

The capacitors are built using a standard unit capacitor of value $C_u = 0.5$ pF; several of these are connected together to obtain larger capacitors. All capacitors are joined together in a cluster over an N-TUB connected to the analog ground in order to obtain adequate isolation from the noisy substract. The capacitor cluster is positioned between the amplifiers and the switches, so that the former are as far way as possible from the noisy digital circuitry. An N-TUB was also implanted under the analog bus.

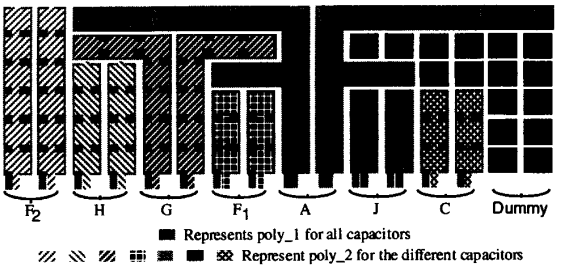

Fig. 4. Layout plan of the pairs of nominally equal capacitors in the programmable SC branches for matched grounded parasitic capacitances.

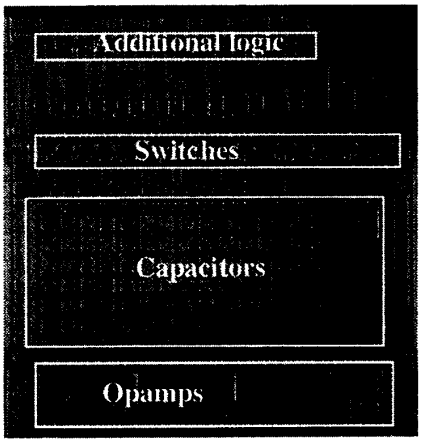

Fig. 5. Microphotograph of the 1.2 μm CMOS prototype chip.

The prototype IC was realized using a 1.2 μm CMOS technology yielding a total active area of 0.38 mm^2. The resulting chip microphotograph is shown in Fig. 5. Next, we discuss the experimental characterization of both the quasi-passive algorithmic DAC extensively employed in the programmable SC biquad as well as the resulting programmable filtering capabilities.

B. Linearity of the Quasi-Passive Logarithmic DAC

In order to characterize the quasi-passive algorithmic DAC we measured the response of the SC biquad configured as a first-order filter (Fig. 6), when the input signal is a square waveform with frequency f_{test} and amplitude A_{test}. From (2), the corresponding z-transfer is given by

$$H(z) = -\frac{(I/B)}{1 - [1 - (F_2/B)]z^{-1}} \tag{5}$$

yielding

$$H_0 = \frac{I}{F_2} \tag{6a}$$

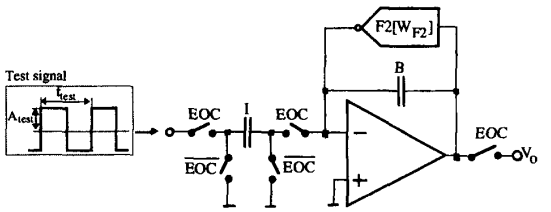

Fig. 6. SC biquad configured as a first-order lowpass filter for testing the linearity of the algorithmic DAC.

TABLE II
CONDITIONS FOR THE SQUARE WAVE TEST SIGNAL

Digital Codes of F_2	Amplitude of Test Signal (mV)	Frequency of Test Signal (Hz)
1 → 9	20	10
10 → 18	50	50
19 → 42	100	100
43 → 62	200	200
63 → 106	300	200
107 → 133	500	500
1134 → 179	600	500
180 → 198	800	1000
199 → 222	900	1000
223 → 255	1000	1000

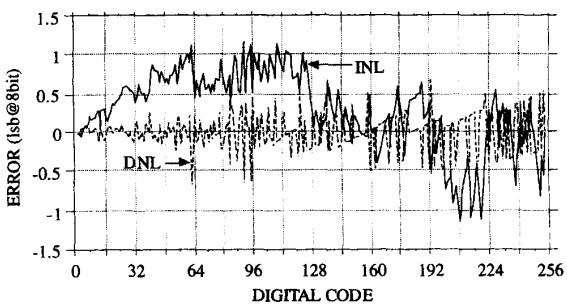

Fig. 7. INL and DNL characteristics of the programmable F_2 SC branch.

for the dc gain, H_0, and

$$f_c = \left(\frac{F_s}{2\pi}\right) \cdot \left(\frac{F_2}{B}\right) \tag{6b}$$

for the -3 dB cut-off frequency, f_c. From the results above, we established the measuring conditions indicated in Table II in order to prevent output voltage clipping of the amplifier and maintain $f_{\text{test}} \ll f_c$, for negligible gain errors. Then, from the measured gain as a function of F_2 we extrapolated the differential and integral nonlinearity characteristics shown, respectively, in Fig. 7.

C. Programmable Filtering Functions

The testing of the filtering capabilities of the programmable SC biquad was carried out for a sampling frequency of 54.4 kHz, pole frequency of 1 kHz and 2 kHz and pole Q-factor of 1, 5, and 10. The resulting measured amplitude responses shown in Fig. 8 are in good agreement with the corresponding nominal responses. Within the programming range of the

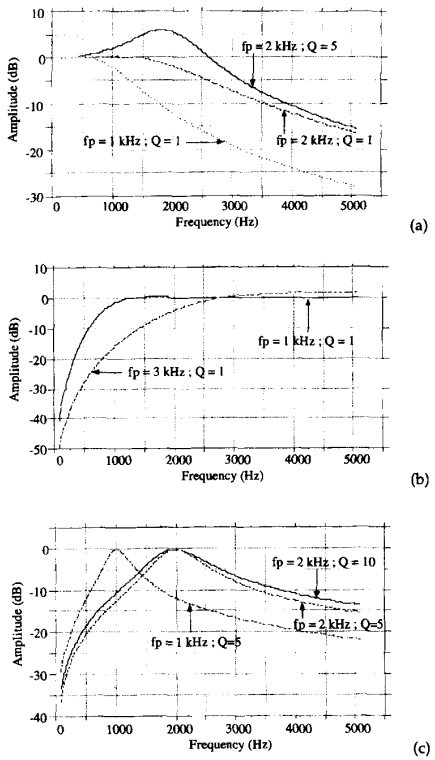

Fig. 8. Measured responses showing the programmability of the filtering shape, pole frequency and pole Q-factor. (a) Lowpass. (b) Highpass. (c) Bandpass.

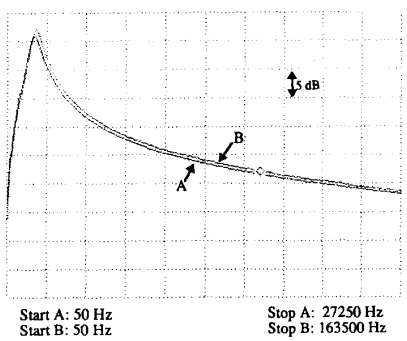

Fig. 9. Superimposed responses at $F_s = 54.4$ kHz and $F_s = 326$ kHz when the SC biquad is configured as a bandpass filter with 2 kHz pole frequency and $Q = 5$.

SC biquad, similar results were obtained for different pole frequencies and Q-factors as well as for higher sampling frequencies. For example, the measured results of Fig. 9 represent superimposed responses of the SC biquad configured as a lowpass filter, with 2 kHz pole frequency, $Q = 5$ and sampling frequencies of 54.4 kHz and 326 kHz (algorithmic conversion up to approximately 2.9 MHz). Finally, we can observe in Fig. 10 the measured spectral contents of the output signal of the SC biquad, configured as an 8 kHz lowpass filter with $Q = 1$, when the test signal is a 1 kHz sinusoid

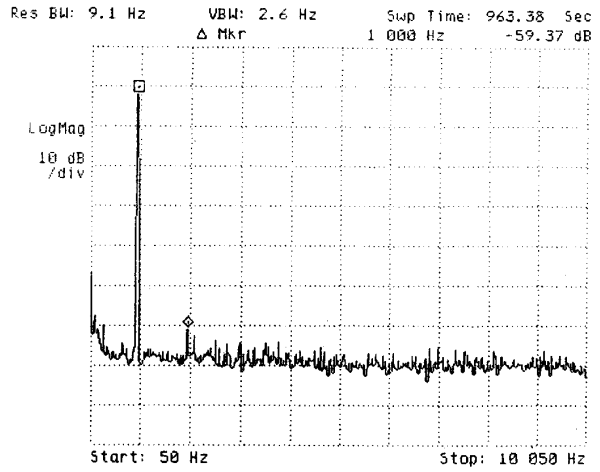

Fig. 10. Spectral contents of the output signal of the SC biquad, configured as a lowpass filter with 8 kHz pole frequency and $Q = 1$, when the test signal is a 1 kHz sinusoid with 2 V peak-to-peak.

TABLE III
SUMMARY OF THE MEASURED CHARACTERISTICS OF THE PROGRAMMABLE SC BIQUAD

Technology	CMOS 1.2 μm DPDM
Active Area	0.38 mm^2
Supply	5 V
Power Dissipation @ F_{clock} = 490 kHz	12 mW
THD (lowpass filter) (F_S = 54.4 kHz; 2 Vpp @ 1 kHz)	0.12 %
SNR (lowpass filter) (F_S = 54.4 kHz; 2 Vpp @ 1 kHz)	66 dB
DNLof Programmable SC branches	< ± 0.7 LSB @ 8-bit
INL of Programmable SC branches	< ± 1.2 LSB @ 8-bit
Coefficients Programmability	8-bits

with 2 V peak-to-peak. The resulting total harmonic distortion at this signal level is approximately 0.12%. A summary of the relevant measured characteristics of the programmable SC biquad is given in Table III.

V. CONCLUSION

This paper describes the practical implementation of a novel technique for electrical programmability of SC biquad sections based on the concept of charge-programmability. This is realized using quasi-passive algorithmic digital-to-analog converters which need much less capacitor area than would be required by traditional programming techniques. The experimental characterization of a 1.2 μm CMOS prototype chip demonstrated the linearity characteristics of the algorithmic converters which realize the programmable SC branches and the programmability of lowpass, highpass and bandpass filtering responses with varying pole frequency and Q-factor.

REFERENCES

[1] G. F. Watson, "Technology 1992—Solid-state," *IEEE Spectrum*, pp. 42–44, Jan. 1992.
[2] M. Ismail and S. Bibyk, "CAD latches onto new techniques for analog ICs," *IEEE Circuits and Devices*, pp. 11–17, Sept. 1991.
[3] R. Gregorian "High resolution switched-capacitor D/A converter," *Microelectronics J.*, no. 12, 1981.
[4] D. J. Allstot, R. W. Brodersen, and P. R. Gray, "An electrically programmable switched-capacitor filter," *IEEE J. Solid-State Circuits*, vol. SC-14, pp. 1034–1041, Dec. 1979.
[5] "CSC7008 digital programmable universal filter," Product Data Sheet, Crystal Semiconductor Corporation.
[6] F. P. Martins, N. Paulino, and J. E. Franca, "Charge programming techniques for SC biquads," in *Proc. IEEE ISCAS 93*, Chicago, IL, May 1993, pp. 1160–1163.
[7] V. F. Dias, J. E. Franca, and J. C. Vital, "High-speed offset compensated D/A convertor with a passive switched-capacitor algorithmic technique," *Electron. Lett.*, vol. 24, no. 17, pp. 1063–1064, Aug. 1988.
[8] J. E. Franca and J. C. Vital, "Low-cost algorithmic digital-analog converter for high-frequency applications," in *Proc. CICC 1990*, Boston, MA, May 1990.
[9] J. C. Vital and J. E. Franca, "Programmable quasi-passive algorithmic digital-analog converter," *Microelectronics J.*, vol. 23, pp. 17–27, 1992.
[10] P. Fleischer and K. Laker, "A family of active switched-capacitor biquad building blocks," *Bell Syst. Tech. J.*, pp. 2235–2269, Dec. 1979.
[11] D. Senderowicz, "CMOS operational amplifiers," in *Design of Analog-Digital VLSI Circuits for Telecommunications and Signal Processing*, J. E. Franca and Y. Tsividis, Eds. Englewood Cliffs, NJ: Prentice-Hall, 1994, ch. 5.
[12] K. R. Laker, P. E. Fleischer, and A. Ganesan, "Parasitic insensitive, biphase switched capacitor filters with one operational amplifier per pole pair," *Bell Syst. Tech. J.*, pp. 685–707, 1982.
[13] R. Gregorian and G. Temes, "Switched-capacitor filters," in *Analog MOS Integrated Circuits for Signal Processing*. New York: Wiley, 1986, ch. 5.